Carbon nanotube neurotransistors with ambipolar memory and learning functions

Ertürk Enver Yildirim, Luis Antonio Panes-Ruiz, Pratyaksh Yemulwar, Ebru Cihan, Bergoi Ibarlucea,* and Gianaurelio Cuniberti*

In recent years, neuromorphic computing has gained attention as a promising approach to enhance computing efficiency. Among existing approaches, neurotransistors have emerged as a particularly promising option as they accurately represent neuron structure, integrating the plasticity of synapses along with that of the neuronal membrane. An ambipolar character could offer designers more flexibility in customizing the charge flow to construct circuits of higher complexity. We propose a novel design for an ambipolar neuromorphic transistor, utilizing carbon nanotubes as the semiconducting channel and an ion-doped sol–gel as the polarizable gate dielectric. Due to its tunability and high dielectric constant, the sol–gel effectively modulates the conductivity of nanotubes, leading to efficient and controllable short-term potentiation and depression. Experimental results indicate that the proposed design achieves reliable and tunable synaptic responses with low power consumption. Our findings suggest that the method can potentially provide an efficient solution for realizing more adaptable cognitive computing systems.

Impact statement

The huge amount of data generated by the current society makes it necessary to explore new computing methods with higher efficiency to overcome the bottleneck formed between data storage and processing tasks. Neuromorphic computing aims at emulating the functioning of our brain, which performs both tasks utilizing the same hardware. Here, we propose ambipolar field-effect transistors based on carbon nanotubes with a polarizable gate dielectric, capable of providing memory functions reminiscent of neuronal synapses, at both polarities of the device. The ambipolar characteristic doubles the possibilities of previously demonstrated neurotransistors. The short-term and ambipolar behavior of the device can find its place in novel applications in the future. Machine learning-enabled gas sensing is an excellent example, where real-time processing of large amounts of data is beneficial. In addition, interaction with oxidative and reductive gases will result in dual responses due to the ambipolarity of the transistor, along with the possibility of storing the sensing data.

Introduction

The demand for high hardware performance has increased in recent years due to the rise of data-intensive computing applications, which require features, such as low access latency, large bandwidth, high capacity, low cost, and the ability to perform artificial intelligence (AI) tasks.[1] However, big data poses additional challenges, such as high energy consumption and limited memory bandwidth. Traditional computer architecture has limitations that affect its performance, such as the von Neumann bottleneck.[2] This bottleneck arises from the separation of processor and memory, requiring data to be transferred between them through a single bus, limiting the overall performance of the system. To address these challenges, neuromorphic computing research is being conducted, aiming to develop computing systems that mimic the way the human brain processes information.[3] This field includes research on neuromorphic materials and devices, circuits, algorithms, and applications. Neuromorphic computing is considered as a potential solution to the challenges faced by conventional computers and is projected to grow rapidly

Ertürk Enver Yildirim, Institute for Materials Science and Max Bergmann Center for Biomaterials, Technische Universität Dresden, Dresden, Germany
Luis Antonio Panes-Ruiz, Institute for Materials Science and Max Bergmann Center for Biomaterials, Technische Universität Dresden, Dresden, Germany
Pratyaksh Yemulwar, Institute for Materials Science and Max Bergmann Center for Biomaterials, Technische Universität Dresden, Dresden, Germany
Ebru Cihan, Institute for Materials Science and Max Bergmann Center for Biomaterials, Technische Universität Dresden, Dresden, Germany
Bergoi Ibarlucea, Institute for Materials Science and Max Bergmann Center for Biomaterials, Technische Universität Dresden, Dresden, Germany; bergoi.ibarlucea@tu-dresden.de
Gianaurelio Cuniberti, Institute for Materials Science and Max Bergmann Center for Biomaterials, Technische Universität Dresden, Dresden, Germany; gianaurelio.cuniberti@tu-dresden.de
*Corresponding authors
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in the coming years, with an estimated market size of USD$22 billion by 2035.[4]

To advance neuromorphic computing and engineering, it is crucial to explore new materials and devices that can disruptively improve the power efficiency and scalability of current solutions. Most of the reported works have focused on the function and plasticity of biological synapses as key elements in the interlacing between neurons.[5–7] However, the neuron as a whole is also a critical element taking part in memory processes through its intrinsic plasticity[8] by nonlinearly integrating the received information in the cell membrane and generating new signals for other postsynaptic neurons. In contrast with many of the previously mentioned synaptic devices, transistors as three-terminal devices resemble with better fidelity the structure of neurons,[9] with a signal that travels over long distance from an input to an output (source and drain) and which is modulated on its way by the input of at least another terminal (gate).

The use of transistor-based artificial neurons and synapses has gathered significant interest due to their ability to emulate complex synaptic functions, perform learning operations and signal transmissions synchronously, and utilize multiterminal geometries to process information in a nonlinear manner, switch and amplify electric signals, such as biological neurons.[10] More specifically, ion-gated transistors utilize the movement of ions in the vicinity of the semiconductor surface to imitate the dynamic behavior of biological synapses and neurons. These transistors can effectively replicate synaptic weight modulation through ion electrochemical doping at the dielectric/channel interface. Furthermore, the multiterminal design of the ion-gated neuromorphic transistor allows neurons to replicate their information processing capabilities.[11] However, these devices suffer from slow switching speeds due to the inherent slow speed of ion movement. For example, our previously reported work[12] proposed an ion-gated transistor where the memory effect relied on the use of a polarizable ion-doped sol–gel interfaced with the semiconductor channel as a dielectric gate. The polarization was based on ionic drift and diffusion in the porous sol–gel material under modulation of presynaptic gate input. Derivatives of sol–gel materials have been observed to exhibit high dielectric constant, high breaking strength, and low dielectric loss, making them appealing candidates for use in energy-storage devices and electronics.[13,14] Adjusting various parameters, including precursor composition, solvent, processing conditions, and post-treatment techniques, enables tailoring the overall properties of the sol–gel to meet specific application demands. In the aforementioned work, despite the speed limitation, the device showed a nonlinear sigmoidal potentiation of time-dependent inputs, which emulated the dynamics of neuronal membrane integration by temporarily enhancing the output current. The device architecture with multiple gate inputs as synaptic inputs and the transistor output as an axon terminal emulated the information processing of a true neuron. Experimental results demonstrated the nonlinear information processing ability based on the intrinsic plasticity of a neurotransistor, which can be controlled to generate and reach faster or slower spike thresholds to control the rate of the spike. Furthermore, the semiconductor channel of the device was based on silicon nanowires. These, together with other 1D, 2D, or organic materials, are in a nonmature state but offer potentially promising approaches. These options may offer extended functionalities and present new opportunities for flexible electronics or 3D integration.[15]

Most transistors present unipolar charge transport, limiting the learning capabilities. Some strategies can be used to achieve ambipolarity, such as using thin films of semiconductor polymer blends, incorporating materials with different (*p*- or *n*-type) behaviors.[16] However, high-material complexity results in longer fabrication times and higher costs due to the additional steps required to deposit and pattern more materials.[17] For this reason, it is preferable to follow a simpler strategy implementing a single component with intrinsic ambipolar characteristics. Field-effect transistors (FETs) based on semiconducting single-walled carbon nanotubes (sc-SWCNTs) are appropriate candidates. Their transfer characteristics present a V or U shape with a transition from the hole to the electron conduction region around the Dirac point, holding great promise for ambipolar neuromorphic performance. The ambipolar behavior of sc-SWCNTs is primarily due to their narrow bandgap, enabling the injection of both carrier types as the gate voltage is raised above or below the flat band voltage, provided that the work function of the source/drain electrodes is similar. The fabrication of CNT-FETs is also simpler compared to that of silicon nanowire FETs, where etching, doping, annealing, and oxide growth steps are required among others.[18] Our group recently demonstrated that an automated dielectrophoretic alignment methodology was possible to achieve multiple highly uniform CNT-based devices in a single chip and with wafer-scale fabrication compatibility.[19] The existence of commercial inks for printing technologies enables industrial fabrication of large-area electronics, even on flexible devices.

In this research work, CNTs are coated with a polarizable sol–gel silicate film containing metal ions, resulting in the fabrication of ambipolar neurotransistors (**Figure 1**). The use of sol–gel material offers a cost-effective option compatible with current semiconductor processes.[20] Additionally, sol–gel-derived porous silica films have shown low dielectric constant and loss as well as high mechanical flexibility due to their porous nature.[21] The proposed scheme allows emulation of the inherent plasticity observed in neurons. By polarizing the gate material, a short-term memory effect is induced, leading to ambipolar memory behavior that can occur in both branches of the current–voltage characteristics. This combined approach incorporates the advantages associated with ambipolar neurotransistors, including the unique mechanical, electrical, thermal, and chemical properties of carbon nanotubes.

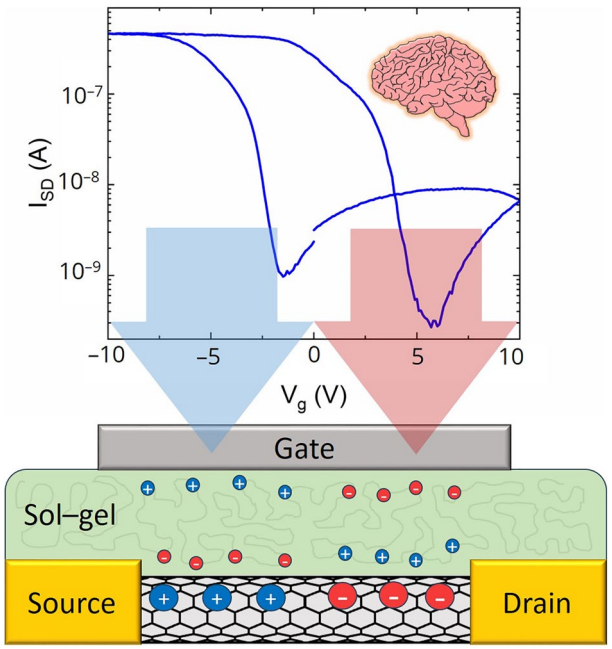

Figure 1. Concept of the current work. An ambipolar field-effect transistor based on carbon nanotubes is modified with a sol–gel dielectric gate material loaded with mobile metal ions. Polarization of the sol–gel layer upon gate potential modulation is the base for memory functions, which can happen in the two conduction regions (holes and electrons) of the device.

Results

Sol–gel-modified CNT-FET characterization

CNT-based neurotransistors were fabricated by depositing a metal-ion-doped sol–gel film on a silicon wafer chip containing thin-film gold electrodes bridged by carbon nanotubes, followed by the evaporation of a thin silver film as the gate electrode (see "Materials and methods" section for details). The mobility of copper and nickel ions in the porous sol–gel in response to the applied gate potential is the main principle of the memory effects of the neurotransistor. The performance of the neurotransistor is influenced by the structure and concentration of metal dopants in the film. Due to the random distribution of metal ions in the sol–gel during gelation, the polarization of the film is zero. However, applying a positive or negative bias across the dielectric film causes the ions to redistribute under the influence of the electric field. Although the ions diffuse back to a random distribution once the bias is removed, the diffusion rate is slower than the previous drift caused by the applied voltage, resulting in a memory effect. When a bias is applied for a prolonged period (around 100 ms), positive and negative ions accumulate and produce a field effect on the transistor channel. With a sufficiently strong effective field, a dipole moment is induced, leading to a steady increase in current until saturation is reached. In our previous work,[12] it was observed that the sol–gel film acted as a dielectric material whose dielectric constant changed significantly with the concentration of metal dopants at frequencies below 100 Hz. However, the dielectric constant remained constant and was no longer affected by the ionic concentration at frequencies above 100 Hz. The incorporation of the trimethoxymethylsilane (MTMS) precursor into the sol–gel film was aimed at enhancing its neuromorphic properties. The addition of organic precursors can also have an impact on the microstructure and properties of the resultant coating, including adhesion, hardness, and optical characteristics. The MTMS precursor has been demonstrated to increase the pore density while decreasing the pore volume, thereby increasing the porosity of the gate material.[22,23] However, the introduction of pores compromises the dielectric properties of the material by reducing its dielectric constant. The extent of this effect depends on several factors, such as MTMS concentration, type and concentration of other precursors, reaction conditions (temperature and pH), and post-treatment processes. Therefore, the effect of MTMS on the porosity of sol–gel materials should be evaluated on a case-by-case basis. The MTMS/TMOS ratio was selected based on a prior investigation which demonstrated that the 3:2 proportion exhibited the lowest leaching potential.[24]

The thickness of the sol–gel gate film was measured using scanning electron microscopy (SEM) and was determined to be approximately 2.8 μm, as depicted in **Figure 2**a. The surface morphology of the deposited films was examined using atomic force microscopy (AFM), and Figure 2b displays the observed results. The depth of the pores within the films ranged between 17 and 26 nm, while the width of the pores varied from 115 to 175 nm.

Figure 2c illustrates the transfer characteristics of the sol–gel-modified CNT-FET at different voltage sweeping speeds. At high sweeping rates, the transfer characteristics exhibit a low ON/OFF current ratio of 10 with unipolar behavior. Conversely, when voltage sweeping rates are slow, a high ON/OFF ratio of 10^3 is observed, accompanied by slight ambipolarity. The ratio of hole conduction to electron conduction follows an order of 10^2. Leakage current, depicted in Figure 2d, was approximately 10^{-9} A and its behavior varied with different voltage sweeping speeds. The leakage current reveals the presence of a polarization switch within the porous gate material, demonstrating the short-term retention of the polarization. This behavior is analogous to that of a lossy dielectric material with free charge carriers or defects.[25] The variations in results obtained with different voltage sweeping speeds can be attributed to slower ion dynamics within sol–gel thin films compared to ferroic or electronic ordering effects, as well as the presence of reductant Miller capacitances.[26,27] Specifically, the low mobility of ionic movement leads to increased ON/OFF current ratios and manifestation of ambipolar behavior when using lower voltage sweeping speeds. This effect is also observed in leakage current, where the hysteresis of voltage values at which current minima occur depends on the scan rate. This phenomenon is reminiscent of the hysteresis

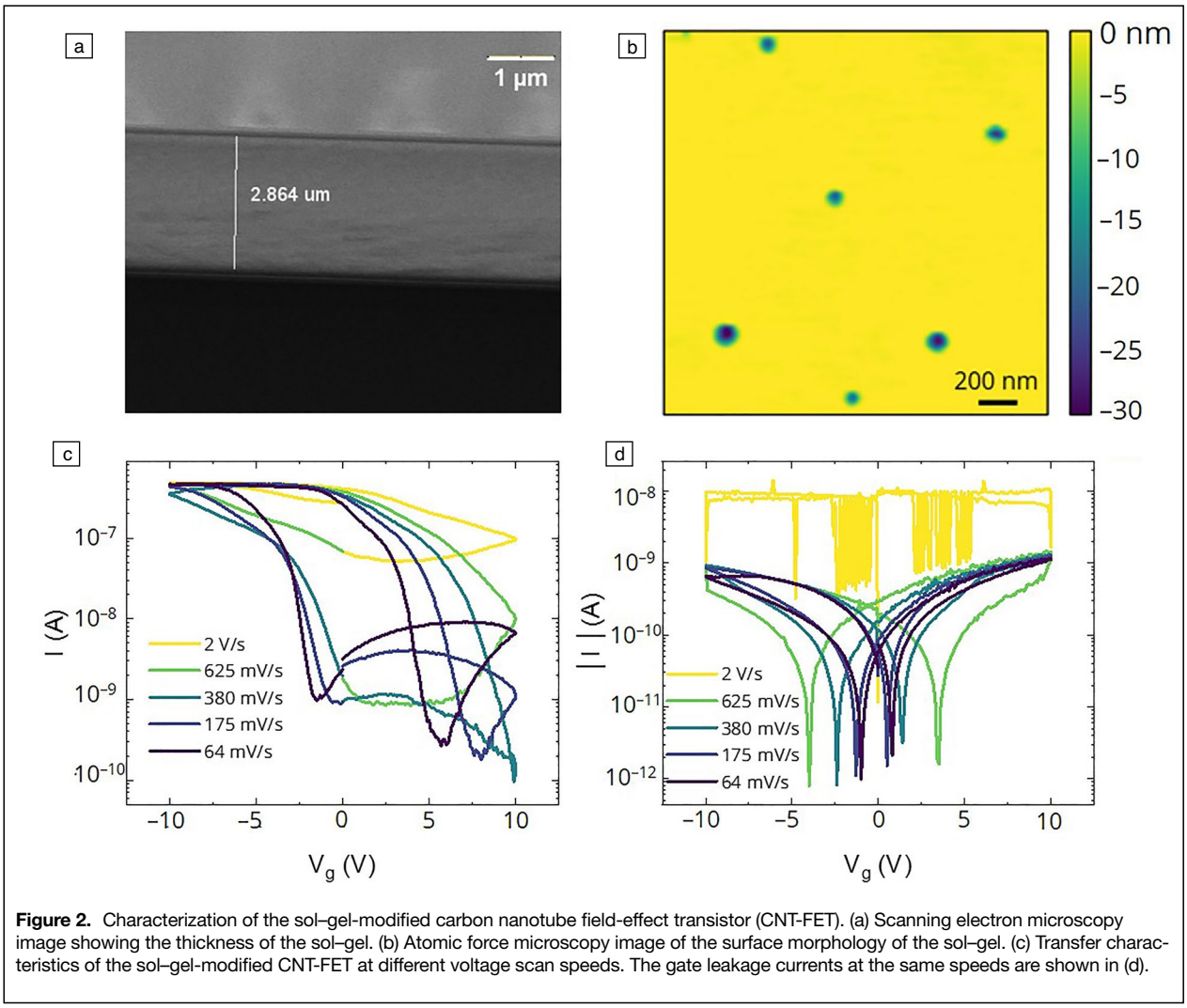

Figure 2. Characterization of the sol–gel-modified carbon nanotube field-effect transistor (CNT-FET). (a) Scanning electron microscopy image showing the thickness of the sol–gel. (b) Atomic force microscopy image of the surface morphology of the sol–gel. (c) Transfer characteristics of the sol–gel-modified CNT-FET at different voltage scan speeds. The gate leakage currents at the same speeds are shown in (d).

observed in memristive nanodevices, where fast scan rates do not allow sufficient time for the recovery of mobile charges along thin nanoscale semiconductors.[28] Moreover, the sol–gel-modified CNT-FET demonstrates comparable gate coupling to ion-sensitive FETs,[29,30] as evidenced by the highest subthreshold slope measured at 120 mV/dec with a voltage sweeping speed of 64 mV/s.

Enhanced gate coupling can significantly improve the efficiency of gate modulation and therefore the ambipolar behavior of CNT-FETs. To achieve better coupling in the future, it is crucial to obtain a thinner sol–gel film. Reducing the thickness of gate film would lead to steeper subthreshold slope due to higher capacitances.[17] This would be beneficial for neuromorphic computing due to low energy consumption and higher gain values, making the device more robust in terms of noise. At the same time, these high capacitance values could slow down the device further, making an optimization necessary. Various methods can be employed for this purpose, including longer plasma treatment durations, different deposition conditions such as adjusting baking temperatures, spin-coating speed, and accelerations, as well as varying proportions of solvents in the precursor mixture, among others.

In our experimental efforts, we explored higher water or isopropanol ratios and increased HCl concentrations, which resulted in the production of thinner sol–gels (approximately 234-nm thick, as depicted in Figure S1 of Supplementary information). However, the corresponding transfer characteristics exhibited a reduced ON/OFF ratio and hysteresis (Figure S2), rendering them unsuitable for memory applications. Additionally, we observed the absence of a distinct electron conduction branch. This could potentially be attributed to the decrease in dielectric properties caused by the increased presence of pores, as illustrated in the AFM image in Figure S3. Furthermore, raising the baking temperature proved to be impractical because temperatures exceeding 100°C caused cracking of the sol–gel (Figure S4).

An alternative approach was explored to enhance gate coupling by modifying the duration of air plasma treatment. Air plasma has the potential to increase the hydrophilicity of CNTs, thereby improving the adhesion of sol–gel to the

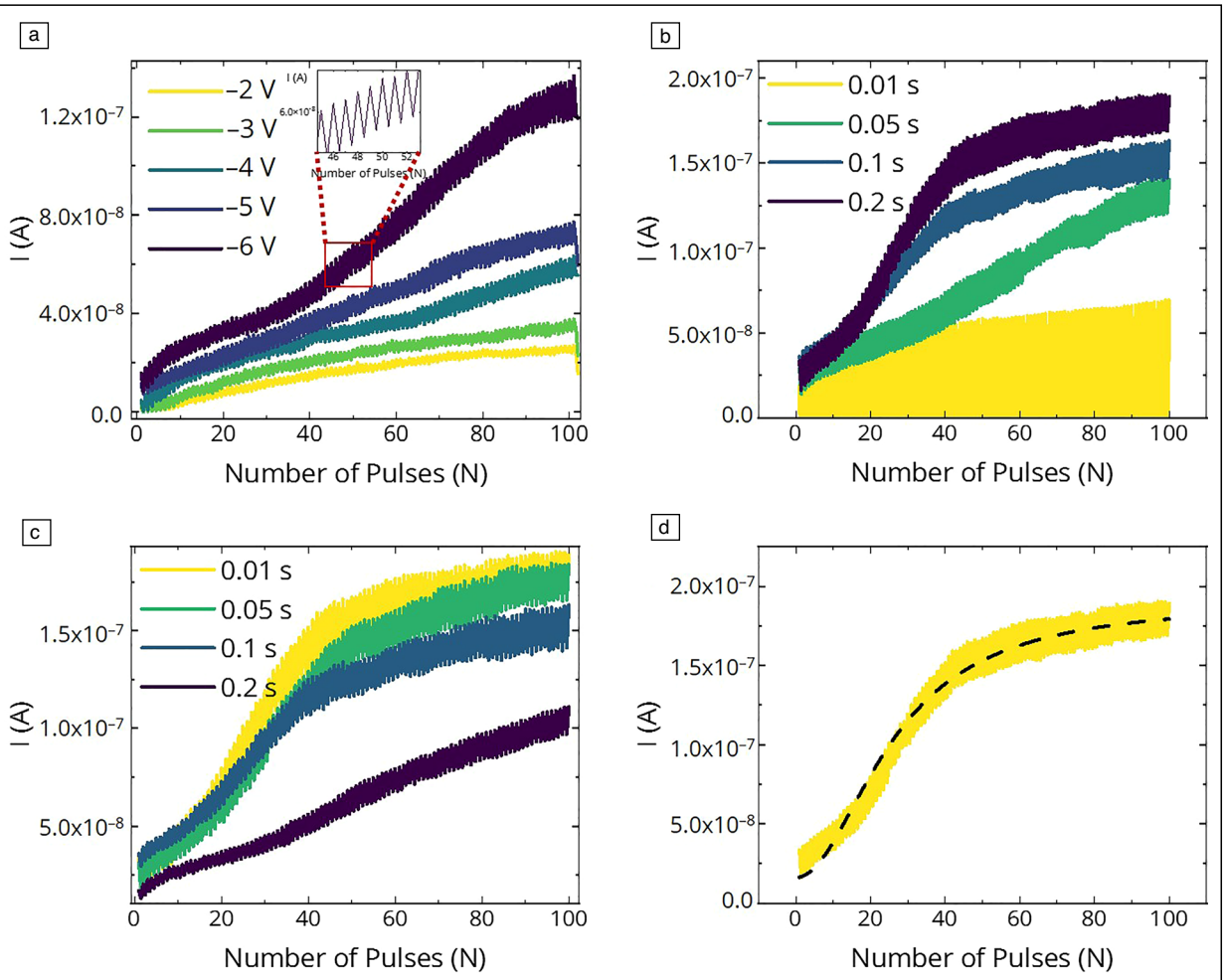

Figure 3. Short-term plasticity (STP) of the sol–gel-modified carbon nanotube field-effect transistors in the *p*-type region. (a) STP with different pulse amplitudes (from −2 V to −6 V) with 100-ms pulse width and 100-ms pulse interval. (b) STP at −6 V and 100-ms time intervals, pulse width varying between 0.01 and 0.2 s. (c) STP at −6 V and 100-ms pulse width, time intervals varying between 0.01 and 0.2 s. (d) Sigmoid function-fitted current corresponding to the input pulses with a pulse amplitude of −6 V, a pulse width of 100 ms, and a time interval of 10 ms.

CNT surface.[31] However, it can also hinder ambipolarity by reducing electron conduction and increasing hole conduction through the generation of oxygen defects on the CNT surface.[32,33] Fourier transform infrared spectroscopy (FTIR) was employed to analyze samples treated with air plasma durations for up to 10 s before sol–gel deposition, and the results are illustrated in Figure S5. The observed transmittance in the range of 1680–1800 inverse centimeters (1/cm) is attributed to C=O stretching, 1600–1680 (1/cm) to C=C stretching, approximately 2150 (1/cm) to C=C=O stretching, around 2349 (1/cm) to O=C=O stretching, and 3500–3780 (1/cm) to O–H stretching. The findings reveal that air plasma treatment rendered the SiO_2 surface with CNTs more hydrophilic, evident from the increased OH stretching, thereby promoting improved adhesion of the precursor solution to the surface. However, this process also resulted in the formation of oxygen defects in CNTs, which could potentially impede ambipolarity. These observations are consistent with prior reports.[31] Moreover, longer plasma treatments were found to cause the removal of CNTs from the surface, leading to a decrease in conductance. Notably, the absence of plasma treatment resulted in the absence of gate modulation, likely due to inadequate adhesion of the sol–gel to the substrate. Additionally, overlap between the gate and drain/source electrodes (Figure S6a) could give rise to unnecessary superfluous charging of Miller capacitances.

To mitigate the formation of Miller capacitances, samples with 6-µm SU8-5 passivation were prepared (as depicted in Figure S6b). However, sol–gel deposition on top of the SU8-5 induced defects due to the rough surface of the passivation layer (Figure S7). Furthermore, the viscosity of the sol–gel resulted in thicker gate films along the edges of the SU8-5 layer, leading to decreased gate coupling.

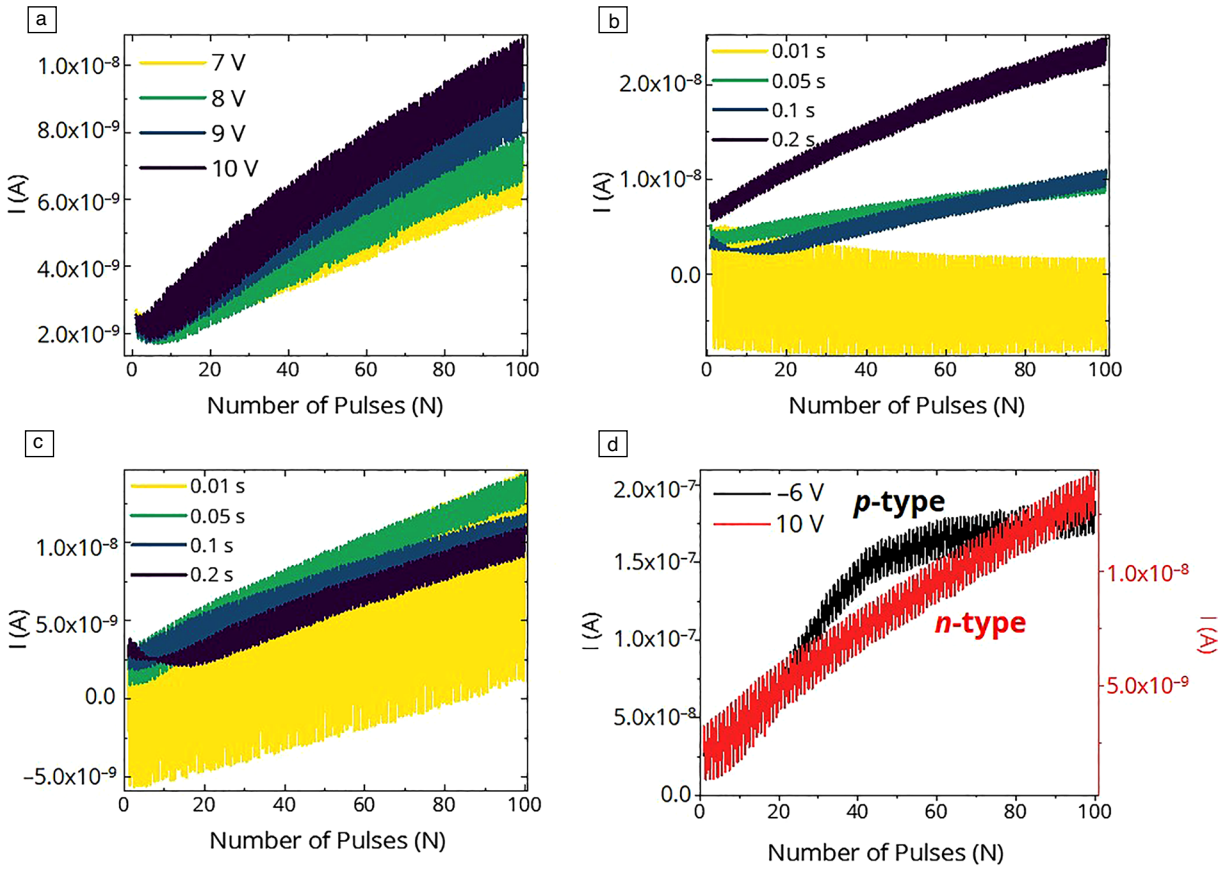

Figure 4. Short-term plasticity (STP) of the sol–gel-modified carbon nanotube field-effect transistors in the *n*-type region. (a) STP with different pulse amplitudes (from 7 to 10 V) with 100-ms pulse width and 100-ms pulse interval. (b) STP at 10-V and 100-ms time intervals, varying pulse width between 0.01 and 0.2 s. (c) STP at 10-V and 100-ms pulse width and time intervals varying between 0.01 and 0.2 s. (d) Comparison of learning curve in *p*-type and *n*-type modes, showing sigmoidal shape only for the *p*-type. Conditions of the *p*-type mode: −6 V, 100-ms pulse width, and 10-ms time interval. Conditions of the *n*-type mode: 10 V, 100-ms pulse width, and 50-ms time interval.

Short-term potentiation in the p*-type region*

To explore the influence of various pulse amplitudes on learning behavior in the *p*-type region, we employed pulses with a width and time interval of 100 ms each, resulting in a frequency of 5 Hz. The findings presented in **Figure 3**a demonstrate that higher pulse amplitudes correspond to a greater increase in drain current (I_{ds}).

To compare the effect of pulse widths on learning behavior in the *p*-type region, the pulse amplitude was fixed at −6 V, and the time interval was held constant at 100 ms. Figure 3b shows that longer pulse widths lead to increased potentiation, which is commonly observed in ionic-based neuromorphic devices.[11,12] On the other hand, very short pulse widths yield a greater change in capacitive current, which is assumed to be due to the width being insufficient for capacitance relaxation at the gate film. To compare the effects of different time intervals between subsequent pulses, the pulse width was maintained at a constant value of 100 ms and the pulse amplitude was fixed at −6 V. The measurements presented in Figure 3c revealed that shorter time intervals led to higher degree of potentiation. Notably, the presynaptic spike-timing-dependent plasticity (STDP) of the short-term plasticity (STP) behavior of the neuromorphic transistor exhibited greater sensitivity to time intervals compared to pulse widths in millisecond ranges.

Interestingly, the augmentation of I_{ds} exhibited a transition from a linear learning curve to a sigmoidal one, depending on pulse width, amplitude, and time interval. This phenomenon is shown in Figure 3d and bears significance as it is frequently used as an activation function of artificial neurons due to its continuous differentiability, making it beneficial for gradient-based optimization algorithms, such as backpropagation.[34]

Based on the conducted analysis, it was observed that the fabricated neuromorphic transistors demonstrated enhanced potentiation in the *p*-type region under specific conditions. Particularly, higher levels of potentiation were noted in correlation with increased applied voltages, broader pulse widths, and reduced intervals between subsequent pulses.

Short-term potentiation in the n*-type region*

The transfer characteristics of neurotransistors have demonstrated that hole conduction surpasses electron conduction. The subthreshold slope in the *n*-type region is higher, adversely affecting the behavior of STP by lowering learning rates. It was necessary to apply a positive resetting pulse (10 V) due to depolarization to the hole conduction region that occurred when no gate voltage was applied (see "Materials and methods" section).

To examine the impact of various pulse amplitudes, pulses with a width and interval of 100 ms, corresponding to a frequency of 5 Hz, were employed. The analysis results depicted in **Figure** 4a unveiled that, akin to the *p*-type region, higher pulse amplitudes in the *n*-type region led to a greater increase in I_{ds}. However, we observed that the dependence of the learning rate on voltage changes was less pronounced in the *n*-type region. Moreover, we discovered that higher voltages were necessary to induce significant alterations in learning rate, which is suboptimal due to increased energy consumption. This drawback poses challenges for ambipolar behavior when different voltages are utilized for the *p*-type and *n*-type regions, as well as for neuromorphic computing, owing to heightened energy requirements.

To evaluate the impact of different pulse widths, we maintained a fixed time interval of 100 ms and a pulse amplitude of 10 V. Our analysis of Figure 4b revealed that, similar to the *p*-type region, longer pulse widths resulted in increased potentiation. Although the curves corresponding to 0.05 s and 0.1 s seem to be flipped, we must consider that they do not start from exactly the same initial current level. Due to the ambipolar nature of CNT-FETs, the OFF state is found in a very narrow voltage level, and the initial state of each FET can be slightly different. For the case of 0.1-s pulse width, a slight current decrease is observed instead of potentiation. We attribute this to an initial FET condition of opposite polarity (hole conduction), needing 10 s of the erasing process (resetting) until the OFF state is completely reached to start a potentiation process in the *n*-conduction branch by accumulating electrons. This is not observed in the plot corresponding to 0.05-s pulse width, which starts to potentiate directly. However, the slope and therefore the potentiation rate is higher for the 0.1-s pulse width compared to 0.05 s width. Additionally, to investigate the influence of varying time intervals between subsequent pulses, we kept a constant pulse width of 100 ms and a pulse amplitude of 10 V. The measurements presented in Figure 4c demonstrated that the time intervals had minimal effect on potentiation in the *n*-type region. However, we observed that the neurotransistor was unable to sustain 10-ms time intervals, unlike the *p*-type region. This discrepancy could be attributed to the faster relaxation rate of negatively held polarization in the sol–gel-derived gate material within the *n*-type region. Notably, our findings indicate that in the *n*-type region, the presynaptic STDP of STP behavior exhibited greater sensitivity to pulse widths compared to time intervals, contrary to the observations in the *p*-type region. This can be attributed to the different drift and diffusion times of the positive and negative ions in the sol–gel.

The conducted analysis revealed that neurotransistors exhibit higher potentiation in the *n*-type region of ambipolar transistors under specific conditions, such as higher applied voltage levels and wider pulse widths. However, learning behavior demonstrated lower sensitivity to time intervals. It is important to note that no discernible transition to sigmoidal learning behavior was observed (Figure 4d). Additionally, the learning rate was lower in all cases when compared to the *p*-type region.

Forgetting and erasing in the p*-type region*

For the forgetting, we first generated a learning curve, followed by a period of pulse absence. Various negative pulse amplitudes were utilized while keeping the pulse width and the time interval constant at 100 ms. After 100 pulses, only I_{ds} was measured without applying any gate potential. The results (**Figure 5**a) demonstrate that a higher degree of potentiation correlates with a longer duration for potentiation to be forgotten. The forgetting rate is initially rapid until it reaches a baseline where the current potentiation exhibits a sigmoidal change. Subsequently, it slows down significantly. Consequently, complete forgetting could take several minutes to hours, while forgetting up to a threshold of less than 50% could occur within seconds. However, in none of the cases, does the signal return to the original value. We attribute this to the fact that the CNT-FET is not in the OFF state when no gate voltage is applied and a gate voltage is required to set it off. This phenomenon could be due to the remnant polarization within the silicate gate material that is characterized by the random distribution of ions and defects or the charge trapping caused by CNTs. On the contrary, when positive pulses of 6 V with a pulse width of 100 ms were applied, a much faster short-term depression (STD) was observed, as shown in Figure 5b. Notably, depression can lead to a current level lower than the initial state. Achieving the same relaxed state of the system presents challenges due to the tunable threshold voltage and device ambipolarity, requiring different pulse amplitudes and widths for different polarization levels.

To examine the erasing rates at different erasing voltages, we employed positive gate voltage pulses of various amplitudes with a width and time interval of 100 ms after a learning period. Because it is difficult to achieve exactly the same potentiation level, we compared the erasing voltages by normalizing the I_{ds} values to the maximum potentiation level. The results (Figure 5c) indicate that higher erasing pulse amplitudes correspond to higher erasing rates, similar to the potentiation process. Furthermore, Figure 5d suggests that higher levels of potentiation initially lead to higher erasing rates, followed by slower erase rates after reaching the sigmoidal change baseline.

To investigate the relearning after forgetting behavior, the samples were first subjected to learning pulses, consisting of 100 consecutive pulses with a −6-V amplitude, 100-ms pulse

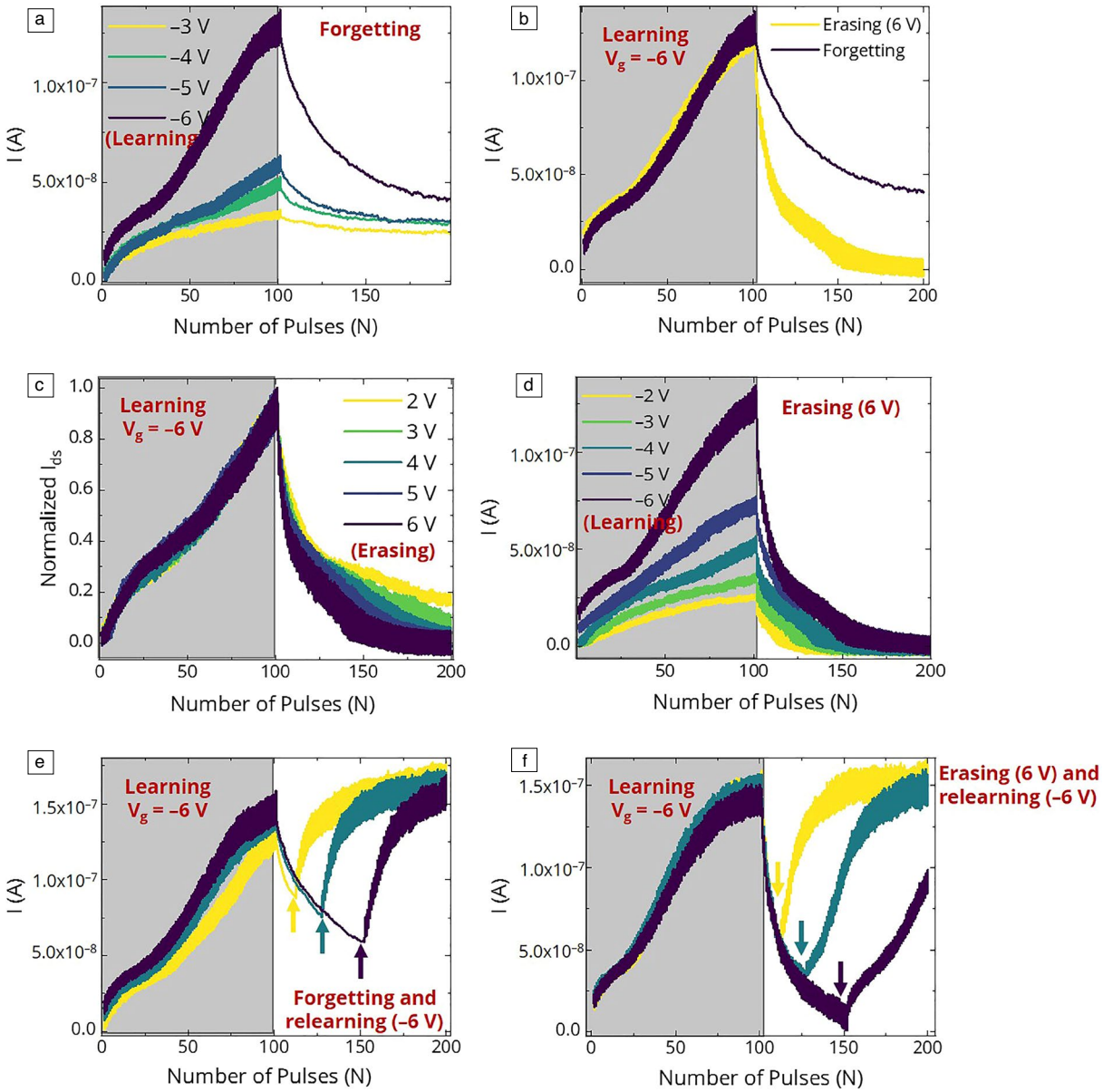

Figure 5. Forgetting and erasing in the *p*-type region of the carbon nanotube field-effect transistor. (a) Short-term potentiation at different gate voltages followed by a forgetting period. (b) Short-term potentiation at −6 V followed by forgetting and erasing (V_g = 6 V). (c) Erasing rates at different erasing gate voltages after a common learning period. (d) Erasing rates at fixed erasing gate voltage (6 V) after different learning processes. (e) Relearning after three different forgetting times (yellow, green, and purple arrows indicate relearning after 2 s, 5 s, and 10 s of forgetting time, respectively). (f) Relearning after three different erasing times (yellow, green, and purple arrows indicate relearning after 2 s, 5 s, and 10 s of forgetting time, respectively).

width, and a fixed 100-ms time interval between subsequent pulses. This was followed by a period of no gate potential to undergo forgetting. Relearning was then initiated after three different forgetting times: 2 s, 5 s, and 10 s (indicated by yellow, green, and purple arrows in Figure 5e, respectively). The results demonstrate that relearning after forgetting occurs at a faster rate (slope) compared to the initial potentiation. After the forgotten information is relearned and reaches a similar current value, the learning rate gradually slows down and returns to normal values.

To assess the effects of erasing on relearning behavior, we conducted experiments involving a sequence of positive 6-V pulses, corresponding to erasing for a specific duration, followed by −6-V pulses with a 100-ms pulse width and time interval for relearning. The impact of erasing duration on the relearning effect was investigated using durations of 2 s, 5 s, and 10 s, as illustrated in Figure 5f. Our results indicate that, due to the rapid erasing rate compared to forgetting, it takes a longer time to recover erased information. Erasing beyond the point where the sigmoidal curve model is exceeded and

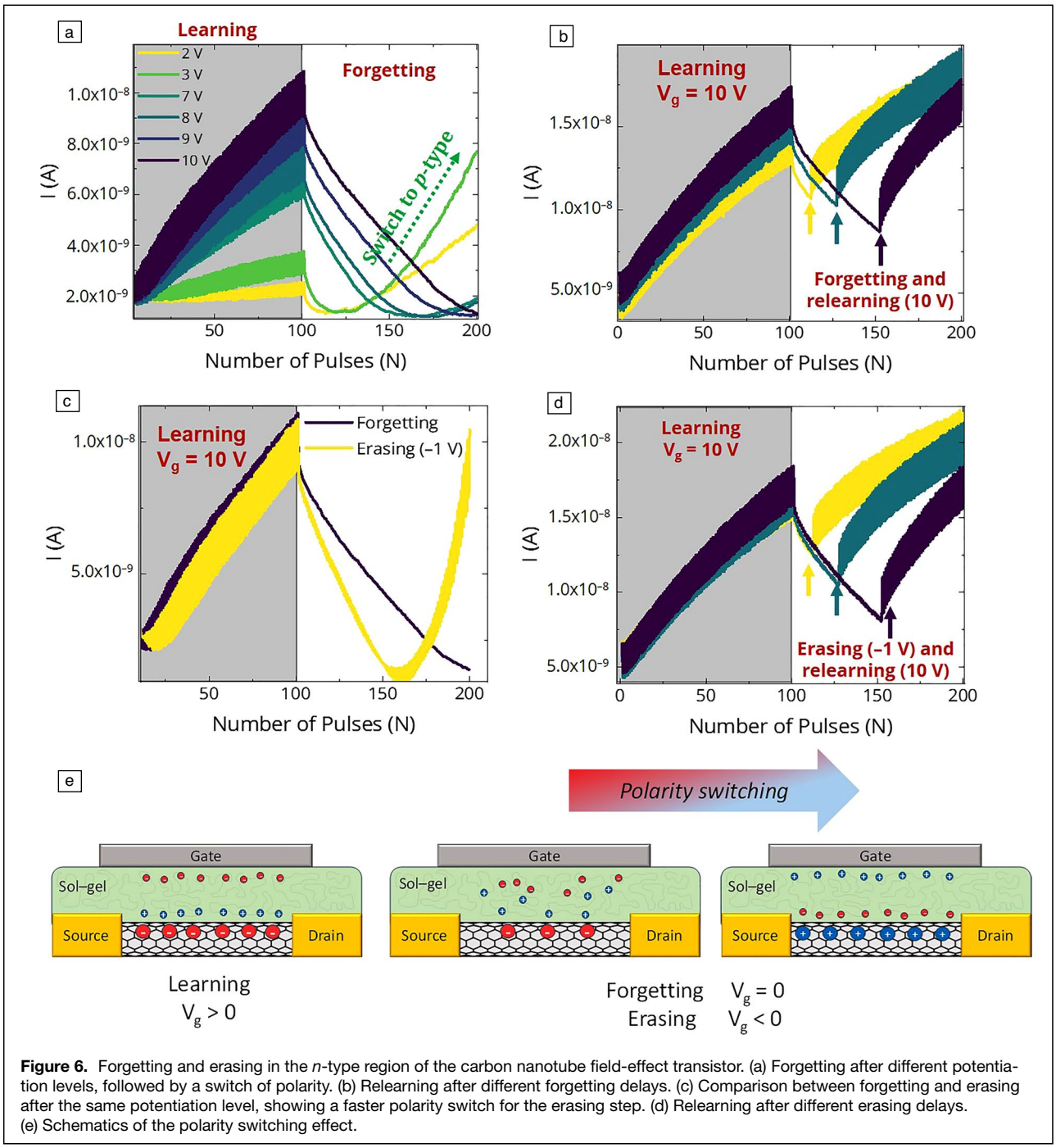

Figure 6. Forgetting and erasing in the *n*-type region of the carbon nanotube field-effect transistor. (a) Forgetting after different potentiation levels, followed by a switch of polarity. (b) Relearning after different forgetting delays. (c) Comparison between forgetting and erasing after the same potentiation level, showing a faster polarity switch for the erasing step. (d) Relearning after different erasing delays. (e) Schematics of the polarity switching effect.

the threshold point is reached poses a significant challenge for the utilization of neurotransistors. Thus, the optimal positive pulse amplitude, pulse width, and interval time must be carefully selected to achieve the desired erasing behavior. In any case, both relearning after forgetting or erasing processes reach a common saturation current level due to the sigmoidal potentiation shape.

Figure S8 reveals that the erasing rate is amplified by wider pulse widths and shorter time intervals between consecutive pulses, mirroring the behavior observed in STP within the *p*-type region. Furthermore, similar to STP, a reduction in pulse width results in an increase in the swing of I_{ds} during erasing, which is attributed to capacitive charging effects.

Forgetting and erasing in the n*-type region*

We explored the forgetting behavior in the *n*-type region of the fabricated neurotransistors by conducting a series of experiments utilizing pulses with varying positive amplitudes. Throughout these experiments, we maintained a consistent

pulse width and time interval of 100 ms. After an initial set of 100 pulses, we focused solely on measuring the I_{ds} current. The results (**Figure 6**a) show a positive correlation between the duration of potentiation and its magnitude. The forgetting rate remained constant in the *n*-type region regardless of the previously utilized learning potential, in stark contrast to the *p*-type region where it exhibited variability. Furthermore, our observations indicate that the learned information can be forgotten to the extent of returning to the baseline. Surprisingly, we also discovered that the neurotransistor can transform into a hole conduction region even in the absence of a gate voltage. We noticed that this inherent switch becomes more prominent at the lowest levels of potentiation (using 2 V or 3 V, as shown in Figure 6a). This intriguing phenomenon suggests the presence of an inherent depolarization effect (Figure 6e), reminiscent of ferroelectric memories.[35] It is this depolarization that can ultimately modify the conduction region of the neurotransistor by the gradual reduction of stored polarization within the gate film and eventually changing to opposite polarization. This can be further supported with Figure 6c in which erasing pulses result in steeper potentiation curve as it would be the case for the operation in *p*-type region. However, this outcome poses a significant challenge for neuromorphic computing, as it could result in the generation of false information if the processes of potentiation, forgetting, and information refreshment are not carefully optimized. Furthermore, following the polarity switch, we observed an abrupt firing, potentially laying the groundwork for an integrate-and-fire model. These findings underscore the importance of optimizing potentiation and forgetting times.

To delve into relearning following forgetting, we subjected the fabricated samples to a series of 100 consecutive pulses with an amplitude of 10 V, a pulse width of 100 ms, and a fixed time interval between subsequent pulses. This initial phase was aimed at achieving potentiation. Subsequently, we proceeded to potentiate the I_{ds} once again after varying time intervals of forgetting (2 s, 5 s, and 10 s). The findings obtained (Figure 6b), vividly demonstrate that relearning after forgetting occurs at an accelerated pace compared to the initial potentiation stage. Notably, akin to the *p*-type region, we observed that longer delays between forgetting and relearning corresponded to swifter relearning in the *n*-type region, albeit not as pronounced as in the *p*-type region. As the forgotten information was relearned, the degree of potentiation gradually diminished, ultimately reverted to its normal values.

To scrutinize the relationship between STD and forgetting in the *n*-type region, we subjected the devices to potentiation during the first 100 positive pulses, and depression during the final 100 pulses, utilizing a pulse amplitude of −1 V, a pulse width of 100 ms, and a time interval of 100 ms. Figure 6c provides a comparative analysis of the STD behavior alongside of forgetting. Our results show that depression occurs faster than forgetting. Moreover, depression has the potential to induce a switch to *p*-type polarity. Furthermore, the earlier onset in the case of erasing in comparison to forgetting suggests that negative voltages during erasing contribute to cumulative depolarization. However, achieving a complete polarization reset poses a significant challenge due to the tunable threshold voltage and ambipolarity of the device.

To explore the erasing rates associated with different erasing voltages and various potentiation levels, we employed pulse widths of 100 ms and time intervals of 100 ms between consecutive pulses. Because it has proven difficult to achieve exactly the same potentiation level, we compared the erasing voltages by normalizing the I_{ds} values against the maximum potentiation level. The results presented in Figure S9a indicate that higher pulse amplitudes lead to accelerated erasing rates. Furthermore, Figure S9b suggests that higher levels of potentiation do not significantly impact erasing rates. Based on the data presented in Figure S10, it becomes evident that the erasing rate of the neurotransistor is enhanced by large pulse widths, while the time intervals exhibit negligible effects, mirroring the behavior observed in STP in the *n*-type region. Additionally, as observed in STP in the *n*-type region, the extremely short pulse widths and time intervals result in an amplified swing of the I_{ds} during erasing, primarily due to capacitive charging effects.

To evaluate the influence of erasing on relearning, we conducted experiments involving a sequence of −1-V pulses, which would translate to erasing for a specific duration, followed by 100 pulses of 10-V amplitude with a width of 100 ms and a 100-ms time interval. We assessed the impact of 2-s, 5-s, and 10-s delays in relearning (Figure 6d). Our results indicate that relearning after erasing exhibits similar behavior to relearning after forgetting in the *n*-type region.

Conclusion

Neuromorphic computing, a rapidly evolving field that aims at emulating the complex functioning of the human brain, holds tremendous promise for developing highly efficient and scalable computing systems. To further advance this field and overcome the limitations of existing complementary metal oxide semiconductor solutions, it is crucial to explore novel materials and devices. This study focuses on the fabrication of ambipolar neurotransistors utilizing carbon nanotube field-effect transistors coated with solution-based ion-doped sol–gel silicate film as polarizable gate material that mimics the plasticity observed in synapses. Neurotransistors exhibited ambipolar behavior under slow voltage sweeping speeds, resulting in reduced electron conduction. The study also investigated the learning, forgetting, and erasing behavior of the device, demonstrating short-term depression and short-term potentiation in both the *n*-type and *p*-type regions. Our findings reveal that the *p*-type region exhibited a high ON/OFF ratio, high erasing rate, high learning rate, and easily adjustable parameters. Despite the device's slow switching speeds, its ambipolar behavior and short-term characteristics set it apart from other novel devices. In contrast, the *n*-type region of the neurotransistor exhibited a low ON/OFF ratio, low learning rate, tunability, and unstable polarization during

erasing and forgetting, making it suboptimal for neuromorphic applications. However, the polarity switch can be the base for integrate-and-fire models that bring new functionalities to the device upon further investigation.

Various fabrication techniques were explored to improve device behavior, focusing on varying baking temperatures, air plasma treatments, proportions in precursor ingredients, or the addition of passivation layers. These led to the formation of defective sol–gels or loss of ambipolar characteristics. Consequently, it is necessary to investigate various sol–gel protocols to enhance the adhesion and formation of thinner films with better gate coupling without compromising the memory effects, originating from hysteretic transfer characteristics. Additionally, improvement of ambipolar behavior can be achieved by employing less defective carbon nanotubes. Alternatively, exploration of reconfigurable FETs, such as those utilizing bottom-up silicon nanowires as semiconductors,[36] could be pursued to avoid uncontrolled polarity switching during forgetting and erasing.

The short-term behavior of the device holds promise for adaptable machine learning applications that require real-time data processing. Gas sensing is an example of a suitable application for this neurotransistor. FET-type gas sensors, known for their compact size, ease of integration, and multifunctionality, have gained significant attention.[19] CNTs have also demonstrated ultrasensitivity for gas-sensing applications.[19] The combination of carbon nanomaterial-based electronics and machine learning techniques with the requirement to process large amounts of data is an important point of attention in current gas-sensing research.[37,38] Ambipolar neuromorphic transistors based on carbon nanotube FETs offer unique advantages over traditional unipolar transistors, making them promising candidates for gas sensing. Their ability to involve two types of charge carriers would enable highly selective sensing, leading to improved discrimination between different gases. They can react double to various gases according to their oxidative or reductive properties, such as NO_2, NH_3, H_2S, and SO_2.[39] The excellent compatibility of CNTs with functional materials can further enhance the sensitivity of these sensors, resulting in improved gas detection and signal amplification. Additionally, neuromorphic properties provide simultaneous sensing, storage, and processing capabilities.[40]

Materials and methods

Fabrication of CNT-FETs

The source and drain electrodes were fabricated following a standard photolithography process and thermal evaporation of Au with a chromium adhesion layer on a silicon wafer with 500-nm oxide layer. First, the samples were put in a sonication bath in acetone for 5 min, followed by a sonication bath in isopropanol for 5 min and then rinsed with de-ionized water. After that, the samples were dried under a stream of nitrogen. Next, a layer of TI Prime was used as an adhesion promoter followed by spin coating of the AZ5214E Image Reversal photoresist (MicroChemicals GmbH, Germany) using an RC8 coater (Karl Süss, Germany) at 4000 rpm for 40 s to achieve a thickness of 1.5 µm. The samples were baked at 110°C for 60 s. Then, contact lithography UV exposure was performed after chip alignment for 2.5 s. After that, the samples were subjected to photoresist development in an AZ726 MIF developer for 60 s and cleaned with de-ionized water for 1 min. Subsequently, a 5-nm Cr adhesion layer was evaporated onto the substrate, followed by 50 nm of Au using physical vapor deposition. The chip was then submerged in acetone and placed on a shaker for 15–20 min for liftoff. Finally, the samples were rinsed with acetone, isopropanol, and de-ionized water. The resultant electrode had a channel length of 20 µm and a width of 100 µm.

Deposition of CNTs was done by the AC dielectrophoresis (DEP) process. Sc-SWCNTs were obtained with diameters ranging from 1.2 to 1.7 nm and lengths up to 4 µm from Sigma-Aldrich (Darmstadt, Germany). To disperse 0.2 mg of sc-SWCNTs in 12.5 mL *N*-methyl pyrrolidone (NMP), tip sonication was used for 2 h at 30% total power in an ice bath, followed by a 1:4 dilution in NMP and resonication for 10 min under the same conditions. To remove nanotube agglomerations and titanium oxide particles that could have been generated during the sonication process, the resulting dispersion was centrifuged for 30 min at 15,000 rpm using a Universal 320 (Hettich, Tuttlingen, Germany). A drop of 100 µL of sc-SWCNT solution was deposited onto the electrode region of the substrates and an AC voltage of 10 V peak to peak at a frequency of 30 Hz was applied for 1 min using a Sony-Tektronix AFG320 function generator to the drain-source electrodes while monitoring signals with a Tektronix TDS3014B oscilloscope. The remaining solution was rinsed with de-ionized water and then dried using a nitrogen gun.

To minimize the interaction between the drain and source electrodes and the gate electrode, SU8-5-negative epoxy photoresist was used. The SU8-5-negative epoxy photoresist was spin-coated at 3000 rpm for 30 s to achieve a thickness of 5 µm. The samples were then baked at 65°C for 2 min and at 95°C for 5 min. Then, contact lithography UV exposure was performed for 5 s. The samples were then baked at 65°C for 1 min and at 95°C for 2 min. Next, the samples were subjected to photoresist development in a mr600 developer for 2 min and cleaned with isopropanol. Finally, the samples were hard-baked at 110°C for 1 h.

Preparation of sol–gel-based silicate film and top-gate electrode

The sol–gel was deposited following a protocol reported in our previous work.[12] The next protocol was followed for 2-µm ion-doped sol–gel silicate film deposition. First, 2.4 mg of nickel(II) chloride hexahydrate ($Cl_2Ni{\cdot}6H_2O$) and 1.7 mg of copper(II) chloride dihydrate ($Cl_2Cu{\cdot}2H_2O$) were dissolved in 467 µL of de-ionized water. Then, 600 µL of trimethoxymethylsilane (MTMS) and 900 µL of tetramethyl orthosilicate (TMOS) precursors were added to the metal salt solution. Next, 33 µL of

0.1-M hydrochloric acid (HCl) was added to lower the pH of the reaction. The glass vial containing the "sol" was vortexed for 2 min and then placed in an ultrasonic bath for 10 min. "Sol" was then passed through a 200-nm pore size filter to remove large particles. The next protocol was followed for 234-nm ion-doped sol–gel silicate film deposition. First, 4.38 mg of nickel(II) chloride hexahydrate and 3.1 mg of copper(II) chloride dihydrate were dissolved in 100 µL of de-ionized water. Then, 100 µL of MTMS and 240 µL of TMOS precursors were added to the metal salt solution. Next, 33 µL of 0.1-M HCl was added to lower the pH of the reaction. The glass vial containing the "sol" was vortexed for 2 min and then placed in an ultrasonic bath for 10 min. "Sol" was aged for 6 h and then passed through a 200-nm pore size filter to remove large particles.

The next protocol was followed to deposit the sol–gel. CNT-FETs were first cleaned in acetone sonication bath for 2 min, then in isopropanol sonication bath for 2 min, and then rinsed with de-ionized water and dried using a nitrogen gun. After that, they were annealed at 120°C for 10 min to remove any residual solvent or water.[41] Then, 100-W air plasma cleaning was applied for 2 s to remove smaller organics and reduce the contact angle, hence enhancing the surface hydrophilicity for sol adhesion. Next, 300 µL of the filtered sol was spin-coated on a 1 cm × 1 cm electrode area of the cleaned chip at 7000 rpm for 60 s. The sol-coated chip was dried in a vacuum oven under 100°C for 24 h to get a uniform gel formation. Finally, a 70-nm top-gate electrode laser of silver was evaporated onto the substrate through a shadow mask using physical vapor deposition.

Measurement setup

Measurements were conducted using MATLAB 2016B (Mathworks) software and a Keithley 2604B Source Measurement Unit (SMU). To generate the transfer curves, gate voltages were swept at varying speeds, spanning from 0 to 10 V and subsequently transitioning to −10 V before returning to the initial voltage of 0 V applying a constant V_{SD} of 100 mV. In order to evaluate the effects of erasing (depression), learning (potentiation), and forgetting, different pulse schemes with varying frequencies and amplitudes were employed. Measurements were done at the end of each pulse. A positive 10-V reset voltage was applied again to show the memory effects on the electron conduction polarity of the sol–gel-modified CNT-FETs, but the input polarities of the pulses were changed.

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Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of interest

The authors have no conflicts of interest to disclose.

Supplementary information

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