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Mit dem Thema

Fabrication, characterization and application of $Si_{1-x-y}Ge_xSn_y$ alloys

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I. Table of contents

II. Abstract

The aim of this thesis is the evaluation of tin (Sn)-containing group IV semiconductor alloys like germanium-tin (GeSn) and silicon-germanium-tin (SiGeSn) as future high-performance semiconductor materials for integrated circuits (ICs). The following questions arise: Is it possible to fabricate these thermodynamic metastable alloys in a high crystalline quality to achieve outstanding electron and hole mobilities? Can post-growth thermal treatments at high temperatures for a few nanoseconds or milliseconds improve the crystal quality? Is it possible to fabricate GeSn and SiGeSn ICs with state-of-the-art silicon-based process steps, and how do they perform? In this context, it is relevant to know the portion of Sn and dopant atoms on the regular lattice sites and if the thermal treatments result in chemical redistribution processes, activation/deactivation of dopants, or the formation of segregations. To answer these questions, GeSn and SiGeSn alloys are produced by epitaxial growth or ion beam implantation followed by short-term thermal treatments or a combination of both. The influence of thermal treatments on the crystal structure is investigated using high-resolution examination methods such as transmission electron microscopy, X-ray diffraction, secondary ion mass spectroscopy, positron annihilation spectroscopy, or Rutherford backscattering spectrometry. The results show that the manufacturing process strongly influences the GeSn and SiGeSn material quality and that thermal treatments can only improve the crystal structure under certain circumstances. Depending on the thermal treatment conditions, different physical effects occur, such as elastic strain relaxation, merging many single-vacancies into a few larger vacancy clusters, and additional activation of dopant atoms. The successful production of SiGeSn using Sn ion beam implantation in silicon-germanium alloys and solid-phase epitaxy is presented for the first time.

Furthermore, so-called “junctionless nanowire” field-effect transistors made of GeSn and SiGeSn are manufactured and characterized in different post-growth thermal treatment states. The fabricated transistors can achieve off-currents close to the measurement sensitivity of <1 fA and on-currents in the µA range. This allows achieving remarkable on/off current ratios of up to 8 orders of magnitude.

III. Kurzfassung (Abstract in German)

Das Ziel der vorliegenden Arbeit ist es zu evaluieren ob Zinn (Sn)-haltige Gruppe IV Halbleiterlegierungen wie Germanium-Zinn (GeSn) und Silizium-Germanium-Zinn (SiGeSn) als zukünftige Hochleistungs-Halbleiter-Materialien für integrierte Schaltkreise (ICs) geeignet sind. Dabei stellen sich folgende Fragen: Können diese thermodynamisch metastabilen einkristallinen Legierungen mit hoher Kristallqualität hergestellt werden um die prognostizierten hohen Elektronen- und Lochbeweglichkeit zu erreichen? Kann die Kristallqualität durch Hochtemperatur-Wärmebehandlungen im Nano- oder Millisekunden Bereich verbessert werden? Können ICs aus GeSn und SiGeSn mit industrienahen Silizium-basierten Prozessschritten hergestellt werden und welche Eigenschaften besitzen diese ICs? In diesem Zusammenhang ist es relevant wie hoch der Anteil von Sn- und Dotieratomen auf den regulären Kristallgitterplätzen ist und ob es durch die Wärmebehandlung zu chemischen Umverteilungsprozessen, Aktivierung/Deaktivierung von Dopanden oder zur Bildung von Ausscheidungen kommt. Um diese Fragestellungen zu beantworten werden GeSn und SiGeSn Legierungen mit Molekularstrahlepitaxie oder Ionenimplantation gefolgt von Kurzzeit-Wärmebehandlungen oder einer Kombination aus beiden Herstellungsverfahren hergestellt. Der Einfluss der Wärmebehandlungen auf die Kristallstruktur wird mittels hochauflösenden Untersuchungsmethoden wie zum Beispiel Transmissionselektronenmikroskopie, Röntgendiffraktometrie, Sekundärionen-Massenspektroskopie, Positron-Annihilations-Spektroskopie oder Rutherford-Rückstreu-Spektrometrie untersucht. Die Ergebnisse zeigen, dass die GeSn und SiGeSn Materialqualität stark vom Herstellungsprozess beeinflusst wird und die Kristallstruktur durch die Wärmebehandlung nur unter bestimmten Umständen verbessert werden kann. In Abhängigkeit der Wärmebehandlungsbedingungen treten unterschiedliche Prozesse auf, wie der Abbau von elastischen Eigenspannungen, der Zusammenschluss von vielen Einzelleerstellen zu wenigen größeren Leerstellenclustern und eine zusätzliche Aktivierung von Dotieratomen. Ebenfalls wird erstmalig die erfolgreiche Herstellung von SiGeSn mittels Sn Ionenimplantation in Silizium-Germanium Legierungen und Festphasenepitaxie präsentiert. Darüberhinaus werden sogenannte “Junctionless Nanowire“ Feldeffekttransistoren aus GeSn und SiGeSn in unterschiedlichen Wärmebehandlungszuständen hergestellt und charakterisiert. Die hergestellten Transistoren können sowohl Aus-Ströme nahe der Messsensitivität von <1 fA als auch An-Ströme von im µA Bereich erreichen, weshalb bemerkenswerte An-/Aus-Strom-Verhältnisse von bis zu 8 Größenordnungen erreicht werden können.

IV. List of Abbreviations

Abbreviation	Meaning
AFM	**A**tomic **f**orce **m**icroscope
Al	Element **al**uminum
ALD	**A**tomic **l**ayer **d**eposition
Ar	Element **ar**gon
As	Element **ar****s**enic
ATSUP	**At**omic **sup**erposition (simulation method)
ATT	**A**dvanced **t**emperature **t**est system
Au	Element gold (lat. **au**rum)
a-Ge	**a**morphous **ge**rmanium
B	Element **b**oron
BCl_2	Di**ch**lor**o****b**orane (RIE etch gas)
Bi	Element **bi**smuth
BESOI	**B**ond and **e**tch **b**ack **s**ilicon **o**n **i**nsulator
BG	**B**and-**g**ap
BN	**B**oron **n**itride
BOX	**B**uried **ox**ide
BSE	**B**ack-**s**catter **e**lectron detector
C	Element **c**arbon
C_4F_8	Octaflurocyclobutane
CB	**C**onduction **b**and
CCD	**C**harge-**c**oupled **d**evice
Cl	Element **c**h**l**orine
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
$CrBr_3$	**C**h**r**omium **br**omide
Cs^+	Positively charged **ce****s**ium ion
Cu	Element copper (lat. **cu**prum)
CV	**C**apacitance-**v**oltage
CVD	**C**hemical **v**apor **d**eposition
Γ	**Γ**-point (center of the Wiegner-Seitz cell) in a crystal
D	**D**euterium
DB-VEPAS	**D**oppler **b**roadening **v**ariable **e**nergy **p**ositron **a**nnihilation **s**pectroscopy
DC	**D**irect **c**urrent
DI	**D**eion**i**zed water

DIBL	**D**rain-**i**nduced **b**arrier **l**owering
e^+	Positrons (positive elementary particle with the positive charge of an e^-)
e^-	**E**lectron (negative carrier type)
EBL	**E**lectron **b**eam **l**ithography
ECV	**E**lectrochemical **c**apacitance-**v**oltage measurement
EDXS	**E**nergy-**d**ispersive **X**-ray **s**pectroscopy
EHT	**E**lectron **h**igh-**t**ension
ELBE	**E**lectron **l**inac for beams with high **b**rilliance and low **e**mittance
et al.	And others
EOT	**E**quivalent **o**xide **t**hickness
F	Element **f**luorine
FFT	**F**ast **F**ourier **t**ransform
FLA	**F**lash **l**amp **a**nnealing
FET	**F**ield **e**ffect **t**ransistor
FWHM	**F**ull **w**idth at **h**alf **m**aximum
f-FLA	**F**ront side **f**lash **l**amp **a**nnealing
Ga	Element **ga**llium
GAA	**G**ate-**a**ll-**a**round (transistor configuration)
GaAs	III-V semiconductor alloy of the element **ga**llium and **ar**s**e**nide
GC	**G**radient-**c**orrection
Ge	Element **ge**rmanium
GeOI	**Ge** **o**n **i**nsulator
$Ge_{1-x}Sn_x$	**Ge**rmanium-tin (**Sn**) alloy with variable Sn concentration
GeSnOI	$\mathbf{Ge}_{1-x}\mathbf{Sn}_x$ alloy **o**n **i**nsulator
GI	**G**razing **i**ncidence (XRD measurement method)
GmbH	Private limited liability company (german. **G**esellschaft **m**it **b**eschränkter **H**aftung)
H	Element **h**ydrogen
h^+	**H**ole (positive carrier type)
HAADF-STEM	**H**igh-**a**ngle **a**nnular **d**ark-**f**ield – **s**canning **t**ransmission **e**lectron **M**icroscope
He	Element **he**lium
HCl	**H**ydro**c**h**l**oric acid
HF	**H**ydro**f**luoric acid
HH	**H**eavy **h**oles (holes with a higher effective mass)
HR-TEM	**H**igh-**r**esolution - **t**ransmission **e**lectron **m**icroscopy

HR-XRD	**H**igh-**r**esolution – **X**-**r**ay **d**iffraction
HSQ	**H**ydrogen **s**ilses**q**uioxane (EBL resist)
HZDR	**H**elmholtz-**Z**entrum **D**resden-**R**ossendorf
IC	**I**ntegrated **c**ircuits
ICDD	**I**nternational **c**entre for **d**iffraction **d**ata
ICP-RIE	**I**nductive **c**oupled **p**lasma **r**eactive **i**on **e**tching
ICSD	**I**norganic **c**rystal **s**tructure **d**atabase
IFW	Leibniz **I**nstitut für **F**estkörper- und **W**erkstoffforschung Dresden
IHP	Leibniz **I**nstitute for **H**igh **P**erformance Microelectronics
InGaAs	**In**dium **ga**llium **ar**senide
IPA	**I**so**p**ropyl **a**lcohol or **i**so**p**ropanol
JLFET	**J**unction**l**ess **f**ield-**e**ffect **t**ransistors
JNT	**J**unctionless **n**anowire **t**ransistor
L	Intersection point with crystallographic [111] direction
LT-PR	**L**ow-**t**emperature **p**hoto-**r**eflectance spectroscopy
LH	**L**ight **h**oles (holes with a lower effective mass)
LO	**L**ongitudinal **o**ptical (related to phonon vibration modes)
Mag.	**Mag**nification of a microscope
MBE	**M**olecular **b**eam **e**pitaxy
MePS	**M**ono-**e**nergetic **p**ositron **s**pectroscopy
MIBK	**M**ethyl **i**so**b**utyl **k**etone
MOS	**M**etal-**o**xide-**s**emiconductor
MOSFET	**M**etal-**o**xide-**s**emiconductor **f**ield-**e**ffect **t**ransistor
N	Element **n**itrogen
NanoFaRo	**Nano**fabrication **fa**cility in **Ro**ssendorf
Nd:YAG	**N**eo**d**ymium-doped **y**ttrium **a**luminum **g**arnet
NH_4HF_2	Ammonium bifluriede
Ni	Element **ni**ckel
NMOS	**N**-type **m**etal-**o**xide-**s**emiconductor
O	Element **o**xygen
P	Element **p**hosphor
PALS	**P**ositron **a**nnihilation **l**ifetime **s**pectroscopy
PAS	**P**ositron **a**nnihilation **s**pectroscopy
Pb	Element lead (lat. **p**lum**b**um)
PbS	Lead (lat. **p**lum**b**um) **s**ulfide
PECVD	**P**lasma **e**nhanced **c**hemical **v**apor **d**eposition

PDF	**P**owder **d**iffraction **f**ile
PL	**P**hoto**l**uminescence
PLA	**P**ulsed **l**aser **a**nnealing ($T<T_m$)
PLM	**P**ulsed **l**aser **m**elting ($T>T_m$)
PMOS	**P**-type **m**etal-**o**xide **s**emiconductor
PMMA	**P**oly-**m**ethyl-**m**eth-**a**crylate
PMT	**P**hoto**m**ultiplier **t**ube (type of detector)
PR	**P**hoto-**r**eflectance spectroscopy
Pt	Element **p**la**t**inum
RBS	**R**utherford **b**ackscattering **s**pectrometry
RBS-C	RBS aligned in a specific **c**hanneling C direction
RBS-R	RBS without a designated (**r**andom R) direction by changing the sample orientation during the RBS measurement
RF	**R**adio **f**requency
RIE	**R**eactive **i**on **e**tching
RSM	**R**eciprocal **s**pace **m**ap
RTA	**R**apid **t**hermal **a**nnealing
r-FLA	**R**ear side **f**lash **l**amp **a**nnealing
SF_6	**S**ulphur-hexa-**f**luoride
Sn	Element tin (lat. **s**tan**n**um)
Sn_{Ge}	**Sn** located on **Ge** lattice sites
α-Sn	Allotrope form of **Sn** with the trivial name gray tin
β-Sn	Allotrope form of **Sn** with the trivial name white tin
SEM	**S**canning **e**lectron **m**icroscopy
Si	Element **si**licon
SIMS	**S**econdary-**i**on **m**ass **s**pectrometry
SIMOX	**S**eparation by **im**planted **ox**ygen
SRIM	**S**topping and **r**ange of **i**ons in **m**atter (simulation software)
SiN_x	**Si**licon **n**itride with a varying stoichiometry
$Si_{1-x-y}Ge_ySn_x$	**Si**licon-**ge**rmanium-tin(**Sn**) alloy with variable Ge and Sn concentrations
SO	**S**plit-**o**ff band
TEM	**T**ransmission **e**lectron **m**icroscopy
TG	**T**op-**g**ate
TMDC	**T**ransition-**m**etal **d**ichal**c**ogenides
TMA	**T**ri**m**ethyl**a**luminum (ALD precursor)
TMAH	**T**etra-**m**ethyl-**a**mmonium **h**ydroxide

TO	**T**ransverse **o**ptical (related to phonon vibration modes)
ToF-SIMS	**T**ime **o**f **f**light **s**econdary-**i**on **m**ass **s**pectrometry
TRIM	**T**ransport and **r**ange of **i**ons in **m**atter (Part of SRIM code)
V	**V**acancy
V_{Ge}	**V**acancy on **Ge** site
V_{2Ge}	Double **v**acancy on **G**e site
VASE	**V**ariable **a**ngle **s**pectroscopic **e**llipsometry
VB	**V**alence **b**and
VEPAS	**V**ariable **e**nergy **p**ositron **a**nnihilation **s**pectroscopy
VS	**V**irtual **s**ubstrate
W	Element tungsten (German **W**olfram)
w/o	**W**ith**o**ut
X	Intersection point with crystallographic [100] direction
Xe	Element **xe**non
XeCl	Molecule of **xe**non and **c**h**l**orine
XRD	**X**-**r**ay **D**iffraction
X-ray	Roentgen (**X**) **ray**s
ZED	Brand name of the ZEP developer n-amyl acetate
ZEP	Brand name of an EBL resist
0D	Zero **d**imensional
1D	One **d**imensional
2D	Two **d**imensional

V. List of Symbols

Symbol	Meaning	Unit
A	Area	m^2
A_C	Mathematical integrated area under RBS-C curve	-
A_H	Hall-coefficient	$m^3\ C^{-1}$
A_R	Mathematical integrated area under RBS-R curve	-
A_λ	Absorption coefficient	-
$\overline{A_\lambda}$	Average absorption of light	-
A	Lattice parameter	Å
a_{II}	In-plane-lattice parameter	Å
$a_\perp$	Out-of-plane lattice parameter	Å
B	Magnetic flux density	T
b_d	Disorder parameter for phonon modes	-
b_ε	Strain coefficient for phonon modes	-
C_D	Depletion capacitance of the gate	F
C_{it}	Interface trap capacitance	F
C_j	Amplitude of the photo-reflectance resonance	-
C_{ox}	Oxide capacitance	F
C_p	Heat capacity at constant pressure	$J\ kg^{-1}\ K^{-1}$
C_{11}	Cubic elastic constant of the elasticity matrix	GPa
C_{12}	Cubic elastic constant of the elasticity matrix	GPa
C_{13}	Cubic elastic constant of the elasticity matrix	GPa
C_{33}	Cubic elastic constant of the elasticity matrix	GPa
C_{44}	Cubic elastic constant of the elasticity matrix	GPa
C	Concentration	at.%
c_D	Dopant concentration	$Atoms\ cm^{-3}$
c_v	Vacancy defect concentration	$Atom^{-1}$
$D(t)$	Time-dependent positron lifetime spectra	$Counts\ ns^{-1}$
D_I	Implantation dose	$Ions\ cm^{-2}$
D_+	Positron diffusion coefficient	$cm^2\ s^{-1}$
D	Thickness or depth	nm
$<d>$	Positron annihilation depth (approximation)	nm
d_c	Critical thickness	nm
$d_{c,epi}$	Critical thickness for epitaxial break down during growth	nm

$d_{c,relax}$	Critical thickness for strain relaxation during growth	nm
d_{NW}	Vertical nanowire thickness	nm
d_{ox}	Oxide thickness	nm
E	Energy	keV
E_0	Energy of the incident He^+ beam	keV
E_1	Detected He^+ energy	keV
E_b	Binding energy	eV
E_{Bg}	Band-gap energy	eV
E_{CB}	Minimum conduction band energy	eV
E_d	Energy density	J cm^{-2}
E_F	Fermi level energy	eV
E_{FI}	Intrinsic Fermi level energy	eV
E_j	Energy of optical transition	eV
E_p	Energy of positrons	eV
E_{VB}	Maximum valence band energy	eV
F	Frequency	Hz
g_r	Growth rate	nm s^{-1}
g_m	Transconductance	S
H	Planck´s constant = 4.1356676969 x 10^{-15}	eV s
I	Intensity	counts
I_{DS}	Drain-source current	A
I_H	Current for Hall-effect measurements	A
I_{max}	Maximum drain-source current in accumulation mode	A
I_{off}	Minimum drain-source current	A
I_{on}	Drain-source current at the flat-band voltage	A
$i´$	Imaginary unit	-
K	Thermal conductivity	W m^{-1} K^{-1}
K	Slope coefficient of a linear curve	-
k_b	Boltzmann constant = 1.38064852 x 10^{-23}	m^2 kg s^{-2} K^{-1}
L	Length/distance	nm
$L_{eff,acc}$	Effective length of the of the accumulation channel	nm
$L_{eff,b}$	Effective length of the of the neutral bulk channel	nm
L_{NW}	Nanowire length	nm
L_+	Positron diffusion length	nm
M	Mass	kg
m_{eff}	Effective mass of carriers	kg

N	Natural number	-
N_D	Total atom concentration	Atoms
N_r	Number of photo-reflectance resonances	-
N_t	Total number of atoms per cubic centimeter	Atoms cm^{-3}
N	Wavenumber	cm^{-1}
n_{e-}	Sheet electron carrier concentration	cm^{-3}
n_{h+}	Sheet hole carrier concentration	cm^{-3}
n_I	Implanted ions per depth	Ions cm^{-1}
Q	Reciprocal scattering vector	nm^{-1}
Q	Elementary charge = 1.602176634 x 10^{-19} C	C
q_x	In-plane component [110] of the scattering vector Q	nm^{-1}
q_z	Out-of-plane component [001] of the scattering vector Q	nm^{-1}
R	Optical reflectance	%
Re	Real part of a complex number	-
RMS	Root-mean-square roughness	nm
R^2	Coefficient of determination	-
R_p	Projected range for implanted ions	nm
R_s	Sheet resistance	$\Omega\ cm^{-2}$
R_λ	Reflection coefficient	-
S	Annihilation line parameter (low electron momentum fraction; valence electron)	-
S_{max}	Cross-section of the channel when the sufface is accumulated	nm
SS	Subthreshold swing	mV per decade of current
SS^{-1}	Subthreshold slope	decade of current per mV
S_λ	Spectrum of the FLA lamp	nm
T	Temperature	K or °C
T_m	Melting temperature	K
T_p	Peak temperature during short-time thermal treatments	K
T_S	Substrate temperature	°C
T_λ	Transmission coefficient	-
T	Time	s
V	Volume	cm^3
V_{BG}	Back-gate voltage	V

V_D	Drain voltage	V
V_{DS}	Potential between drain and source	V
V_{Fb}	Flat-band voltage	V
V_G	Gate voltage	V
V_{Ge}	Vacancy on a germanium lattice site	-
V_H	Hall-voltage	V
V_S	Source voltage	V
V_{TG}	Top-gate voltage	V
V_{th}	Threshold voltage for JNTs	V
v_V	Specific positron trapping rate (trapping coefficient)	s^{-1}
W	Annihilation line parameter (high electron momentum fraction; core electrons)	-
W_{eff}	Channel perimeter	nm
W_{NW}	Nanowire width	nm
W_{TG}	Top-gate width	nm
X	Elemental fraction of Sn	at.%
Y	Elemental fraction of Ge	at.%
Z	Elemental fraction of Si	at.%
A	Correction factor	-
B	Exit angle	°
Γ_j	Broadening of the photo-reflectance resonance	eV
Δ	Tilt angle of crystal	°
Δ_{SO}	Spin-orbit split-off energy	eV
$\Delta\rho_j$	Inhomogeneous broadening parameter	eV
$\Delta\omega_p$	Peak shift of the phonon vibration frequency	cm^{-1}
ε_{II}	In-plane biaxial strain	-
ε_r	Dielectric constant	-
θ_j	Phase angle of the photo-reflectance resonance	°
2θ	XRD diffraction angle between ω and detector	°
Λ	Wavelength	nm
μ	Carrier mobility	$cm^2\ Vs^{-1}$
μ_{e-}	Electron mobility	$cm^2\ Vs^{-1}$
$\mu_{e-,acc}$	Electron mobility in the accumulation channel of the JLFET	$cm^2\ Vs^{-1}$
μ_{h+}	Hole mobility	$cm^2\ Vs^{-1}$
Ξ	Incorporation rate of an element in a lattice	at.%

P	Material density	g cm^{-3}
ρ_r	Resistivity	Ω cm
Φ_{Ge}	Flux of Ge	cm^{-2} s^{-1}
Φ_{Sn}	Flux of Sn	cm^{-2} s^{-1}
χ	RBS channeling yield	-
τ	Positron annihilation lifetime	ps
τ_{av}	Average positron annihilation lifetime	ps
τ_B	Positron bulk lifetime	ps
τ_1	First positron annihilation lifetime of component	ps
τ_2	Second positron annihilation lifetime of component	ps
Ψ	Bowing parameter for lattice parameter calculation	-
Ω	Incident angle	°
ω_p	Phonon vibration frequency	cm^{-1}

VI. List of Figures

VII. List of Tables

1 Introduction

Currently, the industriy´s main production lines of integrated circuits (ICs) are still silicon (Si)-based because Si is:

- nearly unlimited available and is relatively inexpensive,
- well investigated for many decades and, therefore, most of the process windows for device fabrication are well known,
- has a stable native oxide, and
- single-crystalline Si-wafers can be fabricated on a large scale with high-quality at a low cost.

However, Si has three main drawbacks. i) The speed of ICs depends on the hole and electron mobility. Unfortunately, Si does not have the highest values of charge carrier mobilities compared to other semiconductor materials (see Table 1 - 1). In the past, researchers found solutions to extend some limits and increase the performance of ICs by applying specific performance boosters, like shrinking the design dimensions down to a few nanometers [1], strain-introduced mobility enhancement via capping layers [2], using isolated substrates like the silicon on insulator (SOI) platform [3, 4] or including novel gate stacks with high-k gate dielectrics [5, 6] and metal gates [5, 7, 8]. For many years, it has been forecasted that these performance boosters would reach their limits soon and, therefore, there is a trend to replace, step by step, Si by germanium (Ge) [9, 10]. ii) The performance of Si degrades at high temperatures, and the high IC integration density with billions of transistors makes heat dissipation problematic. iii) Si is not lasing actively since it has an indirect band-gap (BG), which makes it difficult to integrate electronics and photonics on a single chip.

These reasons make it necessary to either develop novel device concepts, rethink the whole device fabrication process, or find alternative material solutions that can be easily integrated with the existing Si-based technology. These approaches will be discussed in the present thesis. An overview of alternative materials that could replace Si are presented in Table 1 - 1. Even though the values presented in the table are not directly comparable because of different extraction methods, carrier concentrations, layer thicknesses, and simulation assumptions, they give a first overview of the expected properties. Every presented semiconductor type has its inherent advantages and drawbacks, which need to be overcome. Group III-V compound semiconductors like GaAs have a high electron mobility μ_{e^-} and a direct BG. However, their hole mobility μ_{h^+} is even lower than in Si, and the material is not CMOS-compatible [11]. 2D materials like the transition-metal dichalcogenides (TMDC), like MoS_2, have a thickness-dependent

tunable band-gap energy (E_{Bg}), but their carrier mobilities are lower than in bulk Si. Furthermore, conventional doping of monolayer thick TMDCs, for instance, via ion beam implantation, is extremely difficult because of the layer thickness below 1 nm, and the high contact resistivity makes it questionable if this material class can replace Si [12].

Table 1 - 1: Overview of semiconductor materials like GaAs [13, 14], MoS_2 [12, 15-19], Si [20, 21], Ge [20], 3C-SiC [22, 23], $Si_{0.2}Ge_{0.8}$ [Sau, 2007 #77][Ismail, 1994 #258][Kumar, 2023 #259][Lee, 2004 #260], $Ge_{0.92}Sn_{0.08}$ [14, 27-29], and $Si_{0.1}Ge_{0.88}Sn_{0.02}$ [30] with their reported electron μ_{e^-} and hole μ_{h^+} mobilities, band-gap energy E_{Bg}, and their band-gap (BG) type.

Group	Material	μ_{e^-} (cm²/Vs)	μ_{h^+} (cm²/Vs)	E_{Bg} (eV)	BG type
III-V	GaAs	8000 - 9400	300 - 400	1.42	Direct
2D	MoS_2 bulk	200-500	480	1.2	Indirect
	MoS_2 monolayer	0.1 - 80	40	1.8	Direct
IV	Si	1400	480	1.11	Indirect
	Ge	4000	1800	0.66	Indirect
	3C-SiC	700	100	2.3	Indirect
	$Si_{0.2}Ge_{0.8}$	500 - 1000	250 - 1000	0.80	Indirect
	$Ge_{0.92}Sn_{0.08}$	6000	800 - 4500	0.57	Direct
	$Si_{0.1}Ge_{0.88}Sn_{0.02}$	4100	1700	1.02	Indirect

Much more promising materials are the so-called “group IV semiconductors”, which include all elements and alloys of the fourth main group of the periodic table, namely Si, carbon (C), Ge, and tin (Sn). All these elements have four valence electrons, leading to some similarities in their properties and allowing the integration into existing Si-based manufacturing lines. Ge shows higher carrier mobilities ($\mu_{e^-} \approx 4000$ cm²/Vs, $\mu_{h^+} \approx 1800$ cm²/Vs) than Si ($\mu_{e^-} \approx 1400$ cm²/Vs, $\mu_{h^+} \approx 480$ cm²/Vs), but, like Si, it is an indirect BG-semiconductor. Materials with a higher carrier injection velocity and mobility are desired for devices with high-frequency operation [31]. Unfortunately, Ge is more expensive than Si, does not have process-relevant stable native oxides and the lattice mismatch to Si causes strain-introduced issues for the implementation on the Si platform. Nevertheless, Ge on Si found its applications in electronics and photonics [32, 33], and Ge is considered to be a promising active component of many electrical and optical applications [5, 9]. Owing to the possibility of tuning multiple material properties, e.g., μ, E_{Bg}, lattice parameter, strain, oxidation behavior, etc., the first group IV alloys were fabricated at the end of the 20th century. For example, IBM presented the first growth of a $Si_{1-y}Ge_y$ crystal in 1986, and the first high-quality grown SiC single-crystal was presented in 1978 [34]. Nowadays, single-crystalline SiC is available in different stacking sequences (4H-, 6H- or 3C-SiC), and its wide BG ($E_{Bg} \approx 2.3$ eV) makes especially 3C-SiC an important semiconductor for future high-power electronics. $Si_{1-y}Ge_y$ alloys, thanks to higher μ_{h^+} and larger lattice parameters, are widely used as a channel material

for p-type transistors or Si stressors [35, 36]. However, the indirect E_{Bg} in cubic $Si_{1-y}Ge_y$ alloys and their composition-dependent lattice parameter make it difficult to achieve a significant improvement for optical applications [37]. To overcome these issues, the ternary Si-Ge-C system was investigated. However, the limited incorporation (< 2%) on substitutional lattice sites of C in $Si_{1-y}Ge_y$ and their segregation tendency limited the broad implementation [38, 39]. Another relatively young group IV approach is alloying Ge and $Si_{1-y}Ge_y$ with Sn to form $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys. α-Sn is a negative direct BG material that allows effective BG engineering due to alloy formation. This enables the reduction of E_{Bg} and allows the conversion from an indirect BG to a direct BG semiconductor [40-43]. The direct BG makes these alloys attractive for optoelectronic applications like lasers and near-infrared detectors [44-48]. Furthermore, the reduced value of E_{Bg} increases the carrier mobilities, which is desired for nanoelectronics [49-51]. The ternary $Si_{1-x-y}Ge_ySn_x$ alloy has two compositional degrees of freedom, allowing the lattice parameter to be decoupled from the electronic structure. Therefore, the ternary alloy can have E_{Bg} and lattice parameters below and above Ge, depending on the Si/Sn ratio [52]. This opens the field for various applications like stressors, buffer layers, or multi-junction photovoltaics [30, 53, 54]. Finally, $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys offer the possibility of combining optoelectronics and nanoelectronics in a fully CMOS-compatible manner on the same chip.

The second approach, to overcome the scaling issues and simultaneously increase the IC power density of Si-based field-effect transistors (FET), is the application of novel device concepts like so-called “reconfigurable field-effect transistors” (RFET), “tunnel field-effect transistors” (TFET) and “junctionless field-effect transistors” (JLFET) as well as three dimensional stacked lateral or vertical FETs [8]. The schematic of the device architectures is displayed in Fig. 1 - 1. RFETs are transistors with an intrinsic channel, which can be customized as a n- and p-channel transistor by using a programming and control gate (see Fig. 1 - 1 a)) [55]. Hence, a lower total number of transistors can be used for a certain logic operation due to their multi-functionality. TFETs convince with a low power consumption because of their switching via quantum tunneling. The active structure consists of a p-i-n region, as shown in Fig. 1 - 1 b). By controlling the top-gate potential, band-to-band tunneling between the p- and n-regions can be achieved. This can lead to subthreshold swings below 60 mV $dec.^{-1}$ [56] at room temperature, which is the thermodynamic limit for Si metal-oxide-semiconductor field-effect transistors (MOSFETs). JLFETs consist of a homogeneous, highly doped semiconductor source, drain, and channel area and work like resistors (see Fig. 1 - 1 c)). The work function of the top-gate depletes the former highly conductive channel beneath the top-gate, which

turns the JLFET off. Applying an appropriate gate potential opens the channel and turns the device on. This device architecture is immune against doping-introduced short channel effects because it does not contain any junctions and, therefore, allows further device shrinkage [57-59]. Additionally, the fabrication is relatively simple, which helps to reduce the complexity of the whole transistor fabrication process [57, 59].

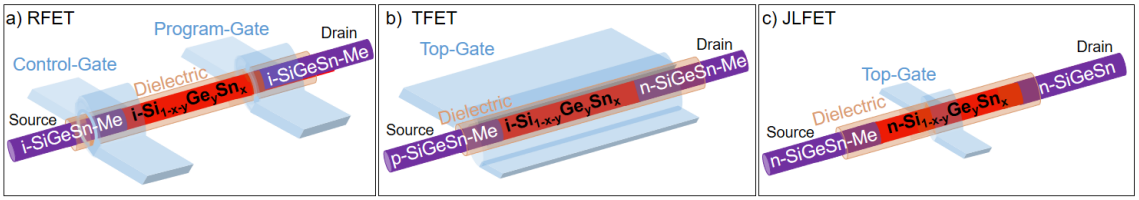


Fig. 1 - 1: Schematic of novel device concepts of reconfigurable field-effect transistors (RFET) a), tunnel field-effect transistors (TFET) b) and junctionless field-effect transistors (JLFET) c) on the example of gate-all-around nanowire structures. The colors represent the top-gate material in blue, the dielectric in orange, the metal (Me)-$Si_{1-x-y}Ge_ySn_x$ source/drain contacts in purple, and the $Si_{1-x-y}Ge_ySn_x$ in red. n-, p- and i- indicate n-type doped (n), p-type doped (p), and intrinsic (i) $Si_{1-x-y}Ge_ySn_x$.

The approach to replace Si as an active component with novel $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ alloys makes it necessary to address alloy-specific challenges like fabrication of single-crystalline high-quality alloys, their thermal stability, and growth-related compressive strain. Following this brief introduction, a general overview of the benefits, challenges, fabrication methods, and thermal treatments for $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys is given in **Chapter 2. Chapter 3** is used to explain the most frequently used experimental setups. The influence of post-growth non-equilibrium thermal treatments like pulsed laser annealing (PLA) and flash lamp annealing (FLA) on the $Ge_{1-x}Sn_x$ system is elucidated in **Chapter 4**. Therein, the microstructure, chemical composition, strain, and layer quality are carefully monitored. **Chapter 5** explains two approaches to fabricate highly doped thin film $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys on silicon on insulator (SOI) by molecular beam epitaxy (MBE) and a combination of Sn ion beam implantation and FLA. The fabricated materials are structurally investigated and non-equilibrium thermal treated. The insights gained are adapted to develop a fully CMOS-compatible top-down process flow to fabricate lateral $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ JLFET in **Chapter 6.** The fabricated transistors are electrically and structurally investigated to show the achievable device parameters with these materials. Finally, a brief conclusion and future prospects of the obtained results, as well as a comparison with other n-type transistors, are given in **Chapter 7**.

2 Fabrication and properties of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys

The general idea of alloying group IV semiconductors traces back to customizing the properties of Si or Ge. The modification occurs in most of the material parameters, such as band structure, carrier mobilities, lattice parameters, chemical reactivity, diffusion parameters, or oxidation behavior. This chapter will introduce the theoretical background of the fabrication and the most essential property modifications of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys.

2.1 Alloy formation

$Si_{1-x-y}Ge_ySn_x$ alloys consist of the elements Si, Ge, and Sn. All these elements belong to the group IV of the periodic table. Therefore, they have four valence electrons, leading to similarities in their bonding behaviors. An overview of the elemental properties is displayed in Table 2.1 - 1. At this stage, it must be mentioned that Sn exists in two allotropic forms under ambient pressure, namely α-Sn and β-Sn. α-Sn is the brittle non-metallic phase with a cubic-diamond lattice, which is desired for the Si-Ge-Sn alloy formation. The β-Sn phase is the ductile body-centered tetragonal metal-like phase, which appears as β-Sn that segregates after equilibrium thermal treatments at elevated temperatures [60-64]. In pure Sn, the phase transition from α-Sn to β-Sn occurs at 13 °C [65, 66]. During this transformation, the density ρ increases from 5.77 g cm^{-3} of α-Sn to 7.31 g cm^{-3} of β-Sn. This density change is equivalent to a decrease in volume of about 27% [66, 67]. On the other hand, Si and Ge crystallize in a cubic diamond crystal structure, like α-Sn. Furthermore, the lattice parameters *a* and densities of Si (0.541 nm, 2.34 g cm^{-3}) and Ge (0.566 nm, 5.32 g cm^{-3}) are much smaller than those for α-Sn (0.6489 nm, 5.77 g cm^{-3}). The lattice parameter of ternary $Si_{1-x-y}Ge_ySn_x$ alloys can be calculated for strain-relaxed alloys via Vegard´s law with a bowing parameter correction by Eq. 2.1 - 1 [68]:

$$a_{Si_{1-y-x}Ge_ySn_x} = a_{Ge} + \Delta_{SiGe}\, y + \Psi_{SiGe}\, y\,(1-y) + \Delta_{GeSn}\, x + \Psi_{GeSn}\, x\,(1-x) \qquad \text{Eq. 2.1 - 1}$$

Where $a_{Si_{1-y-x}Ge_ySn_x}$ is the alloy lattice parameter, Δ_{SiGe} and Δ_{GeSn} are the differences of the elemental lattice parameters, Ψ_{SiGe} = -0.0026 nm [68] and Ψ_{GeSn} = 0.0166 nm [68] are the bowing parameters. *x* and *y* describe the chemical composition of the alloy. The presented bowing parameters were determined for Ge-rich $Si_{1-x-y}Ge_ySn_x$. In the case of binary $Ge_{1-x}Sn_x$ alloys, Ψ_{GeSn} is in the range between 0.041 to 0.047 nm [69, 70]. Unfortunately, the absolute bowing value varies across the literature. The calculated

elastic constants C_{11}, C_{12}, and C_{44} of the elasticity matrix can be used to judge the elastic material properties. The generally smaller values of C_{11}, C_{12}, and C_{44} for Sn indicate a softer behavior than Si and Ge and could allow larger strain within $Si_{1-x-y}Ge_ySn_x$ layers compared to Si or Ge. The covalent radius a_k is defined as the averaged one-half of the distance of two identical atoms and describes the bond length. α-Sn has a 14.7% and 19.8% larger a_k compared to Ge and Si, respectively. This significant mismatch is assumed to be one reason for the low miscibility of Sn in Ge and Si [71, 72].

Table 2.1 - 1: Overview of the elemental properties of Si, Ge, α-Sn, and β-Sn in terms of crystal structure [73-76], density ρ [73-76], lattice parameter a [73-76], calculated elastic constants C_{11}, C_{12} and C_{44} [77, 78], covalent radius a_k [79] and melting temperature T_m [66, 76, 80, 81].

Material	Si	Ge	α-Sn	β-Sn
Crystal structure	cubic diamond	cubic diamond	cubic diamond	tetragonal body-centered
ρ (g cm^{-3})	2.33	5.32	5.77	7.28
a (nm)	0.54308	0.56576	0.6489	a=b=0.5831, c=0.3282
C_{11} (GPa)	160	122	66	74 *1
C_{12} (GPa)	63	46	34	62 *1
C_{44} (GPa)	78	61	44	23 *1
a_k (Å)	1.173	1.225	1.405	
T_m (K)	1685	1211	phase transition at 286	505

Indeed, $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ with x > 1% alloys are thermodynamically meta-stable, as visible in the equilibrium pseudo-binary $Si_{1-y}Ge_y$ - Sn phase diagram in Fig. 2.1 - 1. Thus, they cannot be produced in bulk form. The highest solid solubility of Sn at equilibrium conditions is observed in pure Ge with about 1.1 at.% at around 400 °C [82] and decreases by reducing the temperature to 0.52 at.% at room temperature [81]. Increasing the Si concentration in the $Si_{1-y}Ge_y$ - Sn alloy system decreases the solubility of Sn even further, as indicated by the movement of the solidus line to lower Sn concentrations (see Fig. 2.1 - 1). In pure Si, the highest solid solubility of Sn is achieved at 1200 °C, which is about 0.1 at.%. Hence, non-equilibrium processes (kinetic suppression of phase separation) are necessary to fabricate and process meta-stabile $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys.

*1 Whereas the elastic properties of Si, Ge, and α-Sn can be described by C_{11}, C_{12}, and C_{44} because of their crystal symmetry, the calculation of tetragonal β-Sn needs additionally C_{13}, C_{33}, and C_{44}, which can be found in ref. [78].

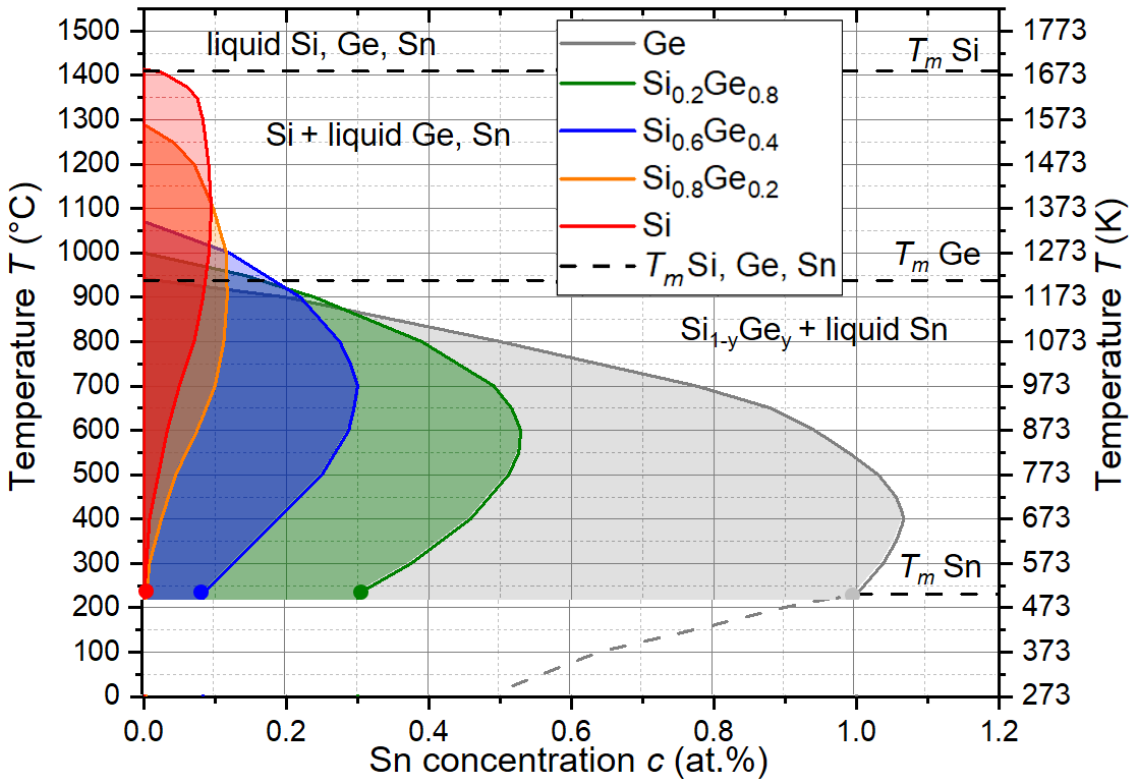


Fig. 2.1 - 1: Calculated pseudo-binary $Si_{1-y}Ge_y$-Sn equilibrium phase diagram with an Sn concentration range of 0 – 1.2 at.% and the $Si_{1-y}Ge_y$ alloys with y = 0, 0.4, 0.8 and 1. The points at 231 °C belong to the ternary eutectic points of the $Si_{1-x-y}Ge_ySn_x$ alloy. The content of the phase diagram refers to ref. [81] and [83]. Note: In the literature, no data was available for Sn concentrations between 0 and 0.52 at.% and temperatures below 231 °C. Elemental melting temperatures T_m were taken from Table 2.1 - 1.

Many CMOS-compatible approaches have been investigated in recent years, like molecular beam epitaxy (MBE) [40, 43, 84-93], chemical vapor deposition (CVD) [94-96], deposition of amorphous alloys followed by rapid thermal annealing (RTA) [97, 98], pulsed laser induced epitaxy (PLIE), epitaxial sputtering [64, 99, 100] followed by RTA [101], ion beam implantation followed by ultrafast annealing methods, e.g., pulsed laser annealing (PLA) [102, 103] or flash lamp annealing (FLA) [104]. Most of the fabrication approaches are still under optimization. However, CVD, ion beam implantation followed by non-equilibrium annealings, and MBE seem to be the most promising fabrication routes for high-quality single-crystalline $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys. Many parameters have a significant impact on the epitaxial growth with MBE and CVD, e.g., temperature, growth rate, pressure, targeted alloy composition, type of dopants, precursors/target quality, gas-/elementalflux, substrate quality, the construction of the tool (temperature control, chamber volume) and much more [71]. The selection of a suitable parameter combination will allow the fabrication of alloys with a homogeneous elemental distribution, low defect concentration, and a smooth surface.

At this stage, the influence of growth temperature and growth rate will be discussed since these are the key parameters for non-equilibrium and single-crystalline growth. Whereas the temperatures for MBE-grown $Ge_{1-x}Sn_x$ alloys are in the range of 25 [84, 105] - 225 °C [106], the temperature of CVD processes can reach up to 390 °C [37, 42, 46, 68]. The growth temperature for $Si_{1-x-y}Ge_ySn_x$ alloys can be slightly higher. The MBE growth above the eutectic temperature leads to inhomogeneity and phase separation at the sample surface*[2] [106-108]. The elevated growing temperatures for CVD processes seem to be enabled by hydrogen termination from the precursors (SiH_3, GeH_3) on the sample surface, suppressing Sn surface segregation [106]. Both techniques use relatively low growing temperatures in combination with large growth rates (up to 150 nm min^{-1} [71]) to achieve non-equilibrium conditions. This reduces the segregation length of Sn atoms and helps to avoid Sn surface segregation during the growth [71]. On the other hand, these non-equilibrium conditions can lead to a breakdown in crystal growth and enhanced defect formation [48]. Some point defects like Sn- and Ge-related vacancies are potential candidates to cause unintentional p-type background doping (see **section 2.3.3**). More details about the growth of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys can be found in refs. [71] and [109].

2.2 Strain and defects

In order to remain compatible with CMOS technology and reduce fabrication costs, the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys are typically fabricated on Si wafers. Unfortunately, Si has the smallest lattice parameter of these group IV elements. Therefore, the epitaxial pseudomorphic growth on Si causes a compressive strained $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ layer. Fig. 2.2 - 1 b) illustrates the perfect pseudomorphic growth. The separated relaxed crystals in Fig. 2.2 - 1 a) have equal in-plane $a_{//}$ and out-of-plane $a_{\perp}$ lattice parameters according to Table 2.1 - 1. The lattice parameter of $Ge_{0.9}Sn_{0.1}$ is calculated using Eq. 2.1 - 1. Owing to the coherent pseudomorphic growth in Fig. 2.2 - 1 b), the lattices of Ge and $Ge_{0.9}Sn_{0.1}$ take over $a_{//}$ of Si and become elongated in $a_{\perp}$ according to the volume constancy of the unit cell. Therefore, Ge and $Ge_{0.9}Sn_{0.1}$ are biaxial in-plane compressively strained and out-of-plane tensile strained when any strain relaxation events are excluded due to the ideal pseudomorphic growth. However, in-plane compressive strain is not desired for planar optoelectronics and n-type nanoelectronics

*[2] Most of the growing processes suffer from Sn surface segregations due to the lower surface energy of Sn_{liquid} (250°C) ≈ 0.58 J m^{-2} [107] compared to Si (100) ≈ 1.36 J m^{-2} [108], (110) ≈ 1.43 J m^{-2} [108], (111) ≈ 1.23 J m^{-2} [108] or Ge (100) ≈ 0.87 J m^{-2} [108], (110) ≈ 0.97 J m^{-2} [108], (111) ≈ 1.11 J m^{-2} [108].

(see **section 2.3**). Therefore, some methods to reduce strain were developed and will be briefly introduced.

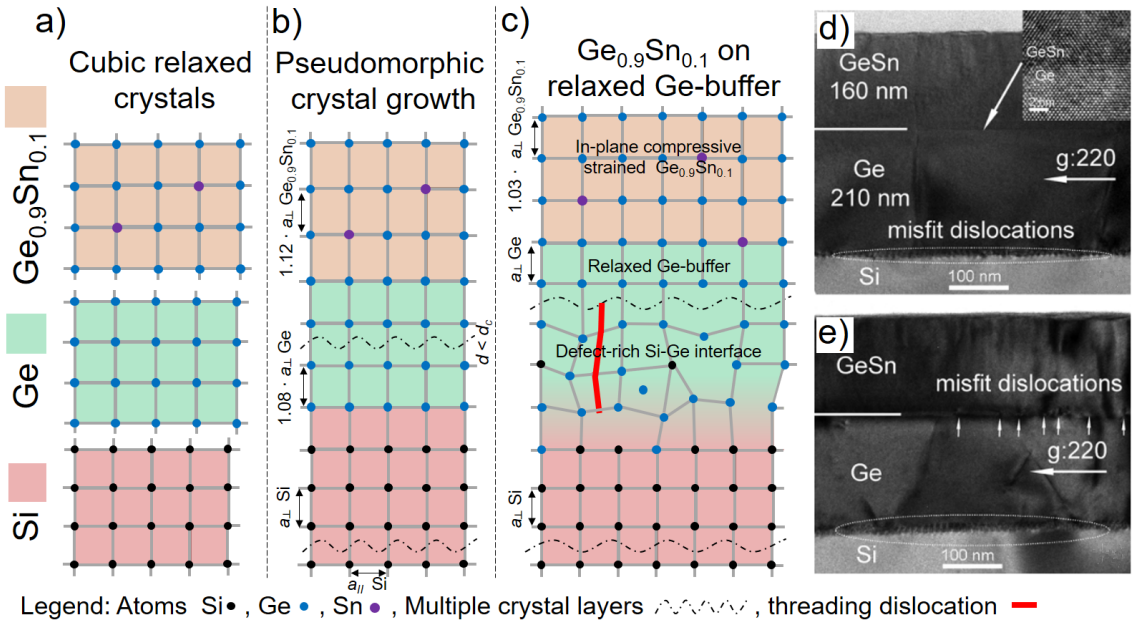


Fig. 2.2 - 1: Schematic of the relaxed cubic crystals of Si, Ge, and $Ge_{0.9}Sn_{0.1}$ with relaxed ($a_{//} = a_{\perp}$) in-plane $a_{//}$ and out-of-plane $a_{\perp}$ lattice parameters a). Single-crystalline lattice after ideal pseudomorphic growth of $Ge_{0.9}Sn_{0.1}$ and Ge on Si substrate with a constant in-plane lattice parameter of Si and elongated $a_{\perp}$ for Ge and $Ge_{0.9}Sn_{0.1}$ b). Ge–buffered Si substrate after strain relaxation via misfit and threading dislocation formation and a pseudomorphically grown $Ge_{0.9}Sn_{0.1}$ with a reduced strain compared to the ideal pseudomorphic growth c). Cross-sectional TEM image of the situation in c) with an inset of pseudomorphically grown Ge/$Ge_{0.92}Sn_{0.08}$ interface d) [110]. The situation of d) after post-growth thermal treatment above the critical temperature for strain relaxation of the $Ge_{0.92}Sn_{0.08}$ layer e) [110].

i) Strain relaxation via the layer thickness:

One way to reduce strain is the growth of a thick film above the critical thickness for plastically strain relaxation $d_{c,relax}$, which enables strain relaxation due to the formation of misfit dislocations [111], Lomer edge dislocations [112-114], threading dislocations [115], and extended defects (see Fig. 2.2 - 1 c)) [92, 116, 117]. However, this approach is limited by the critical thickness for epitaxial breakdown $d_{c,epi}$ ($d_{c,relax} < d_{c,epi}$) because of increasing surface roughness with increasing grown layer thickness [118]. $d_{c,relax}$ and $d_{c,epi}$ depend on many parameters like the fabrication method, growth temperature, growth rate, substrate quality, lattice mismatch, alloy composition, etc. [92, 119, 120]. Hence, this strain relaxation method relies on a good process control. Furthermore, strain relaxation events within the active layer reduce the alloy quality and degrade its properties.

ii) Insert buffer layers as a virtual substrate:

Another method is the growth of Ge-[121], $Si_{0.2}Ge_{0.8}$- [122] or graded $Si_{1-y}Ge_y$-buffer [115, 123] layers on Si substrates followed by a post-growth thermal treatment under

equilibrium conditions, e.g., *in situ* annealing at 848 °C for 30 min for MBE-grown Ge-buffers [122]. During the thermal treatment, the elements of the buffer and the substrate start to diffuse, and the previously compressively strained buffer layer can additionally relax by formation and annihilation of misfit dislocations [115], interfacial dislocations [111], and threading dislocations [115] (see Fig. 2.2 - 1 c)). The overall threading dislocation density (TDD) for a 200 nm thick Ge layer grown by CVD on Si is reduced from 1 x 10^{11} cm^{-2} in the as-grown state to 1 x 10^{9} cm^{-2} after annealing at 800 °C in H_2 [115]. By increasing the layer thickness over $d_{c,relax}$ to 4.7 µm, the TDD decreases from 3 x 10^{9} cm^{-2} in the as-grown state to 8 x 10^{6} cm^{-2} after annealing [115]. Hence, after the post-growth thermal treatment, the surface of the Ge-buffer layer has a lower defect concentration [124] and a $a_{//}$ similar to a fully relaxed Ge. Owing to the larger $a_{//}$ *of* Ge-buffers, they are widely used as virtual substrates (VS) for additional pseudomorphic growth of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys (see Fig. 2.2 - 1 c)). The largest compressive strain is expected for binary $Ge_{1-x}Sn_x$ systems, where the compressive strain increases roughly by 0.15% for every percentage of Sn when $Ge_{1-x}Sn_x$ is grown on Ge. The larger lattice parameter of partially strain-relaxed $Ge_{1-x}Sn_x$ layers makes this alloy an excellent candidate to become a novel buffer layer. For example, partially strain-relaxed $Ge_{1-x}Sn_x$ can be utilized as a buffer for tensile strained Ge [125] or graded $Ge_{1-x}Sn_x$-buffer layer systems [126], where the Sn concentration is systematically increased across the layer thickness and strain relaxation events occur preferentially in the bottom layers. However, the use of buffer layers makes the device processing more difficult because of additional interfaces or chemical reactions [37].

iii) Lattice parameter engineering:

It is possible to compensate the increasing lattice parameter difference between the substrate and the Sn-containing alloy by alloying or doping it with smaller elements like C [38], Si [37, 53], P [127], or B [37, 93, 127]. Therein, the most important element is Si since Si has the lowest lattice parameter in $Si_{1-x-y}Ge_ySn_x$ and a high miscibility with Ge. Therefore, this method enables the growth of partly strain-relaxed, fully strain-relaxed, and even tensile strained $Si_{1-x-y}Ge_ySn_x$ on Ge-buffers [37] but reduces the overall design freedom in the alloy composition depending on the targeted strain condition.

iv) Post-growth thermal treatments:

Post-growth thermal treatments are generally performed to reduce the defect concentration in the layer, as explained in **section 2.2 - ii)** for Ge-buffers. Unfortunately, there is a tendency to form Sn segregations owing to the meta-stability of the Sn-containing $Si_{1-x-y}Ge_ySn_x$ alloys. Therefore, only a few successful thermal treatments,

e.g., on $Ge_{0.93}Sn_{0.07}$, are reported. Fig. 2.2 - 1 d) shows the pseudomorphically grown $Ge/Ge_{0.92}Sn_{0.08}$ layer stack after RTA for 40 s at 300 °C [110], which indicates a certain thermal stability of the alloy. Here, misfit dislocations are observed only at the interface between Si and the Ge-buffer. The $Ge_{0.92}Sn_{0.08}$/Ge interface appears to be very smooth and defect-free. Fig. 2.2 - 1 e) shows a partial strain relaxation via the formation of misfit dislocations at the $Ge/Ge_{0.92}Sn_{0.08}$ interface after 40 s RTA at 540 °C [110]. Recently, a post-growth thermal treatment method for $Ge_{1-x}Sn_x$ by PLA was developed within this work and published in refs. [128] and [129]. This approach enables a complete strain relaxation via ns-liquid phase epitaxy. The fabricated films might be used as a new virtual substrate for the growth of tensile strained $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys. This method is discussed in detail in **section 4.1.5**.

v) Nano-fabrication:

Finally, there are post-growth fabrication methods reported that enable strain relaxation due to patterning of structures in small dimensions like nanowires [130], fins [131] or micro disks [95, 132]. The separation of the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloy layer from the surrounding or the substrate releases the elastic strain but is limited to small dimensions and does not release in-plane strain at the junction between the alloy and the stressor.

2.3 Electrical and optical properties

The electrical and optical properties of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys are mainly influenced by the chemical composition, strain, defect concentration, dopant concentration, and temperature. Owing to their influence on the material analysis, fabrication steps, and final device performance, it is crucial to introduce the properties of these novel materials in this section.

2.3.1 Band structure of strain-relaxed alloys

Many optical and electrical properties are influenced by their band structure. Si and Ge are semiconductors with indirect band-gaps of about 1.11 and 0.66 eV [20], respectively, whereas α-Sn is a semimetal with a negative direct band-gap of about -0.42 eV [14, 133]. The band structure calculations of each element with their most important conduction and valence bands are depicted in Fig. 2.3 - 1. All these three elements have a cubic diamond lattice and their valence band (VB) maximum at the Γ-point. The conduction band (CB) minima are located close to the X-point for Si, at the L-point for Ge, and at the Γ-point for α-Sn. Band structure parameters assigned to the position in reciprocal space are presented in Fig. 2.3 - 1 a) – Fig. 2.3 - 1 c). A quadratic interpolation by Eq. 2.3 - 1

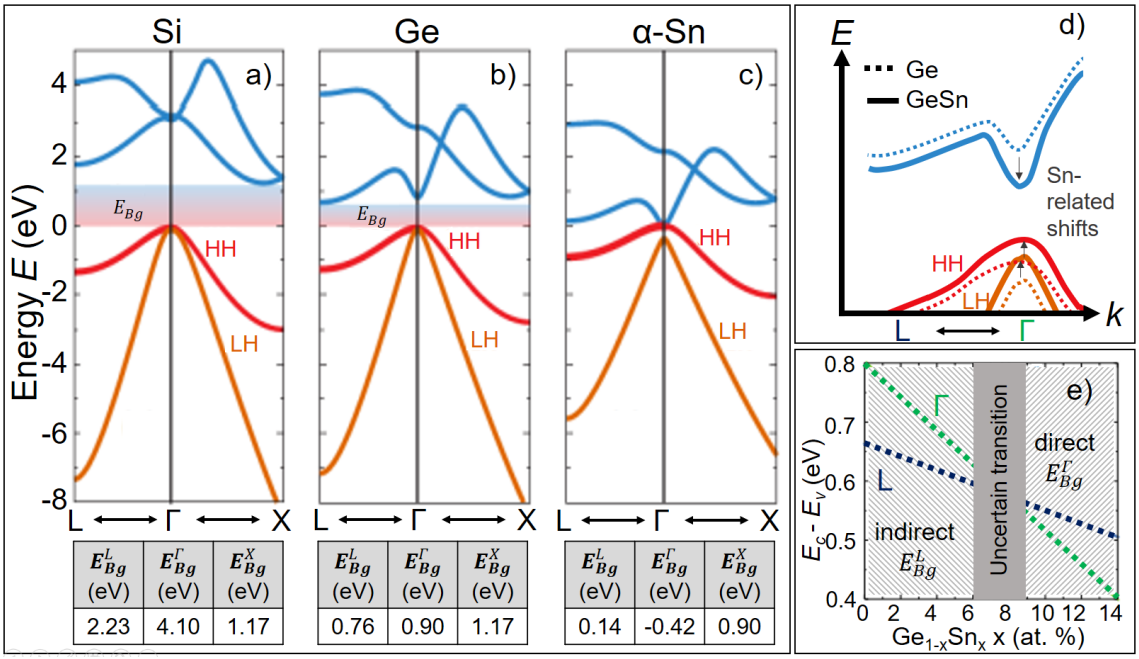
is one established approach to predict the direct-band-gap energy E_{Bg}^{Γ} for $Ge_{1-x}Sn_x$ and $Si_{1-y-x}Ge_ySn_x$ [134, 135].

$$E_{Si_zGe_ySn_x}^{\Gamma} = E_{Si}^{\Gamma}\, z + E_{Ge}^{\Gamma}\, y + E_{Sn}^{\Gamma}\, x - b_{SiGe}^{\Gamma}\, z\, y - b_{SiSn}^{\Gamma}\, z\, x - b_{GeSn}^{\Gamma}\, y\, x \qquad \text{Eq. 2.3 - 1}$$

$E_{Si_zGe_ySn_x}^{\Gamma}$ represents the direct E_{Bg} at the Γ-point of the $Si_zGe_ySn_x$ ($x + y + z = 1$) with the alloy composition x, y and z. E_{Si}^{Γ} / E_{Ge}^{Γ} / E_{Sn}^{Γ} are the elemental direct E_{Bg}, and $b_{SiGe}^{\Gamma}/b_{SiSn}^{\Gamma}/b_{GeSn}^{\Gamma}$ are the bowing parameters of the binary systems. Whereas elemental band energies can be determined by experiments, e.g., via optical transition by ellipsometry or photo-reflectance (PR) measurements, the binary bowing parameters are more difficult to determine. The reported bowing parameter fluctuates for b_{SiGe}^{Γ} between 0.0723 eV [136] and 0.27 eV [30, 137, 138] and for b_{GeSn}^{Γ} between 1.35 eV [139] and 2.49 eV [30, 140]. Since $Si_{1-x}Sn_x$ alloys are very difficult to fabricate because of the low solid solubility (see Fig. 2.1 - 1), the reported bowing parameter b_{SiSn}^{Γ} fluctuates in a huge range between -21 eV [140, 141] and 13.2 eV [52] and seems to be compositional-dependent [142]. Accurate band structure investigations for $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys are very complex because of strained alloys (see **section 2.3.2**), potential fluctuations due to disorder effects during alloying [137], and concentration-dependent bowing parameters [41, 134]. Even though it is currently not possible to determine E_{Bg}^{Γ} precisely for $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys, the estimation made by using Eq. 2.3 - 1 makes it possible to evaluate promising alloy composition.

The general effect of alloying Ge with Sn is depicted in Fig. 2.3 - 1 d). Alloying of Ge with Sn in a strain-relaxed material leads to an overall reduction of E_{Bg}, but in the Γ-valley E_{Bg}^{Γ} decreases much faster than in the L-valley E_{Bg}^{L}. This is caused by the fact that the difference between the E_{Bg} at the Γ-point is much larger than at the L-point ($\Delta E_{Bg}^{\Gamma} = E_{Ge}^{\Gamma} - E_{Sn}^{\Gamma} > \Delta E_{Bg}^{L} = \Delta E_{Ge}^{L} - E_{Sn}^{L}$). The transition from indirect into direct E_{Bg} semiconductor is predicted for strain-relaxed $Ge_{1-x}Sn_x$ between 6 and 9 at.% of Sn [42, 51, 87, 91, 143-146] (see Fig. 2.3 - 1 e)). The composition range is caused by slightly different experimental and theoretical results in the literature due to some difficulties. For example, the fitting of photoluminescence (PL) spectra is complicated because of the presence of different effects like changes in effective mass, hole splitting, alloy broadening, carrier lifetimes, band tail states, steady-state carrier occupation [87] and different dopant concentrations [146]. It is common to investigate the E_{Bg} at low temperatures to reduce the influence of some effects like thermal expansion, electron-phonon interactions, or broadening at the critical points and increase of the E_{Bg} size. This is highly important close to the transition point when the difference between

E_{Bg}^{L} and E_{Bg}^{Γ} is small (see Fig. 2.3 - 2 a)). Further information about the temperature-dependent E_{Bg} tuning mechanism can be found elsewhere [147]. Alloying $Ge_{1-x}Sn_x$ with Si leads to an additional degree of design freedom of the physical and chemical properties. Regarding the E_{Bg}, Si has the largest band-gap among these three elements (see Fig. 2.3 - 1 a)). Hence, the E_{Bg} of $Si_{1-x-y}Ge_ySn_x$ can be increased by increasing the Si concentration in the alloy. However, the gained design freedom by adding a third element makes it more challenging to draw a general image of the expected ternary alloy properties.



E_{Bg}^{L} (eV)	E_{Bg}^{Γ} (eV)	E_{Bg}^{X} (eV)
2.23	4.10	1.17

E_{Bg}^{L} (eV)	E_{Bg}^{Γ} (eV)	E_{Bg}^{X} (eV)
0.76	0.90	1.17

E_{Bg}^{L} (eV)	E_{Bg}^{Γ} (eV)	E_{Bg}^{X} (eV)
0.14	-0.42	0.90

Fig. 2.3 - 1: Theoretical band structure calculation via pseudopotential theory of elemental Si a), Ge b), and α-Sn c) with the CB in blue and VB of heavy holes (HH) in red and light holes (LH) in orange, respectively [41]. Γ is the center of the Brillouin zone, X is the intersection point with the [100] direction, and L is the intersection point with the [111] direction. Below the high symmetrical points are the corresponding E_{Bg} at 0 K [133]. Schematic of the alloying effect of Ge with Sn on the band structure d). The predicted transition from indirect to direct E_{Bg} in $Ge_{1-x}Sn_x$ depending on the Sn concentration e).

2.3.2 Band structure of strained alloys

As introduced in **section 2.2**, $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys are epitaxially grown on substrates, which can cause strain, depending on the lattice parameter difference between the substrate and alloy. The simulated influence of strain on the indirect-direct E_{Bg}^{Γ} transition is illustrated in Fig. 2.3 - 2 for $Ge_{1-x}Sn_x$.

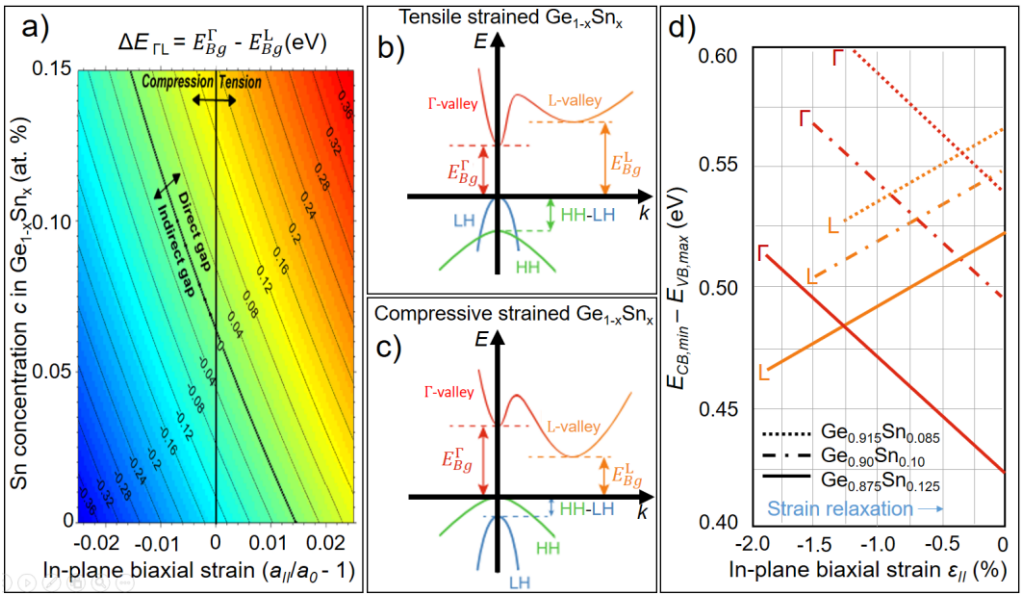


Fig. 2.3 - 2: Strain dependency of the indirect-direct band-gap transition for $Ge_{1-x}Sn_x$. The directness of the band-gap $\Delta E_{L\Gamma}$ in dependence of in-plane biaxial strain and Sn concentration a) [28]. Schematic of the band structure in the case of compressive strain b) and tensile strain c) [95]. Band-gap at the Γ- and L-point for pseudomorphically grown $Ge_{1-x}Sn_x$ (x = 8.5, 10, 12.5 at.%) on Ge in dependence of the relaxation degree d) [28].

As expected from **section 2.3.1**, the indirect-direct transition for in-plane strain-relaxed (ε_{II} = 0) $Ge_{1-x}Sn_x$ takes place at around 8 at.% of Sn (see Fig. 2.3 - 2 a)) and a higher Sn concentration reduces E_{Bg}. The effect of tensile strain in Fig. 2.3 - 2 b) is qualitatively similar to alloying with Sn (see **section 2.3.1**). It reduces E_{Bg}^{Γ} much faster than E_{Bg}^{L}. Additionally, the light holes (LH) band is lifted up above the heavy hole (HH) VB. Details about the strain-introduced band deformation can be found in the deformation potential theory or in the related literature for Si [148], Ge [148, 149], and $Si_{1-y}Ge_y$ [150]. In the case of pure Ge, a strain introduced indirect-direct transition was predicted at $\varepsilon_{II} \approx 1.9\%$ [149]. Since tensile strain and alloying of Sn work in the same direction, achieving the indirect-direct transition with a lower Sn concentration is possible when the alloy is tensile strained (see Fig. 2.3 - 2 a)). Recently, Elbaz et al. achieved a direct E_{Bg} in tensile strained (ε_{II} = +1.4%) $Ge_{0.946}Sn_{0.054}$ micro discs by nano-structuring and using SiN_x stressors [95]. On the other hand, compressive strain in Fig. 2.3 - 2 c) and Fig. 2.3 - 2 d) works in the opposite direction and shifts the indirect-direct transition to higher Sn concentrations as well as pushes the LH band downwards. In Fig. 2.3 - 2 d), the difference between the CB and VB extrema at the Γ- and L-points is displayed on the example of different compressive strained $Ge_{1-x}Sn_x$ with x = 8.5, 10, and 12.5 at.% alloys [28]. As expected, with increasing Sn concentration, the E_{Bg} drops down, and the increasing biaxial strain shifts the curve onset and transition point towards higher compressive strain values. Since both effects tend to compensate for each other, we can conclude that only an increased Sn concentration in $Ge_{1-x}Sn_x$ is not enough to achieve

direct E_{Bg} $Ge_{1-x}Sn_x$. Therefore, strain engineering is an essential topic in this research area. The first experimental proof of the indirect-direct transition was observed in a partially strain-relaxed ($\varepsilon_{//}$ = -1.16%) $Ge_{0.9}Sn_{0.1}$ by temperature-dependent PL in 2014 [151].

2.3.3 Doping-influenced properties

The non-equilibrium growth of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys causes point defects, as mentioned in **section 2.1**. Some point defects like Sn- and Ge-related vacancies and dislocations or a combination of both are potential candidates to cause an unintentional p-type background doping, which is in the range of 10^{16} cm^{-3} to 10^{18} cm^{-3} for $Ge_{1-x}Sn_x$ [37, 116, 152-155]. It is observed that the background doping increases with the Sn concentration and decreases by reducing the layer thickness [152]. Xie et al. reported a reduction in background doping from 2×10^{17} to 5×10^{16} cm^{-3} in $Si_{1-x-y}Ge_ySn_x$ after post-growth RTA without mentioning the RTA conditions and alloy composition [37]. The background doping causes some difficulties in device fabrication. For instance, it lowers the carrier mobilities (see **section 2.3.4**) and needs to be considered in the device concept. The unintentional p-type doping can be compensated, for example, by shallow n-type doping with P or Sb to achieve a compensated $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ alloy. The band structure of a compensated direct BG $Ge_{1-x}Sn_x$ alloy is presented in Fig. 2.3 - 3 a). On the other hand, special devices, like junctionless transistors (see **Chapter 6**) or low-resistance metal-semiconductor contacts, require high doping levels. In practice, different *in situ* and *ex situ* doped $Si_{1-x-y}Ge_ySn_x$ alloys with p-type dopants like B [27, 37, 96, 103, 156] or Ga [157] and n-type dopants like P [37, 104, 158], As [158] and Sb [93] with active dopant concentrations up to $\approx 3 \times 10^{21}$ cm^{-3} [159] can be fabricated. Activated dopants contribute mobile carriers in the semiconductor and enhance conductivity. In the case of high doping levels, shallow dopants can merge with the CB and VB and influence the band structure due to the so-called Burstein-Moss effect (see Fig. 2.3 - 3 b)), and band-gap renormalization or a combination of both (see Fig. 2.3 - 3 c)). For highly n-type doped semiconductors, the CB is filled with electrons. Since the Fermi level E_F is now lifted up deep into the CB (see Fig. 2.3 - 3 b)), the degenerated semiconductor attained a high electrical conductivity and behaves like a metal. Additionally, the Burstein-Moss effect can shift the effective absorption edge $E_{Bg}^{eff}(n)$ upwards, influencing the exact prediction of E_{Bg}^{Γ} due to ΔE_F offset [127, 146]. In the case of low Sn content alloys with an indirect BG, a high n-type doping can help to populate the CB valley at the Γ-point and lead to a quasi-direct semiconductor, as reported for Ge [160]. On the other hand, p-type dopants in Ge and $Ge_{1-x}Sn_x$ usually have much higher solid solubilities. The band structure of a highly p-type doped degenerated direct band-gap $Ge_{1-x}Sn_x$ is presented in

Fig. 2.3 - 3 c). Therein, the HH and the split-off (SO) bands are elevated, which reduces the E_{Bg}^{Γ} for a direct band-gap semiconductor due to band-gap renormalization. Additionally, E_F is shifted into the VB, which increases the effective absorption edge E_{Bg}^{eff}(p) (Burstein-Moss effect) for the highly p-doped semiconductor. Hence, the effects of band-gap renormalization and Burstein-Moss can compensate for each other since they work in opposite directions for p-type semiconductors. Compared to the n-type case, achieving a direct or quasi-direct semiconductor for indirect semiconductors with p-type doping is impossible since the CB remains unchanged. Nevertheless, super-conducting properties at low temperatures might also be achievable for $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys, as demonstrated for Ge hyperdoped with Ga ($n_{h+} \approx 1 \times 10^{21}$ cm^{-3}) with a critical temperature of about 0.45 K [161].

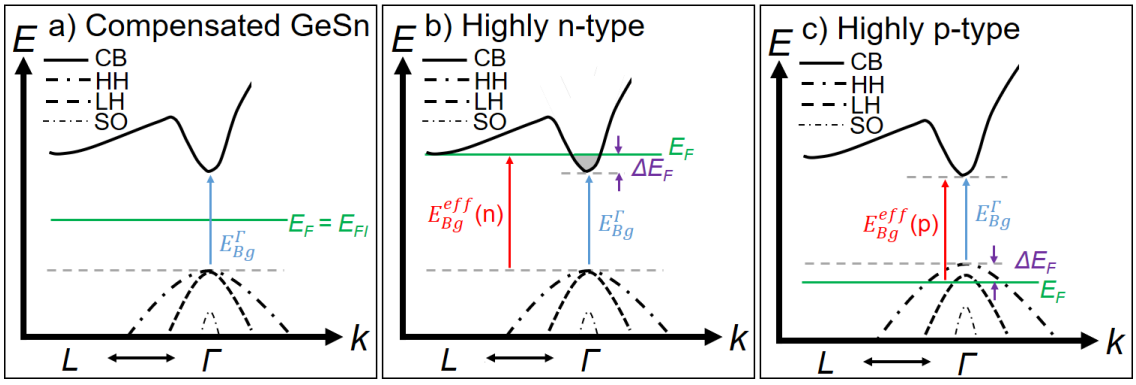


Fig. 2.3 - 3: Schematical band structure of strain-relaxed direct BG $Ge_{1-x}Sn_x$ in the intrinsic state a), in the degenerated highly n-type doped state b), and in the degenerated highly p-type doped state c). E_F is the Fermi level, E_{FI} is the intrinsic Fermi level, CB is the conduction band, HH is the heavy hole band, LH is the light hole band, and SO is the split-off band. $E_{Bg}^{eff}(n)$ and $E_{Bg}^{eff}(p)$ refer to the optical E_{BG} shift due to the Burstein-Moss effect.

2.3.4 Electrical properties

According to the k·p – theory [162-166], the smaller E_{Bg} of the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloy system leads to a decrease in the carrier effective mass m_{eff} [167]. Carriers with a lower m_{eff} can have a higher mobility μ, which is an essential parameter for electronic devices. However, μ also depends on scattering events with phonons and defects. Therefore, the $Si_{1-x-y}Ge_ySn_x$ alloying degree, lattice defects, and the introduced dopants play an essential role.

For $Ge_{1-x}Sn_x$, intensive investigations of μ in dependence on the carrier concentration were performed in ref. [152]. The author simulated and measured μ of unintentionally doped and P doped ($\approx 1 \times 10^{17}$ cm^{-3}) $Ge_{1-x}Sn_x$ with x = 0, 8.5, 10 and 12.5 at.% via Hall-effect in van-der-Pauw configuration of the partially relaxed alloys and strain-relaxed counterparts on insulator. The most important results are presented in Fig. 2.3 - 4. In Fig. 2.3 - 4 a), the undesired defect-dominated p-type background doping increases with

increasing Sn concentration from about 3×10^{17} to about 4×10^{18} cm^{-3}. This effect is reported multiple times in the literature and is attributed to Sn-related defects and dislocations caused by the low-temperature growth of the alloy (see **section 2.3.3**). At low temperatures, the carrier mobility presented in Fig. 2.3 - 4 b) is dominated by defects and impurity scattering. Therefore, the Ge virtual substrate (VS) and the partially strain-relaxed $Ge_{0.915}Sn_{0.085}$ have the highest mobility. At around 300 K, the mobility is limited by phonon scattering, which is in a similar range for Ge and $Ge_{1-x}Sn_x$. Additionally, the small difference in the E_{Bg}^{L} and E_{Bg}^{Γ} of the $Ge_{0.915}Sn_{0.085}$ could lead to inter-valley scattering events. The results of the n-type $Ge_{0.875}Sn_{0.125}$ epitaxial layer and strain-relaxed n-$Ge_{0.875}Sn_{0.125}$ on insulator (GeSnOI) are presented in Fig. 2.3 - 4 c) and d). The GeSnOI material has a significantly lower dopant concentration than the same layer in contact with the Ge-VS. Additionally, the GeSnOI mobility is much higher at room temperature, which is most probably due to a combination of the reduced dopant concentration and strain relaxation (higher Γ-valley occupation). At room temperature, μ_{e^-} of Ge and n-$Ge_{0.875}Sn_{0.125}$ are in the same range since both materials are indirect band-gap semiconductors with a high L-valley electron population. The results show the benefit of strain-relaxed GeSnOI compared to epitaxially grown Ge and GeSn layers grown on Ge. On the contrary, the simulated μ was determined to be about 6000 $cm^2\ V^{-1}s^{-1}$ at room temperature, which is significantly higher than the measurement result. The author mentioned that the background doping might be a reason for this difference and pointed out that one sample with a lower Sn concentration reached μ_{e^-} of 4600 $cm^2\ V^{-1}s^{-1}$ ($n_{e^-} = 3 \times 10^{17}\ cm^{-3}$). Therefore, it might be possible to boost the GeSnOI mobilities further by reducing the undesired background doping via post-growth thermal treatments, as presented in ref. [37], or by further improvements in growth conditions.

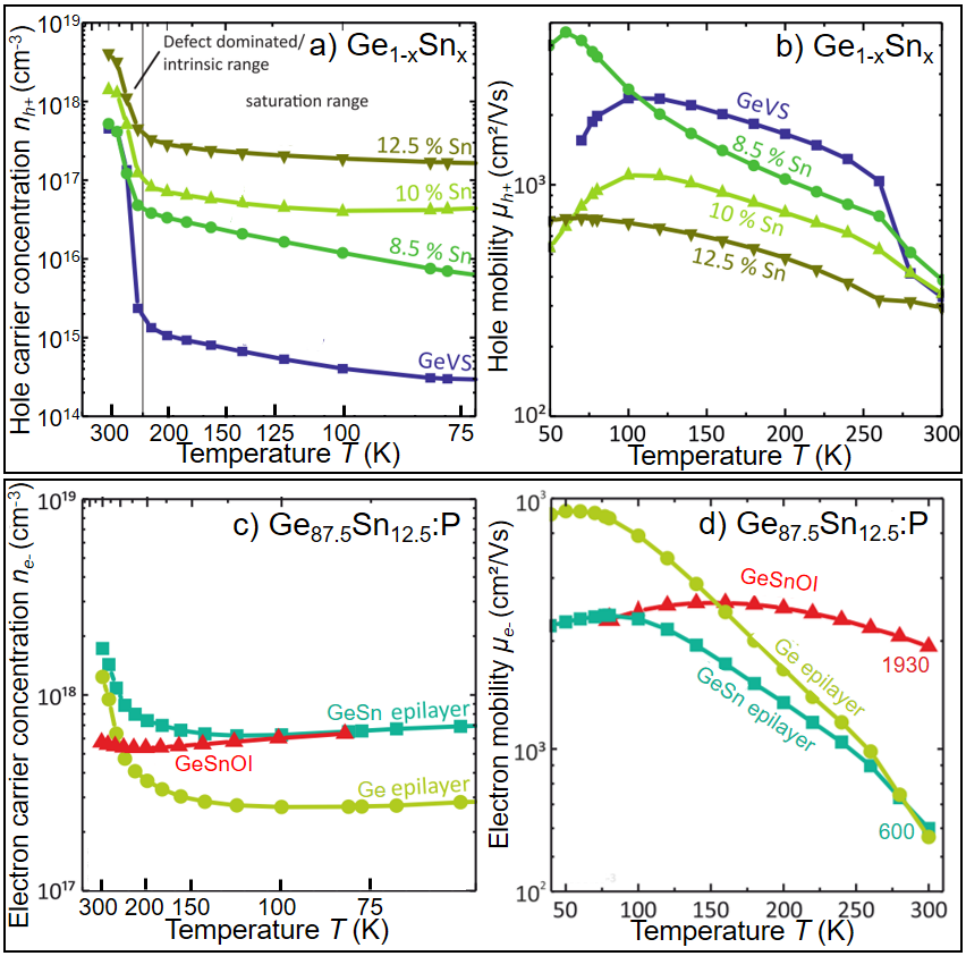


Fig. 2.3 - 4: Hall-effect results of CVD grown $Ge_{1-x}Sn_x$ [152]. Hole concentration a) and mobility b) of the unintentional p-$Ge_{1-x}Sn_x$ (x = 0, 8.5, 10, and 12.5 at.% with a layer thickness of 2500, 768, 835, and 414 nm, respectively). Comparisons of the electron concentration c) and mobility d) of epitaxially grown Ge (Ge epilayer), n-$Ge_{0.875}Sn_{0.125}$ (GeSn epilayer), and the strain-relaxed $Ge_{0.875}Sn_{0.125}$OI (GeSnOI).

For $Si_{1-x-y}Ge_ySn_x$, the electrical properties scatter due to the different alloy compositions, doping levels, and less-known fabrication parameters. Therefore, two different conclusions were drawn depending on the doping level: i) In the case of low dopant concentrations, a reduced μ is observed when Ge is alloyed with Si or Sn [96, 122, 158]. This effect was mainly attributed to an enhanced alloy scattering. However, for highly doped alloys ii), the presence of Sn does not negatively influence the electrical properties, as shown in Fig. 2.3 - 5. The comparable trend of Ge and the $Si_{1-x-y}Ge_ySn_x$ alloys in the resistivity measurements in Fig. 2.3 - 5 a) does not indicate significant additional alloy scattering due to Si and Sn. Similar conclusions were drawn by Wang et al. for Sn and B implanted $Si_{0.75}Ge_{0.25}$, presented in Fig. 2.3 - 5 b) [103]. For the $Ge_{1-x}Sn_x$ system, similar mobilities were observed compared to p-type Ge when the doping levels were above 1×10^{19} cm^{-3} (see Fig. 2.3 - 5 c)) [96, 158]. Such high carrier concentrations (1×10^{19} to 5×10^{19} cm^{-3}) are desired for the junctionless transistors fabricated and characterized in **Chapter 6**.

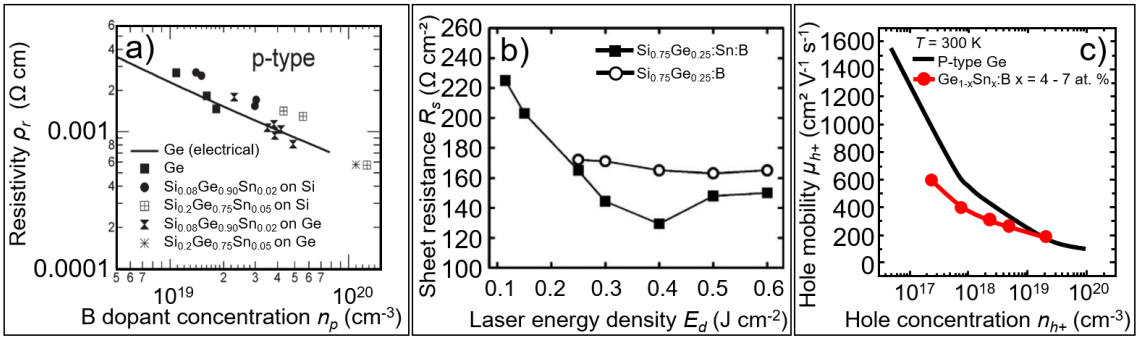


Fig. 2.3 - 5: Resistivity comparison of B doped Ge, latticed matched CVD grown $Si_{0.08}Ge_{0.90}Sn_{0.02}$ on Ge, $Si_{0.20}Ge_{0.75}Sn_{0.05}$ on Ge, $Si_{0.20}Ge_{0.75}Sn_{0.05}$ on Si in dependence of their B dopant concentration a) [37]. Sheet resistance of the $Si_{0.75}Ge_{0.25}$:Sn:B and $Si_{0.75}Ge_{0.25}$:B implanted samples with Sn (D_I = 8 x 10^{15} cm^{-2} at E = 30 kV) and B (D_I = 4 x 10^{15} cm^{-2} at E = 5 kV) versus the laser energy density E_d needed for recrystallization [103]. Hole mobility μ_{h+} of p-type Ge (bulk) and 80 nm $Ge_{1-x}Sn_x$:B (x = 4 - 7 at.%) grown on Ge versus the active hole concentration n_{h+} measured at 300 K c) [96].

As shown in this section, it is possible to improve the electrical properties by alloying Ge and $Si_{1-y}Ge_y$ with Sn. However, inherent fabrication defects still inhibit achieving the magnificent calculated electrical properties. Furthermore, the reduced E_{Bg} can cause increased band-to-band tunneling leakage that limits the electrical performance of fabricated devices. Therefore, it seems necessary to perform strain engineering and intelligent alloying of Ge and $Si_{1-y}Ge_y$ with Sn to achieve the desired device performance.

2.4 Thermal treatments

Thermal treatments are widely used to improve crystal structures, activate dopants, recrystallize amorphous materials, grow thermal oxides, or reduce contact resistance via metal-semiconductor alloy formation. Unfortunately, by shrinking the device dimensions or using novel meta-stable materials, like the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloy systems, long thermal treatments are not acceptable anymore. Since diffusion is a temperature- and time-dependent process, only very short annealing allows sharp property transitions and further miniaturization. Additionally, meta-stable materials can start to segregate when it comes to equilibrium conditions at high temperatures, as explained in **section 2.1**.

The thermal stability of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys with different compositions and annealing approaches has been investigated in recent years [106, 110, 168-170]. However, the authors came to different conclusions since many parameters varied between their experiments, like the growth method [169], growth temperature, alloy composition, alloy quality (dislocation density [169], degree of relaxation [169], layer thickness) and the annealing conditions (method, time, temperature, heating rate, cooling rate, atmosphere, etc.). Furthermore, it is very difficult to observe Sn segregations in the early nucleation stages by scanning electron microscopy (SEM),

transmission electron microscopy (TEM), or X-ray diffraction (XRD) since the first clusters have a size below the detection limit of used techniques, are randomly distributed, and their entire volume fraction is low. A few important thermal stability results will be exemplarily reviewed in this section.

Groiss et al. performed *in situ* annealing between 200 and 275 °C in an MBE chamber directly after the growth of $Ge_{0.9}Sn_{0.1}$ on Ge and investigated the material with SEM and XRD [106]. They reported Sn surface segregations and a reduced crystal quality already after 15 min annealing at temperatures slightly above 231 °C [106]. These results were supported by XRD rocking curves, which indicate layer quality reduction after annealing [106]. Unfortunately, they did not present the depth distribution of elements to evaluate the Sn-diffusion towards the surface. Comrie et al. grew an 80 nm thick $Ge_{0.935}Sn_{0.065}$ layer on a Ge-buffered Si substrate by CVD and performed post-growth thermal treatments between 300 and 700 °C for 30 min in a vacuum oven [168]. They could show by Rutherford backscattering spectrometry (RBS) and XRD measurements that $Ge_{0.935}Sn_{0.065}$ can be heated up to 400 °C without any strain relaxation and Sn segregation. The strained alloy relaxes above 400 °C, and first Sn redistributions were visible after annealing at 475 °C. The channeling yield stayed relatively constant with respect to the as-grown state, which means that no additional Sn atoms diffuse from substitutional to interstitial lattice position up to 575 °C. When the temperature exceeded 575 °C, Sn diffused towards the surface, degrading the material quality. Similar thermal stabilities and strain relaxation observations were reported by Li et al. on 160 nm thick $Ge_{0.935}Sn_{0.065}$ grown by MBE on a Ge-buffered Si substrate after RTA between 300 and 620 °C for 40 s [110]. Zaumseil et al. investigated thermal stability and strain relaxation of pseudomorphic and partially strain-relaxed CVD-grown $Ge_{1-x}Sn_x$ (x = 5, 9, 12 at.%) with XRD, TEM, and PL. The thermal treatment was performed *in situ* in the XRD chamber from room temperature to up to 700 °C with a heating rate of 30 K/min and maintaining the temperature for each step 15-20 min. They observed for the already partly strain-relaxed $Ge_{1-x}Sn_x$ alloys a proceeding strain relaxation at $T \approx 300$ °C for $Ge_{0.95}Sn_{0.05}$, $T \approx 250$ °C for $Ge_{0.91}Sn_{0.09}$, $T \approx 270$ °C for $Ge_{0.88}Sn_{0.12}$ followed by β-Sn segregation at $T \approx 620$ °C for $Ge_{0.95}Sn_{0.05}$, $T \approx 400$ °C for $Ge_{0.91}Sn_{0.09}$, $T \approx 300$ °C for $Ge_{0.88}Sn_{0.12}$. On the other hand, the pseudomorphically grown $Ge_{0.95}Sn_{0.05}$ counterpart did not show proceeding strain relaxation up to 620 °C but a sudden Sn segregation at $T \approx 640$ °C. Hence, the presence of treading- and misfit dislocations in the as-grown material has a significant influence on strain relaxation and might also influence the critical temperature for β-Sn formation.

Furthermore, some experiments indicated the potential to increase the thermal stability of $Si_{1-x-y}Ge_ySn_x$ alloys by reducing the Sn concentration [167, 169] or increasing the Si fraction [37, 68]. In contrast, Fournier-Lupien et al. reported for CVD-grown $Ge_{0.88}Sn_{0.12}$ a thermal stability at 460 °C by *in situ* SEM. In the same experiment, they observed Sn surface segregation in $Ge_{0.84}Si_{0.04}Sn_{0.12}$ alloy already at 415 °C, which speaks against the higher thermal stability of the ternary compared to the binary alloys [170].

Nevertheless, some processes, like the activation of implanted dopants or contact formation, benefit from thermal treatments. Therefore, it is suggested that non-equilibrium thermal treatments be used to improve the layer quality, inhibit Sn segregation, and reduce elemental redistributions during processing.

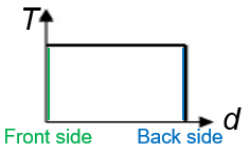
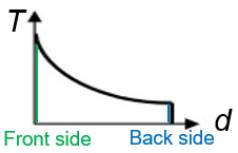
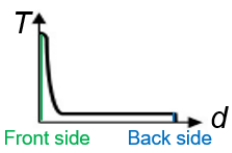
The general idea of non-equilibrium thermal treatments is reducing the annealing time t while increasing the peak temperature T_p, which requires high heating and cooling rates. According to Eq. 2.4 - 1, diffusion processes depend mainly exponentially on temperature T. D is the diffusion coefficient, D_0 is the slightly temperature-dependent diffusion pre-exponential factor, E_A is the activation energy for diffusion, and k_B is the Boltzmann constant. On the other hand, the diffusion length x_D often has a square root-like dependence on time (see Eq. 2.4 - 2) [171].

$$D = D_0 \, e^{\left(\frac{-E_A}{k_B T}\right)} \qquad \text{Eq. 2.4 - 1}$$

$$x_D \approx 2\sqrt{D\,t} \qquad \text{Eq. 2.4 - 2}$$

However, it must be mentioned that the *in situ* temperature measurements and modeling of non-equilibrium effects are complicated when it comes to ultra-short-time processes. Additionally, the component-dependent diffusion coefficients for novel metastable alloys are rarely known.

Table 2.4 - 1: Comparison of the most common non-equilibrium thermal treatment methods RTA, FLA, and PLA [171, 172].

Method	RTA	FLA	PLA
Light source	Halogen lamp	Xenon flash lamp	Laser
Light source spectra	Broad, max. ~ NIR	Broad, max. ~ blue	Discrete lines, UV to MIR
Temperature T profile versus the sample depth d			
Annealing time	1 s - 100 s	10 µs - 100 ms	300 fs - 40 ns
Heating rate (K/s)	10^3	10^4 - 10^7	>10^8
Cooling rate	Slow	Medium	High

The most suitable non-equilibrium thermal treatments for $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys are RTA, flash lamp annealing (FLA), and pulsed laser annealing (PLA). A brief comparison between these methods is summarized in Table 2.4 - 1 and will be explained in the associated sub-sections below. All three methods are based on light sources and their associated spectra. The wavelength of the light source is an essential parameter for the material-dependent absorption. Usually, light is absorbed close to the surface, and the heat is guided through the material via thermal conduction.

2.4.1 Rapid thermal annealing

RTA is a fast annealing method that uses halogen lamps to heat the material within seconds. The process proceeds isothermally, meaning that the samples obtain a similar temperature on the front and back side of the sample over the whole annealing time (see temperature profile in Table 2.4 - 1). For a conventional RTA system, the annealing time is between 1 s and 100 s [171]. Compared to FLA and PLA, this method generates the smallest thermal stress in the material due to relatively low cooling rates. This helps to prevent cracks in the wafer but does lead to undesired longer elemental diffusion length. Some work with RTA on $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys has been done regarding post-growth thermal treatments, as mentioned in Refs. [42, 110, 117, 119] and contact formation at temperatures close to the $Si_{1-x-y}Ge_ySn_x$ growth temperature [122, 152, 173]. Since the segregation of β-Sn in $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys is critical for the device performance, it seems more suitable to use ultra-short-time annealing methods with steep thermal gradients.

2.4.2 Flash lamp annealing

FLA uses an intense flash from Xenon (Xe)-lamps mounted above the sample for thermal treatment. The schematic of an FLA setup is depicted in **appendix 8.27**. The time scale of the flash is normally between 10 µs and 100 ms [171]. Depending on the selected annealing length, FLA can be classified as isothermal for long pulses (long annealing time, as explained for RTA in **section 2.4.1**), thermal flux, and adiabatic for very short annealing times (see explanation in **section 2.4.3**). In the case of the thermal flux regime, the flash length is in the same time range as the heat can be conducted through the sample. Therefore, the temperature reaches its maximum close to the surface and decays across the sample thickness until stable conditions are reached (see temperature-depth profile in Table 2.4 - 1). The resulting annealing temperatures (T_p, T_{equ}, T_0) depend mainly on the FLA settings (flash energy density, flash-time profile, spectrum of the Xe-lamp ($\lambda \approx 250 - 1000$ nm), pre-heating parameter) and material properties (absorption, thermal conduction, heat capacity, thickness). Therefore, the same FLA parameters applied to different materials will cause different temperature

profiles. Furthermore, the absorption can be influenced by the E_{Bg} and changed surface properties due to patterned structures or other roughness-causing processes. When the flash energy is absorbed by the sample, a heatwave propagates across the material. This leads to a large thermal gradient across the wafer thickness that can induce the wafer bending, and finally, the wafer can break. In order to reduce the thermal gradient, a pre-heating system close to the backside of the sample can be used.

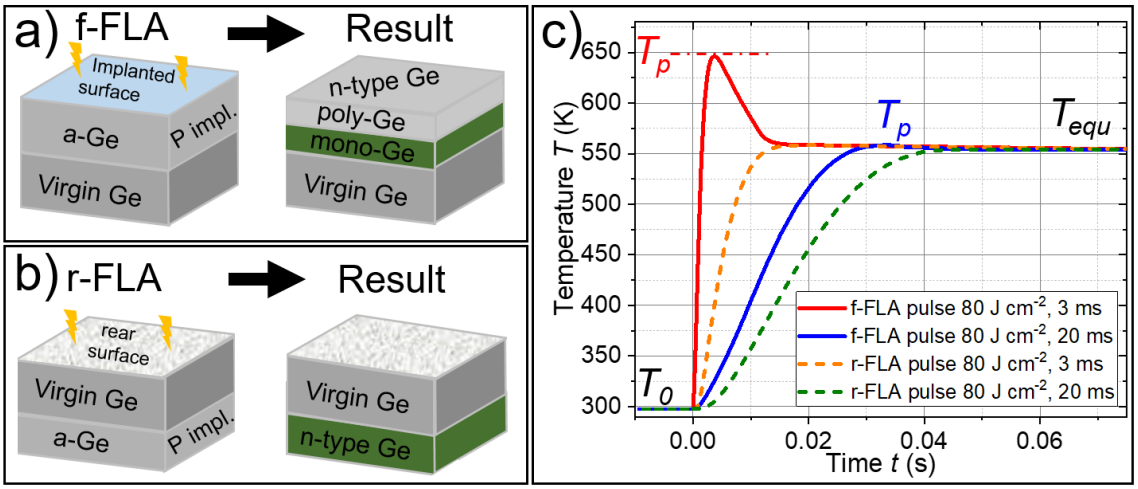


Fig. 2.4 - 1: Schematically explanation for f-FLA a) and r-FLA b) on the example of a recrystallization process of P implanted amorphous Ge (a-Ge) with the explained double layer formation due to f-FLA and single-crystalline Ge layer formation by r-FLA [174]. Temperature profile according to COMSOL, simulating the time-dependent heatwave propagation in bulk Si in the case of f-FLA and r-FLA for a flash energy density E_d = 80 J cm^{-2} and a pulse length of 3 and 20 ms c). T_0 is the temperature before FLA, T_p is the peak temperature, and T_{equ} is the quasi-equilibrium temperature.

Conventionally, the flash is applied from the front side of the sample (f-FLA), as visible in Fig. 2.4 - 1 a). This leads to a direct annealing of the targeted surface layer, e.g., an amorphous germanium (a-Ge) layer formed during the ion beam implantation process. When the amorphous layer thickness is in the range of 100 nm or larger, two different crystallization processes can take place for f-FLA, as reported by Prucnal et al. [174]. On the one hand, the a-Ge recrystallizes epitaxially from the interface between the implanted and virgin Ge towards the sample surface. On the other hand, after a short incubation time, a nucleation process on the hot surface occurs and forms laterally and in-depth growing nanocrystals on the top surface. This top surface recrystallization creates a thin polycrystalline doped Ge layer on a single-crystalline doped Ge layer. In the case of an applied flash on the sample rear-side (r-FLA) (see Fig. 2.4 - 1 b)), the heatwave propagates through the wafer until the elevated temperature activates the explosive solid-state epitaxy. This recrystallization process starts at the interface between the amorphous Ge and the virgin Ge and avoids the formation of nano-crystalline Ge on the surface. The time-dependent temperature of the heatwave can be simulated by the software “COMSOL” [175]. An exemplary simulation of temperature evolution on the

sample front side during f-FLA and r-FLA is shown in Fig. 2.4 - 1 c) for bulk Si. For f-FLA, the annealing starts (t = 0 s) at room temperature with T_0 and increases rapidly by applying the pulse until the peak temperature T_p is reached. The thermal spike propagates as a heatwave through the sample until the quasi-equilibrium temperature (T_{equ}) is reached. For r-FLA, the T_{equ} is used for annealing. By comparing the different pulse lengths simulated with the same energy density, it is obvious that a shorter pulse length leads to higher T_p.

FLA is not only a method to heal implantation defects and activate dopants, it can also be used for contact formation (**section 5.2.4**) or might be helpful to reduce the point defect density in semiconductors, as discussed in **section 4.2**.

2.4.3 Pulsed laser annealing

PLA is an annealing method for thin films (<1 µm) and is based on the strong light (λ = 380 - 780 nm) absorption in the surface regions of semiconductors like Si and Ge. Usually, monochromatic pulsed excimer lasers with pulse lengths between 300 fs [176] and 40 ns [171] are used as a light source. Owing to the high absorption, the material can be rapidly heated up, melted, and solidified with cooling and heating rates of 10^8 [172] - 10^{10} K s^{-1} [177] *3. This makes PLA an adiabatic process in which only a thin layer at the surface is significantly heated up (see Table 2.4 - 1). However, this extreme thermal gradient makes this method more sensitive to thermal stress than FLA. Additionally, the monochromatic laser makes the PLA more influenced by surface-related structures or interference-causing patterns. The reported ultra-fast thermal treatment has some advantages over conventional RTA or equilibrium oven treatments.

i) The process is very fast and does not necessarily need a special atmosphere or vacuum. This reduces the processing time.

ii) The thermal treatment can be controlled in depth by varying the laser fluence, as shown in Fig. 4.1 - 2 b), and the treated area can be selected by varying the beam focus. Therefore, the major part of the material is still unaffected, and diffusion processes are partially suppressed because of the short time scales in the case of solid phase epitaxy [178, 179]. The diffusion coefficient for liquid phase epitaxy is usually many magnitudes higher than in the solid phase. This allows the formation of a single-crystalline material with a box-like elemental distribution after ion beam implantation since the atoms can be equally distributed in the liquid [102, 103, 172]. In this case, it is necessary to have the

*3 Cooling rates higher than 10^{10} K s^{-1} are reported for melted Si because of a relatively high thermal conductivity in the liquid phase of ~ 67 W m^{-1}K^{-1} [177].

depth of the molten layer larger than the amorphization depth. Additionally, it was reported that the amorphous layer melts at temperatures of 100 - 200 K below the melting point of the crystal and depends on the selected dopant [177].

iii) The reported high heating and cooling rates allow the fabrication of materials far away from the thermodynamical equilibrium. Therefore, this method is considered for $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloy formation and ultra-high doping. In practice, PLA has shown the highest concentration of incorporated dopants in Si [172], Ge [178, 180, 181] and $Ge_{1-x}Sn_x$ [159, 182]. In some cases, the reported dopant concentrations exceed the equilibrium solubility limits by a factor of 500 [183]. Such high impurity concentrations can be achieved when the solidification velocity is larger than the impurity out-diffusion [184]. However, if the dopant concentration exceeds this non-equilibrium solubility, then the material can form lamellar or cellular structures with dopant segregation on the cell wall sides since the liquid-solid interface is not any more stable [172]. One approach to explain the non-equilibrium cell formation was proposed by Mullins [185] and Narayan [172].

2.5 Summary

The material class of group IV $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys enables broad design freedom in chemical and physical properties. The fabrication of high-quality $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys requires non-equilibrium processes. Currently, the dominant fabrication methods are non-equilibrium MBE and CVD processes at relatively low temperatures and high growth rates since the equilibrium solid solubility of Sn in $Si_{1-x-y}Ge_ySn_x$ is limited to about 1 at.%. The fabricated alloys show the potential to become one of the leading fully CMOS-compatible materials for opto- and nanoelectronics. The ability to independently modify the band-gap, the charge carrier mobility, and the lattice parameter by adjusting the chemical composition or strain is very promising. In general, increasing the Sn concentration in $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys or tensile strain moves the properties towards a direct semiconductor with a reduced band-gap. On the contrary, increasing the Si concentration or applying compressive strain increases the band-gap and favors indirectness. However, higher Sn concentrations reduce the thermal stability and can generate compressive strain depending on the used substrate. Therefore, focusing only on the Sn concentration would not automatically lead to a direct-band-gap-material of a device-grade quality. Nevertheless, these Sn-containing direct-band-gap and CMOS-compatible alloys might be the missing component to fabricate fully integrated group IV semiconductor lasers. Electrical investigations of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ showed improved or at least similar

properties like Ge, highlighting these alloys as promising active components for various electronic devices. Very high carrier mobilities in the range of 6000 $cm^2 V^{-1}s^{-1}$ at room temperature were theoretically predicted, but the undesired p-type background doping, which appears during the non-equilibrium growth by defect formation, diminishes the measured mobilities. Therefore, in reality, mobilities of up to 4600 $cm^2 V^{-1}s^{-1}$ ($n = 3 \times 10^{17}$ cm^{-3}) were measured in strain-relaxed GeSnOI. From Ge and $Si_{1-y}Ge_y$ alloys, it is known that post-growth thermal treatments can remove some of the defects created during growth. However, the thermodynamic instability of Sn in $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ prevents the application of state-of-the-art equilibrium *in situ* thermal treatments during the growth at temperatures significantly above the growth temperature. One way to overcome this problem are highly non-equilibrium thermal treatments like FLA and PLA, which will be addressed in this thesis. A detailed understanding of the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ material responses during these ultra-short high-temperature treatments and suitable process windows are still missing. However, knowing these processes can pave the way to realize high contact qualities and enable the implementation of *ex situ* doping processes via ion beam implantation followed by an appropriate thermal treatment.

Another challenge for the successful integration of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ is the in-plane compressive strain, which appears due to the epitaxial growth of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on substrates with smaller lattice parameters like Si or Ge. The in-plane strain influences especially planar device concepts. Whereas the compressive strain might be helpful for p-type MOS (PMOS) devices [71], for n-type MOS (NMOS) and optoelectronics applications, strain-relaxed, defect-free, or even tensile strained materials are desired. Hence, different approaches were developed to overcome these strain-related issues, for example, the growth of thick layers, inserting virtual substrates, nano-structuring, post-growth thermal treatments, and alloy engineering by adding smaller elements. On the other hand, the possibility to reduce or increase the lattice parameter by alloying Ge with Si and Sn paves the way for applications of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ as stressors [156, 186] or virtual substrates to further tune the properties of currently better-known semiconductors like Si, $Si_{1-x}Ge_y$ or Ge.

Nevertheless, it must also be mentioned that $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys are still a relatively young material class. Therefore, the data availability for ternary alloys is still limited, which causes larger uncertainties in the simulation of alloy properties. Here, more data can improve the precision of the results soon. The database for the binary $Ge_{1-x}Sn_x$ system is much larger since the growth was achieved earlier, and the composition opportunities are limited.

3 Experimental setups

This chapter introduces important and frequently used measurement setups and methods. Other techniques will be explained at the position where it is needed. I would like to thank all institutions and collaborators named below for the experimental support and advice for the analyses of the experimental data. All experiments with named collaborators were performed and analyzed in cooperation with the author, Oliver Steuer. Experiments without named collaborators are performed and analyzed by Oliver Steuer.

3.1 Molecular beam epitaxy (MBE)

Most of the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys in this thesis were fabricated by a solid source MBE system with a base pressure of 1×10^{-10} mbar by Dr. Daniel Schwarz at the University of Stuttgart. The elements Ge, Sn, Sb, and B were evaporated using Knudsen effusion cells. Si was evaporated via electron beam evaporation. The general approach was to use commercially available Si or Si on insulator (SOI) wafers as a substrate. The SOI wafers were cleaned, etched in 2.5% HF for 15 s, and immediately inserted in the MBE chamber. The Si wafers were cleaned, and the native SiO_2 was removed by thermal desorption at a substrate temperature $T_S \approx 900$ °C. Afterward, an Si-buffer layer was grown in order to reduce the influence of substrate-surface-related defects. Next, a Ge-buffer was grown and thermally treated *in situ* in the MBE chamber to relax the compressive strain and reduce the defect concentration. Finally, the $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ alloys were grown. Details of the process parameters used for each sample can be found in **appendix 8.1** and **8.12**. The T_S was controlled by a graphite heater calibrated with a thermocouple ($T_S > 300$ °C) and an infrared camera ($T_S < 300$ °C) [93].

3.2 Ion beam implantation

Ion beam implantation of P, Ga, and Sn was either performed using a 40 kV and 500 kV ion implanters at the Ion Beam Center in Helmholtz-Zentrum Dresden-Rossendorf (HZDR) or a 330 kV Unimas ion implanter at Maria Curie-Skłodowska University in Lublin, Poland. For Sn, a solid sputter target was used. P powder was evaporated with a halogen lamp, and Ga was sputtered from a Ga_2O_3 target. All implantations were performed under a sample tilt of 7° and with an active liquid nitrogen cooling system (cold finger). The temperature was measured *in situ* with a thermocouple type-K pressed on an Si reference sample with a tungsten needle. In order to reduce the surface degradation during ion implantation, the samples were kept below -100 °C. The ion beam current was measured with four Faraday cups on the aperture directly in front of the

sample holder. The sample backside was glued on the sample holder with Ag-paste in order to ensure thermal conduction for the sample cooling.

3.3 Pulsed laser annealing (PLA)

For post-growth thermal treatments, the pulsed laser annealing tool Coherent VarioLas ECO 308 5x5 for COMPexPro200 equipped with a 308 nm wavelength XeCl excimer laser with a fixed pulse length of 28 ns was used. A MaxBlack EnergyMax Sensor measured the laser energy. Afterward, the energy was converted into an energy density for the homogeneously irradiated area of 5 x 5 mm². All laser annealing steps are performed under atmospheric conditions with single pulses.

3.4 Flash lamp annealing (FLA)

Flash lamp annealing is used as a post-growth thermal treatment method to recrystallize ion-beam implanted $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys, improve the crystal structure, and perform contact formation. The FLA system is equipped with Xe flash lamps and halogen lamps used as a pre-heating system below the sample (see **appendix 8.27**). The energy of the flash lamps can be controlled by selecting the capacitance (0.2-6 mF per circuit), the inductance (0-18 mH per circuit), and the charging voltage (0 – 4.5 kV) of the capacitor. These parameters define the flash energy and the shape of the light pulse. The energy density on the sample surface is separately measured with a power probe (Fit for Intense Pulse Light (Fit-IPL-R)) of the company “Laserpoint”. The temperature in the sample can be simulated by the software COMSOL [175] by considering the material parameters. The pre-heating system uses halogen lamps and can be controlled by the lamp power and heating time. In order to calibrate the pre-heating system, the temperature was measured on the front surface of a 525 µm thick Si wafer with a thermocouple, and the given value corresponds to the maximum temperature. A 525 µm thick Si wafer was placed between the sample and the underlying quartz window for all FLA annealing steps. The Si wafer was used as a hot plate for pre-heating. All annealings were performed under a N_2 atmosphere.

3.5 Micro-Raman spectroscopy

Micro-Raman spectroscopy was performed on a Horiba LabRam n°1/24 h system equipped with a neodymium-doped yttrium aluminum garnet (Nd:YAG) laser with a wavelength of 532 nm and a liquid-nitrogen-cooled charge-coupled device (CCD) camera. All measurements were performed in ambient conditions and backscattering geometry with a laser power of 1 or 4 mW [187] focused on a circular area with a 1 µm diameter. The phonon spectra were recorded in the wavenumber range of 50 – 550 cm^{-1}

with an accuracy of the measured phonon modes of 0.1 cm^{-1}. The scattered light was diffracted by an 1800 lines / mm grating and finally detected by a liquid nitrogen-cooled charge-coupled device (CCD).

3.6 Rutherford backscattering spectrometry (RBS)

Random (RBS-R) and channeling (RBS-C) experiments were performed at the Ion Beam Center at the HZDR using its 2 MV Van-de-Graaff accelerator. The used He^+ beam had an energy of 1.7 MeV and beam currents between 10 and 20 nA. An aperture with a diameter of about 1 mm was used. Each measurement was performed with a detector angle of 170°. The RBS measurements were used to investigate the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ layer thickness, composition, and quality. The obtained RBS spectra were fitted with the Software SIMNRA [188]. RBS-C was performed along the [001] crystal axis. The RBS channeling yield χ can be calculated by Eq. 3.6 - 1, where A_C is the integrated area under the channeling curve, and A_R is the area under the random curve.

$$\chi = \frac{A_C}{A_R} \qquad \text{Eq. 3.6 - 1}$$

3.7 X-ray diffraction (XRD)

XRD was performed on a Rigaku SmartLab X-ray diffractometer system by Dr. Michael Oehme at the University of Stuttgart and Oliver Steuer at HZDR. Both systems are equipped with a copper (Cu) X-ray source and a Ge two-bounce 2 x (220) monochromator. Phase analysis was performed in Bragg-Brentano geometry using a Ni-filter and a detector in one-dimensional (1D) mode. The powder diffraction file (PDF) version “4+ 2022” from the International Centre for Diffraction Data (ICDD) was used as a database for crystalline phases. High-resolution XRD (HR-XRD) 2 θ-θ scans were carried out on the symmetrical (004) reflections. The reciprocal space maps (RSM) were generated for the (004) and the asymmetrical (224) reflections by scanning the ω and measuring the diffraction intensity in dependence of 2 θ with the detector in 1D single-exposure mode. The alignment for HR-XRD and RSM was performed on the (004) and (224) Si substrate reflections. The lateral and vertical lattice parameters of the epitaxially grown layers were determined from the (224) RSM. Grazing incidence (GI) measurements were performed with a fixed incidence angle ω of 3° and 2 θ detector angle scan between 5 and 90° in zero-dimensional (0D) detector mode without using the monochromator. This technique was used to identify potential polycrystalline contributions or Sn segregations within the single crystal.

3.8 Secondary ion mass spectrometry (SIMS)

Time of flight (ToF) SIMS measurements were conducted by Florian Bärwolf at Leibniz Institute for High Performance Microelectronics (IHP) Frankfurt (Oder) to determine or compare the absolute dopant concentration and distribution before and after annealing. The used IONTOF V tool is equipped with a ToF mass separator. The measurement conditions for the static SIMS investigation of Sn, Ge, Si, Ga, B, P, and Sb can be obtained for each section from Table 3.8 - 1.

Table 3.8 - 1: Overview of the TOF-SIMS measurement parameter used for each section. Sputtering of the doped $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ layers was performed with cesium (Cs^+) and oxygen (O_2^+) ions with an acceleration voltage *E* and a raster area *A*. Bi_1^+ ions are used for the analysis.

Section	Sputtering			Analysis			Mode
	Ion	*E* (eV)	*A* (µm²)	Ion	*E* (kV)	*A* (µm²)	
4.2.4	Cs^+	500	300 × 300	Bi_1^+	25	50 × 50	negative
5.1.4	O_2^+	500	100 × 100	Bi_1^+	15	100 × 100	positive
5.2.4	Cs^+	500	400 × 400	Bi_1^+	15	200 × 200	negative

3.9 Hall-effect measurement

The variable-field Hall-effect measurements in the van-der-Pauw configuration were performed using the HMS 9709A measuring system from LakeShore. Close to the sample corners, 50 - 100 nm thick circular-shaped Au or Ni contacts with a diameter of 1 mm were fabricated by thermal evaporation. The magnetic flux density (*B*) was varied between -5 and 5 T.

Room temperature Hall-effect measurement in van-der-Pauw configuration on an HMS-3000 setup with a magnetic field of ± 0.51 T was used as a fast pre-screening method to judge the carrier concentration after annealing. A special sample holder with Au contacts was used.

3.10 Transmission electron microscopy (TEM)

TEM was performed by Dr. René Hübner at the Ion Beam Center in HZDR. $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys of the as-grown and annealed states, as well as the final transistors, were imaged in cross-sectional geometry using a Titan 80-300 microscope (FEI) operated at an accelerating voltage of 300 kV. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) imaging and spectrum imaging analysis based on energy-dispersive X-ray spectroscopy (EDXS) were performed at 200 kV with a Talos F200X microscope equipped with a Super-X EDX detector system (FEI). High-resolution TEM images were recorded to evaluate the layer crystallinity, and Fast Fourier Transformed (FFT) HR-TEM images were used for phase conformation.

Prior to TEM analysis, the specimen mounted in a high-visibility low-background holder was placed for 10 s into a Model 1020 Plasma Cleaner (Fischione) to remove potential contamination.

3.11 Positron annihilation spectroscopy (PAS)

The positron lifetime experiments were performed at the mono-energetic positron spectroscopy (MePS) beamline, which is a beamline of the radiation source ELBE (Electron Linac for beams with high Brilliance and low Emittance) at HZDR [189]. Positrons were accelerated and monoenergetically implanted into samples in the range between E_p = 1 - 10 keV for positron annihilation lifetime spectroscopy (PALS) and E_p = 0.05 - 35 keV for Doppler broadening variable energy positron annihilation spectroscopy (DB-VEPAS), which realizes depth profiling. A mean positron implantation depth was approximated using a simple material density ρ dependent equation Eq. 3.11 - 1 [190].

$$< d > = \frac{3.6}{\rho} E_p^{1.62} \qquad \text{Eq. 3.11 - 1}$$

<*d*> is an approximation of the depth and cannot be treated as an absolute measure since it does not account for positron diffusion. However, it gives a reliable depth estimation for materials with large defect concentrations because of a limited positron diffusion length. A digital lifetime $CrBr_3$ scintillator detector operated by a homemade software, utilizing a SPDevices ADQ14DC-2X digitizer with 14-bit vertical resolution and 2 GS/s horizontal resolution, was used (the overall time resolution was down to about 230 ps) [191]. The resolution function required for spectrum analysis was composed of two Gaussian functions with distinct intensities depending on the positron implantation energy and appropriate relative shifts. All spectra contain at least 5 x 10^6 counts. The lifetime spectra *D(t)* were analyzed as a sum of time-dependent exponential decays according to equation Eq. 3.11 - 2, convoluted with the spectrometer timing resolution [192] using the non-linearly least-squared-based package PALSfit fitting software [193].

$$D(t) = \sum_N \frac{I_N}{\tau_N} e^{\frac{-t}{\tau_N}} \qquad \text{Eq. 3.11 - 2}$$

The indices *N* correspond to the number of discrete lifetime components (defect sizes, types) in the spectra with individual lifetimes τ_N and their relative intensities I_N. A commercial undoped bulk Ge substrate was used as a reference for DB-VEPAS and VEPALS. The measurements were performed by Oliver Steuer and Dr. Maciej Oskar Liedke. The experimental results were supported with ATomic SUPerposition (ATSUP) calculations carried out by Dr. Maik Butterling.

3.12 Cleanroom

All wet chemical etchings with hydrofluoric acid (HF) and phosphoric acid (H_3PO_4) were performed in a class 100 cleanroom at HZDR.

4 Post-growth thermal treatments of $Ge_{1-x}Sn_x$ alloys

Low-temperature growth of hetero-epitaxial $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ layers can cause strain and undesired defects (see **section 2.2**). Therefore, post-growth thermal treatments might be an attractive approach to improve the layer quality. However, equilibrium-like long thermal treatments above the eutectic temperature of the Sn-containing alloy can lead to β-Sn segregation. As introduced in **section 2.4**, one avenue of escape could be ultrashort non-equilibrium annealings. **Section 4.1** investigates the influence of post-growth nanosecond pulsed laser annealing (PLA) on the structural properties of MBE-grown $Ge_{0.89}Sn_{0.11}$. The impact of post-growth millisecond flash lamp annealing (FLA) on MBE-grown $Ge_{1-x}Sn_x$ (x = 9, 12, and 16 at.%) alloys is discussed in **section 4.2**.

4.1 Post-growth pulsed laser annealing

Nanosecond pulsed laser annealing is a widely used method for non-equilibrium thermal treatments. In the last few years, many research groups have studied the influence of PLA on $Ge_{1-x}Sn_x$ alloys [126, 128, 182, 194]. In the scope of this work, two publications contributed to a general understanding of this post-growth thermal treatment approach. The results presented in this section are partial excerpts of the published results in J. Phys. Condens. Matter [128] and J. Phys. Condens. Matter [129]. It is shown that the post-growth PLA of $Ge_{1-x}Sn_x$ on Ge buffered Si can lead, under certain conditions, to a fully strain-relaxed $Ge_{1-x}Sn_x$ layer. The influence of the PLA process on the microstructural, electrical, and optical properties of the $Ge_{1-x}Sn_x$ alloys was studied by RBS-R/C, cross-sectional TEM, XRD, μ-Raman, low-temperature photo-reflectance (LT-PR) spectroscopies, PALS and Hall-effect measurements. Finally, the strain-relaxed $Ge_{1-x}Sn_x$ layer was used as a buffer layer for a new MBE growth of stain-relaxed high-quality $Ge_{1-x}Sn_x$.

4.1.1 Material fabrication and PLA annealing

$Ge_{1-x}Sn_x$ layers with an Sn concentration of 11% were epitaxially grown on (100) oriented 4-inch p-type Si substrates with a sheet resistance R_s = 10 – 20 Ωcm by MBE. The MBE process is performed as introduced in **section 3.1**. After the *in situ* thermal desorption step at T_S = 900 °C, a 50 nm thick Si-VS layer was grown at a substrate temperature of T_S = 600 °C. Next, the substrate temperature was reduced to T_S = 330 °C, and a 100 nm thick Ge layer was grown. Afterward, an *in situ* thermal annealing step at T_S = 830 °C for a duration of t = 5 min allows threading dislocations to annihilate. This Ge layer is used as a virtual Ge substrate (Ge-VS). An additional 300 nm thick Ge-buffer layer was grown

on the top and *in situ* annealed at T_S = 750 °C for t = 5 min. Finally, a 290 nm thick $Ge_{0.89}Sn_{0.11}$ layer was grown on top of the Ge-buffer layer at T_S = 120 °C. The schematic of the fabricated layer stack can be seen in Fig. 4.1 - 1 a). Afterward, PLA with the setup presented in **section 3.3** and energy densities E_d between 0.15 and 0.6 J cm^{-2} was performed as depicted in Fig. 4.1 - 1 b).

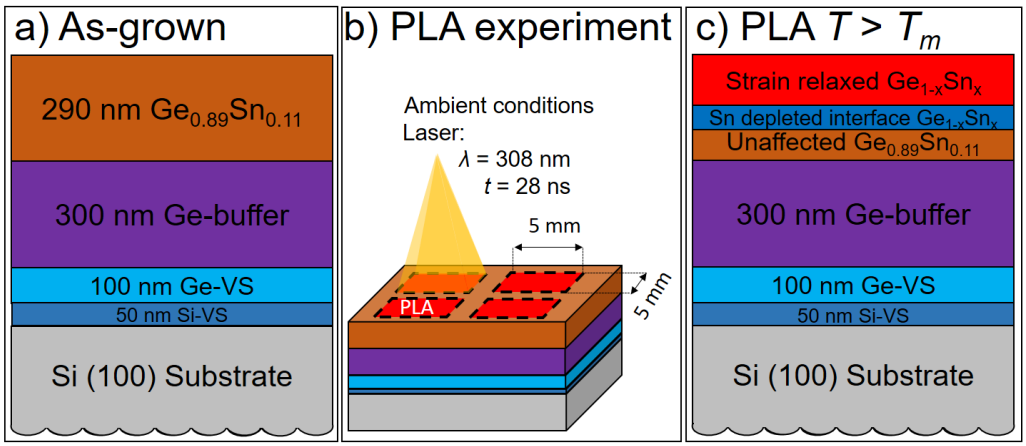


Fig. 4.1 - 1: Schematical cross-section of the MBE-grown layer stack on Si substrate with the $Ge_{0.89}Sn_{0.11}$ top layer in the as-grown state a). Schematic of the experimental approach by prost-growth PLA b). Schematical cross-section of the post-growth PLA-treated layer stack at annealing conditions above the melting temperature T_m c).

4.1.2 Microstructural investigation

RBS-R/C measurements of the as-grown and PLA samples were performed to investigate changes in the elemental distribution and crystal quality as a function of the energy density E_d. The results of the as-grown state and representative PLA samples are shown in Fig. 4.1 - 2 a). RBS-R results of all annealed states from this section and general information to understand RBS-R spectra can be found in **appendix 8.2**. The as-grown $Ge_{0.89}Sn_{0.11}$ layer shows a homogeneous distribution of Sn in RBS-R. The RBS-C spectra are aligned to the [001] crystal axis of the $Ge_{1-x}Sn_x$ layer and show for the $Ge_{0.89}Sn_{0.11}$ as-grown state a decreasing intensity in the Sn contribution towards the sample surface. This can be explained by an improvement in layer quality during the growth process and a generally relatively high channeling yield (absence of a surface channeling peak).

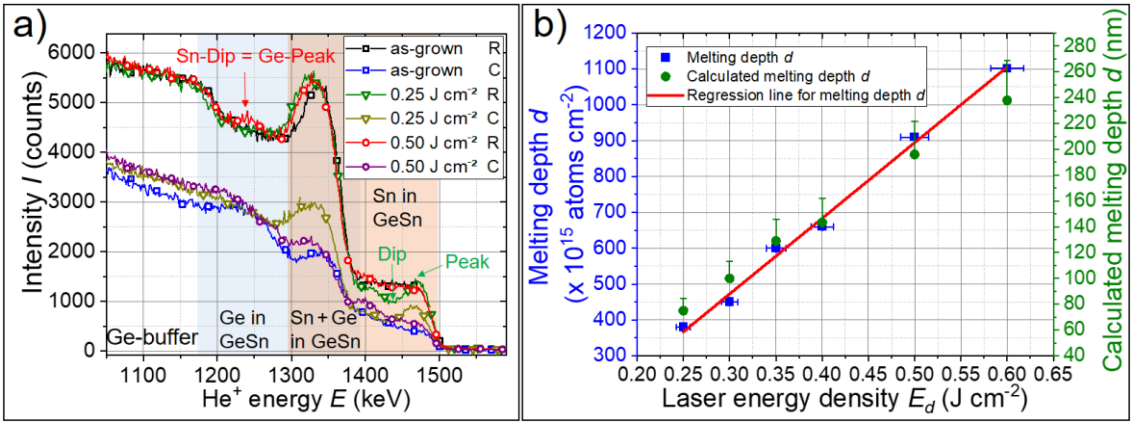


Fig. 4.1 - 2: RBS-R/C before and after PLA with 0.25 and 0.5 J cm^{-2} a). The Sn signal of the $Ge_{1-x}Sn_x$ layer contributes to backscattering energies between 1300 keV and 1500 keV (orange background). The Ge contribution of the $Ge_{1-x}Sn_x$ layer (blue background) is between 1180 keV and 1380 keV and overlaps the Sn contribution for high energies. Below 1180 keV is the Ge contribution of the pure Ge-buffer layer (white background). The dip in the Sn contribution, marked with the corresponding curve color, was used to determine the physical and calculated thicknesses of the molten $Ge_{1-x}Sn_x$ layer as a function of the energy density E_d of the laser pulses in Fig. 4.1 - 2 b).

The channeling yield χ is calculated by Eq. 3.6 - 1 and presented in Table 4.1 - 1 for the different annealing states. It is visible that the channeling yield of the Ge fraction in the as-grown $Ge_{1-x}Sn_x$ layer is higher than the Sn fraction. This effect is most likely related to the different depth regions of the integrated signal. The signal of Sn is obtained from the surface of the $Ge_{1-x}Sn_x$ layer, whereas the integrated area of Ge is close to the bottom of the $Ge_{1-x}Sn_x$ layer.

Table 4.1 - 1: Calculated channeling yields of Sn χ_{Sn} and Ge χ_{Ge} of the $Ge_{0.89}Sn_{0.11}$ alloy before and after PLA with energy densities E_d between 0.15 and 0.60 J cm^{-2}. For χ_{Sn}, the energy integration interval is between 1400 and 1475 keV, and for χ_{Ge}, it is between 1230 and 1280 keV, respectively. Owing to their inconvenient spectra overlap (highlighted by the overlap of the background filling in Fig. 4.1 - 2 a)), it is impossible to select the same investigation depth for a direct comparison of χ_{Ge} and χ_{Sn}.

Sample	Integration range (keV)	As-grown (%)	0.15 J cm^{-2} (%)	0.20 J cm^{-2} (%)	0.25 J cm^{-2} (%)	0.30 J cm^{-2} (%)	0.35 J cm^{-2} (%)	0.40 J cm^{-2} (%)	0.50 J cm^{-2} (%)	0.60 J cm^{-2} (%)
χ_{Sn}	1400 – 1475	42.1	43.2	46.7	66.6	69.0	66.4	59.2	55.7	55.1
χ_{Ge}	1230 – 1280	59.8	60.4	53.7	61.1	65.7	65.8	61.6	60.4	68.9

PLA with E_d = 0.15 J cm^{-2} is below the melting temperature and shows no significant change in the elemental distribution (see Fig. 8.2 - 1) or in the channeling yield (see Table 4.1 - 1). In the case of samples annealed with E_d = 0.2 J cm^{-2}, a slightly lower Sn concentration and a slightly higher χ_{Sn} are observed close to the surface. This is attributed to the first elemental redistributions when the selected E_d approaches temperatures close to the melting threshold. For E_d > 0.2 J cm^{-2}, a peak and dip between 1180 keV and 1500 keV of the Ge and Sn RBS-R spectra contributions are visible (see arrows in Fig. 4.1 - 2 a). This indicates Sn and Ge redistribution. In general, PLA above

the melting point divides the $Ge_{1-x}Sn_x$ layer into three parts as illustrated in Fig. 4.1 - 1 c): i) the molten top layer, ii) an Sn-depleted zone, and iii) an almost unaffected remaining $Ge_{0.89}Sn_{0.11}$ layer, which is similar to the as-grown state. The dip represents the Sn-depleted interface of zone ii), which will be clearly observed in the TEM images presented below (see Fig. 4.1 - 3 e)). The comparison of χ in Table 4.1 - 1 shows that post-growth PLA above the melting point increases χ, which means a reduced layer quality compared to the as-grown state. This can be caused by atoms in the interstitial sides, the formation of Sn-Sn dimers, small Sn-nanocrystals, or a combination of those effects. The maximum χ_{Sn} is observed for E_d = 0.25 J cm^{-2} since the integration range coincides with the Sn peak in Fig. 4.1 - 2 a). However, with increasing E_d, the layer quality close to the surface is gradually improved (see χ_{Sn} in Table 4.1 - 1). To understand this effect, the melting depth was calculated by the dips in the Sn spectra with the software SIMNRA [188] and is plotted in Fig. 4.1 - 2 b). For this, the mass density in $Ge_{1-x}Sn_x$ and the simulated RBS-R spectra of each measurement were considered. The almost linear relationship between melting depth d and E_d allows the control of laser penetration depth by adjusting E_d. However, the conversion from the extracted melting depth in atoms cm^{-2} by SIMNRA into melting depth in nm leads to about 13% thinner $Ge_{1-x}Sn_x$ layers. This difference was determined by comparing the RBS-R in Fig. 4.1 - 2 a) and TEM results in Fig. 4.1 - 3. The error comes from the not well-determined mass density of the $Ge_{1-x}Sn_x$ alloy grown by MBE, mass approximation by Vegard's law, and roughness. After melting, the mass density becomes inconstant due to the atom and strain redistributions. Nevertheless, a clear χ_{Sn} reduction close to the sample surface is observed with increasing E_d, which is related to a more defined structure after long-range liquid phase epitaxy.

The microstructure and element composition of the as-grown and PLA samples were investigated using cross-sectional TEM-based analysis and XRD. Fig. 4.1 - 3 a) depicts a representative bright-field TEM image of the $Ge_{0.89}Sn_{0.11}$ layer grown on a Ge-buffered Si substrate. While the Ge-VS and buffer are characterized by a uniform contrast (besides the presence of some dislocations close to the Si substrate), the $Ge_{0.89}Sn_{0.11}$ layer shows a columnar signature, particularly in the upper three-quarters of the film. Compared with the EDXS-based element analysis in Fig. 4.1 - 3 b), this columnar contrast arises from a slightly varying Sn distribution in the as-grown $Ge_{0.89}Sn_{0.11}$ layer. This interpretation is also supported by EDXS horizontal line scans, shown in Fig. 8.3 - 1 f) in **appendix 8.3**. Regarding the microstructure, the $Ge_{1-x}Sn_x$ film grows epitaxial on the Ge virtual substrate, as derived from the fast Fourier transform (FFT, depicting a $[1\bar{1}0]$ zone axis pattern) of the representative high-resolution (HR-TEM)

image in Fig. 4.1 - 3 c). At the border regions between the columns, there are no defects visible.

After PLA with E_d = 0.5 J cm^{-2}, the columnar signature changed and the sample surface morphology was restructured (Fig. 4.1 - 3 d)). Comparing the superimposed Sn and Ge element maps in Fig. 4.1 - 3 b) and Fig. 4.1 - 3 e), it can be concluded that the Sn redistribution in the molten layer observed in RBS-R is divided into two phenomena. On the one hand, the Sn-dip in Fig. 4.1 - 2 a) belongs to an Sn-depleted layer at the interface between the molten layer and an almost unaffected $Ge_{0.89}Sn_{0.11}$ bottom layer. This conclusion is also supported by vertical EDXS line scans in Fig. 8.3 - 1 e) in **appendix 8.3**. On the other hand, the Sn-peak is a superposition of the slightly Sn-depleted $Ge_{1-x}Sn_x$ matrix with Sn-rich clusters and filaments. The filaments reaching up to the sample surface and might be related to the observed texture or already existing threading dislocations in the as-grown state. It should be mentioned that a wall-like structure, having its plane normal perpendicular to the normal of the TEM lamella plane, may also appear as filament in a two-dimensional TEM-based projection image. Similar filament structures have been recently observed after PLA of CVD-grown $Ge_{0.89}Sn_{0.11}$ [126] with λ = 355 nm for t = 6 ns, but their origin is still unclear. For instance, such filament structures were discussed by Narayan [172] for highly indium-, gallium-, and iron-doped Si after PLM. He concluded that if the non-equilibrium solubility of the alloy exceeds a certain value, the solid-liquid interface becomes unstable, and the structure experiences a cellular breakdown during ultra-fast solidification. However, there are some reasons against this theory, as discussed in ref. [126] and [142]. The Sn-rich filaments in the present study are still part of the $Ge_{1-x}Sn_x$ crystal structure. Assuming that the filaments might be an early phase separation stage, there should be a significant increase in the Sn concentration towards the surface, which is not visible in Fig. 4.1 - 3 e). Furthermore, Abdi et al. reported an enhanced defect concentration around the Sn-rich filaments and assumed a combination of pipe diffusion and spinodal decomposition as the origin of the filaments [126]. In fact, our filament in Fig. 4.1 - 3 f) may also contain some defect structures.

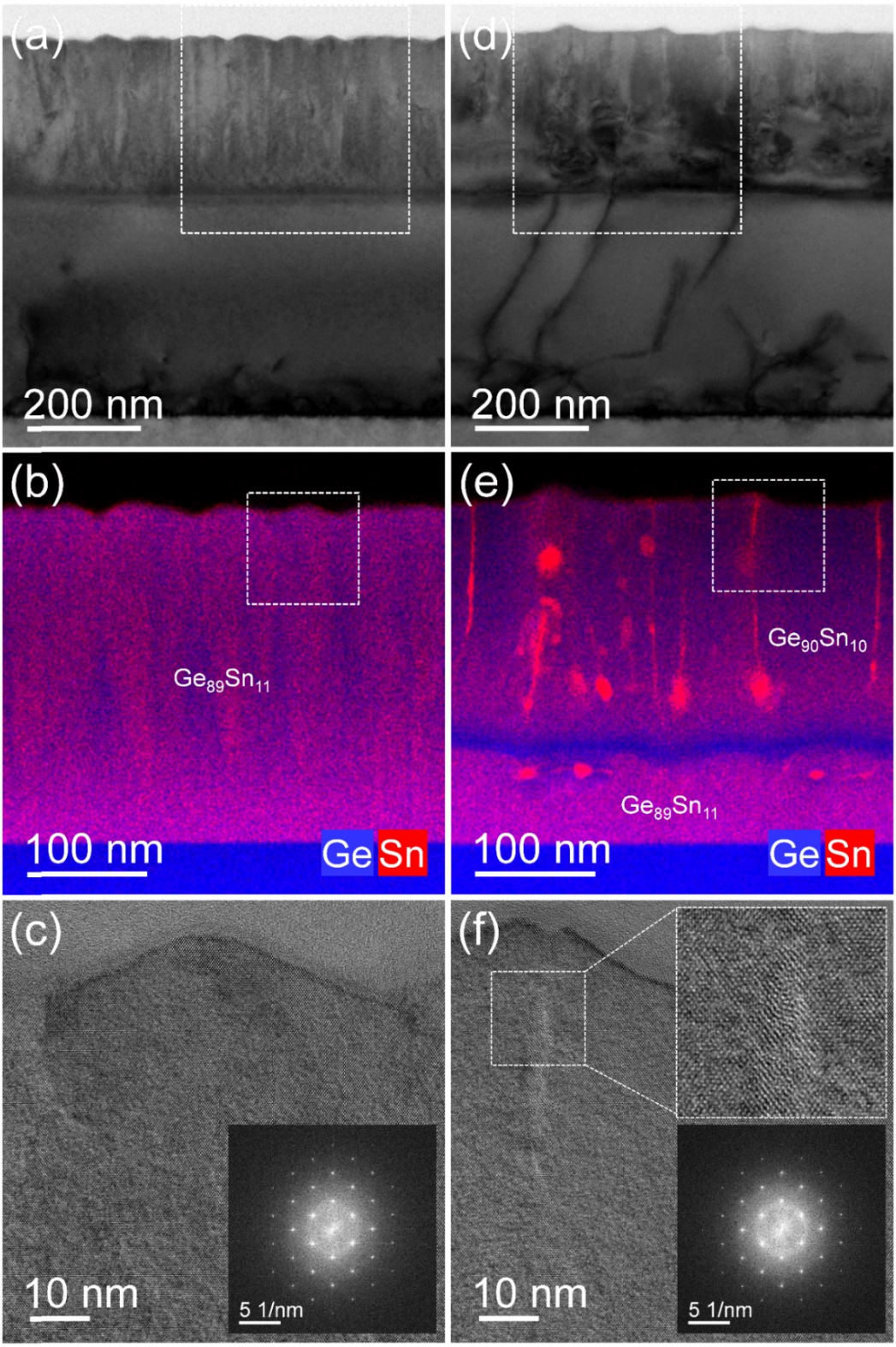


Fig. 4.1 - 3: Cross-sectional TEM-based analysis of the as-grown $Ge_{0.89}Sn_{0.11}$ sample a) - c) and after PLA treatment with an energy density of 0.5 J cm^{-2} d) - f). Representative bright-field TEM images a), d). Superimposed Ge (blue) and Sn (red) element distributions in b) and e) were obtained for the regions marked with a dashed white square in a) and d). The given compositions were determined by EDXS-based quantification. HR-TEM images in c) and f) for the regions marked with a dashed white square in b) and e). In each panel, the corresponding fast Fourier transformation of the complete HR-TEM image is shown in the lower right corner. In panel f), the enlarged view of the Sn-enriched location is shown as an inset in the upper right corner.

Apart from the filaments, the microstructure of the $Ge_{0.90}Sn_{0.10}$ matrix close to the sample surface seems to be homogeneous and has a comparable composition ($Ge_{0.90}Sn_{0.10}$) and similar structural properties as the as-grown sample, i.e., it is of single-crystalline nature. In particular, the FFT analysis of the HR-TEM image in Fig. 4.1 - 3 f) leads to a $[1\bar{1}0]$ zone axis pattern comparable to the one given in the inset of Fig. 4.1 - 3 c). However, there may be some defect structures at the Sn-enriched location, as exemplarily shown in the enlarged part of the HR-TEM image depicted in the upper right inset of Fig. 4.1 - 3 f). Additionally to the Sn-rich clusters, many defect structures are visible in the PLA-treated microstructure between the $Ge_{1-x}Sn_x$/Ge interface up to about 100 nm below the $Ge_{1-x}Sn_x$ top surface (see Fig. 4.1 - 3 d) or Fig. 8.3 - 1 d)). The presence of these defects after PLA might be related to strain relaxation, which comes with the formation of misfit dislocation networks and threading dislocations, as discussed below in **section 4.1.3**.

The formation of β-Sn segregations was studied by GI-XRD 2 θ scans presented in Fig. 4.1 - 4 a). The fixed X-ray incident angle *ω* at 3° in combination with the broad detector angle *2θ* scan allows the identification of additional crystal structures, which would appear as distinct peaks in the spectra. Indeed, the scans of the as-grown and after PLA with 0.5 J cm^{-2} state have one sharp peak at about 38.08° and 38.18°, respectively. This peak might be obtained from some inclusion of small nanocrystals or a textured growth of $Ge_{0.89}Sn_{0.11}$ visualized in the cross-sectional TEM image taken from the as-grown sample (see Fig. 4.1 - 3 a)). Other annealing states do not show the peak at $2\theta \approx 38°$ at all. In order to exclude Sn-segregations, the Powder Diffraction File database entries of α-Sn and β-Sn were checked for conformity. However, the data did not match the peak at around 38° as visible for β-Sn in Fig. 4.1 - 3 a). On the contrary, a match with the peak at 44.9° could be identified for the as-grown state and after PLA at 0.5 J cm^{-2}. Nevertheless, the very low intensity close to the noise level, the lack of visible Sn segregations in the TEM images of the as-grown state (see Fig. 8.3 - 1 a)), and the absence of the high-intensity β-Sn-related reflections at around 30.7° and 32.1° in Fig. 4.1 - 4 a) suggest no Sn segregations. The absence of other well-distinguishable peaks confirms the epitaxial growth of $Ge_{1-x}Sn_x$ alloy on the Ge-buffer.

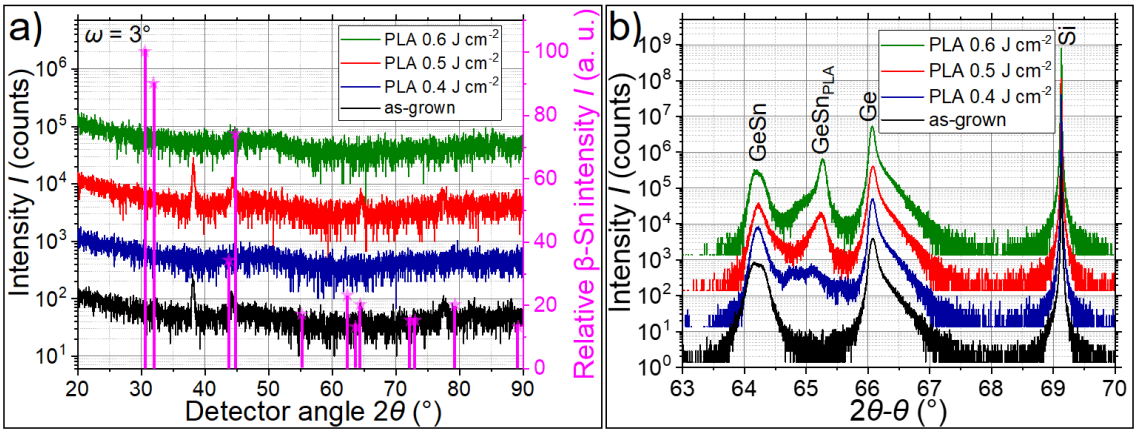


Fig. 4.1 - 4: Grazing incidence GI-XRD a) and (004) HR-XRD b) of the $Ge_{1-x}Sn_x$ sample in as-grown state and after PLA with energy densities of 0.4, 0.5 and 0.6 J cm^{-2}. In order to distinguish between the curves, a visualization offset with increasing energy densities is applied in a) and b). The expected β-Sn peak positions and their relative intensities obtained from ref. [76] are added in a).

Fig. 4.1 - 4 b) shows the HR-XRD results obtained from the (004) planes in the as-grown state and after PLA with energy densities of 0.4, 0.5, and 0.6 J cm^{-2}. The as-grown state exhibits three XRD reflections located at about 69.13°, 66.07°, and 64.18° corresponding to the Si substrate, Ge (buffer and VS), and the strained $Ge_{0.89}Sn_{0.11}$, respectively. After PLA at 0.5 J cm^{-2}, the original $Ge_{0.89}Sn_{0.11}$ reflection is divided into two peaks. The GeSn reflection at 64.22° belongs to the not molten deeper $Ge_{0.89}Sn_{0.11}$ layer, and the $GeSn_{PLA}$ reflection at 65.24° is related to the molten top layer of $Ge_{1-x}Sn_x$. The sample annealed with 0.4 J cm^{-2} shows a similar peak separation, but the PLA-affected layer is thinner, which leads to a lower intensity. This correlation between the $GeSn_{PLA}$ reflection intensity and the increase in the PLA-affected layer thickness matches qualitatively the PLA at E_d = 0.6 J cm^{-2} results and findings from Fig. 4.1 - 2 b). Furthermore, the shift of the $GeSn_{PLA}$ reflection towards higher diffraction angles indicates a reduced out-of-plane lattice parameter, which can be related to strain relaxation.

4.1.3 Strain relaxation and optical properties

The strain condition of the samples is investigated by XRD-RSM and μ-Raman spectroscopy. Fig. 4.1 - 5 shows the reciprocal space mapping results of as-grown a), PLA 0.4 J cm^{-2} b), PLA 0.5 J cm^{-2} c), and PLA 0.6 J cm^{-2} d) samples. The maps include (224) reflections of the Si substrate (not shown), Ge buffer (Ge), as-grown $Ge_{0.89}Sn_{0.11}$ (GeSn), and $Ge_{1-x}Sn_x$ after PLA ($GeSn_{PLA}$). In general, a reflection position below the strain relaxation line indicates compressive strain and above tensile strain. The as-grown $Ge_{0.89}Sn_{0.11}$ layer is highly compressively strained and some tail regions of its reflection match the pseudomorphic line. Hence, the bottom $Ge_{0.89}Sn_{0.11}$ layer can be considered as pseudomorphically grown on the Ge-buffer. After PLA with 0.4 J cm^{-2}, the additional $GeSn_{PLA}$ reflection appeared close to the strain relaxation line. The intensity of the

$GeSn_{PLA}$ reflection increases with increasing PLA E_d, which correlates with the thickness-dependent intensity (see Fig. 4.1 - 2 b) and Fig. 4.1 - 4 b)). For quantitative analysis, the (224) in-plane q_x and out-of-plane q_z reciprocal lattice parameters of the Ge, GeSn, and the $GeSn_{PLA}$ were extracted by a fitting procedure, converted into the real-space in-plane a_{II} and out-of-plane $a_{\perp}$ lattice parameter and the in-plane strain $\varepsilon_{II,XRD}$ was calculated by Eq. 4.1 - 1. Details about the data extraction, calculation procedure for a_{II}, $a_{\perp}$, the relaxed lattice parameter a_0, alloy composition, and the in-plane strain $\varepsilon_{II,XRD}$ calculation are explained in **appendix 8.4**.

$$\varepsilon_{II,XRD} = \frac{(a_{II} - a_0)}{a_0} \qquad \text{Eq. 4.1 - 1}$$

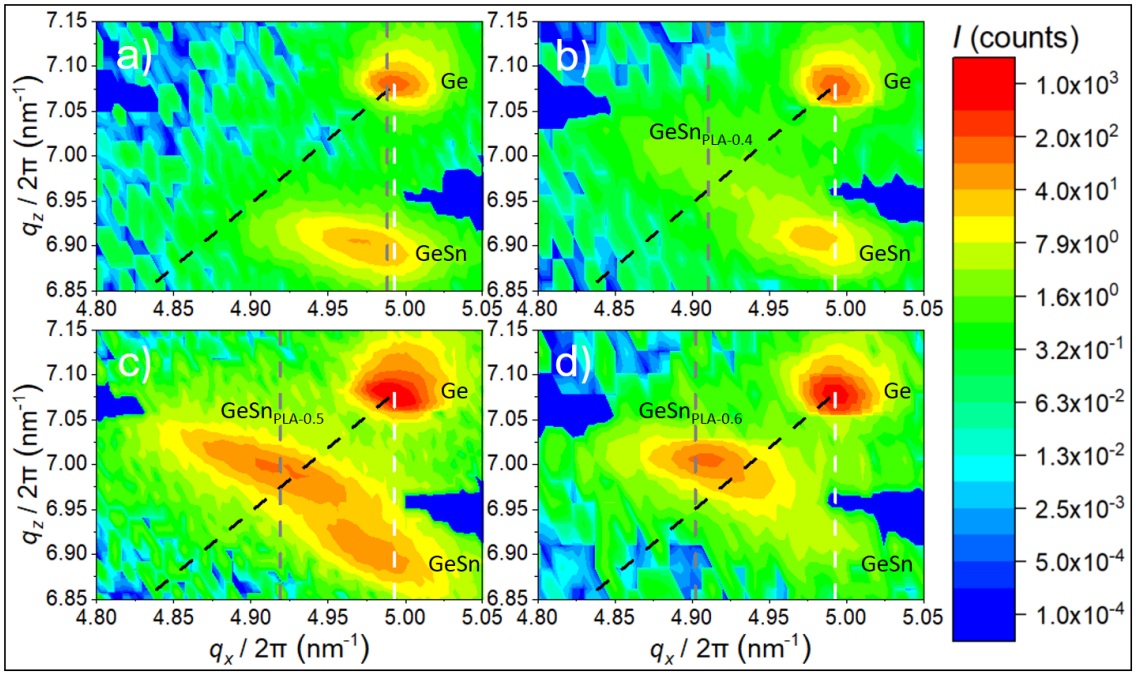


Fig. 4.1 - 5: (224) XRD-RSM with in-plane q_x and out-of-plane q_z reciprocal lattice parameters for as-grown a) and annealed samples with an energy density of 0.4 J cm^{-2} b), 0.5 J cm^{-2} c), and 0.6 J cm^{-2} d). Each map is equipped with a strain relaxation line (dashed black), pseudomorphic line (dashed white), and the reciprocal lattice parameter line (dashed grey) obtained from µ-Raman analysis in Table 4.1 - 3 and converted by applying Eq. 4.1 - 1.

The obtained values are summarized in Table 4.1 - 2. The a_{II} and $a_{\perp}$ for the as-grown Ge-VS/buffer are 5.665 and 5.6503 Å, respectively, while the tabulated value for relaxed Ge is 5.6575 Å [195]. This means that the Ge-VS/buffer is slightly tensile strained by $\varepsilon_{II,XRD}$ = 0.09%. In the as-grown sample, the GeSn reflection is shifted to a larger a_{II} value compared to the Ge-VS/buffer reflection. The in-plane lattice parameter of as-grown GeSn is a_{II} = 5.693 Å, but the calculated value of a_0 for relaxed $Ge_{0.89}Sn_{0.11}$ is 5.7502 Å. Hence, our $Ge_{0.89}Sn_{0.11}$ layer in as-grown state is under biaxial compressive strain $\varepsilon_{II,XRD}$ = -1% because of the pseudomorphic growth of $Ge_{0.89}Sn_{0.11}$ on the Ge-buffer. This in-plane compressive strain results in an out-of-plane elongated lattice parameter of $a_{\perp}$ = 5.7944 Å (tensile strain) for the as-grown $Ge_{0.89}Sn_{0.11}$ due to volume constancy.

After PLA with 0.5 J cm^{-2}, the a_{II} and $a_{\perp}$ of the top layer are 5.748 and 5.7190 Å, respectively, while the lattice parameters of the non-molten GeSn layer remain almost unchanged. The in-plane strain changes from compressive $\varepsilon_{II,XRD}$ = -1% in the as-grown state to tensile $\varepsilon_{II,XRD}$ = 0.28% after PLA with an energy density of 0.5 J cm^{-2} and to $\varepsilon_{II,XRD}$ = 0.38% after PLA at 0.6 J cm^{-2}. The $Ge_{0.904}Sn_{0.096}$ layer after PLA with 0.4 J cm^{-2} is still in-plane compressive strained with $\varepsilon_{II,XRD}$ = -0.03%, but the strain is reduced compared to the as-grown state.

Table 4.1 - 2: In-plane a_{II} and out-of-plane $a_{\perp}$ real space lattice parameters obtained by peak fitting of Fig. 4.1 - 5 and data conversion by Eq. 8.4 - 1 and Eq. 8.4 - 2. Calculated Sn concentrations c_{Sn}, relaxed lattice parameter a_0, and in-plane strain $\varepsilon_{II,XRD}$ calculated for as-grown and PLA-treated $Ge_{1-x}Sn_x$ samples. $Ge_{as\text{-}grown}$ and $GeSn_{as\text{-}grown}$ belong to the material in the as-grown state. The results of GeSn pertain to the unaffected GeSn bottom layer. $GeSn_{PLA\text{-}0.4}$, $GeSn_{PLA\text{-}0.5}$, and $GeSn_{PLA\text{-}0.6}$ are samples annealed with 0.4, 0.5, and 0.6 J cm^{-2}, respectively. The accuracy of the out-of-plane lattice parameter $a_{\perp}$ is ± 0.0001 Å and in-plane a_{II} ± 0.001 Å.

	c_{Sn} (at.%)	a_{II} (Å)	$a_{\perp}$ (Å)	a_0 (Å)	$\varepsilon_{II,XRD}$ (%)
$Ge_{as\text{-}grown}$	-	5.665	5.6503	5.6575	0.09
$GeSn_{as\text{-}grown}$	11.1 ± 0.5	5.693	5.7944	5.7502	-1.00
GeSn	10.2 ± 0.5	5.681	5.7907	5.7430	-1.08
$GeSn_{PLA\text{-}0.4}$	9.6 ± 0.5	5.736	5.7394	5.7380	-0.03
$GeSn_{PLA\text{-}0.5}$	10.2 ± 0.5	5.748	5.7190	5.7316	0.28
$GeSn_{PLA\text{-}0.6}$	8.9 ± 0.5	5.754	5.7149	5.7318	0.38

µ-Raman measurements and calculations were carried out to investigate the strain relaxation at lower laser energy densities close to the sample surface. The normalized µ-Raman spectra in Fig. 4.1 - 6 are obtained from the $Ge_{1-x}Sn_x$ samples before and after PLA and a pure Ge reference. The results describe the surface-related properties since the penetration depth of the green laser (λ = 532 nm) in Ge, used for sample excitation in the µ-Raman, is approximately 20 nm from the surface [196]. Due to alloying with Sn, the penetration depth of the green laser in the $Ge_{1-x}Sn_x$ layer can be even smaller.

The Ge-Ge optical phonon mode in relaxed Ge $\omega_{p,Ge}$ is at 300.5 ± 0.1 cm^{-1}, as visible for the Ge reference in Fig. 4.1 - 6 [197]. The peak position of the phonon mode in Ge can be shifted to lower or higher wavenumbers due to different phenomena like strain, alloying, disorder, or phonon-plasmon interaction in heavily doped semiconductors. In general, compressive strain shifts the phonon mode to higher wavenumbers, while tensile strain causes a red shift [128, 198]. Alloying Ge with heavier elements like Sn shifts the phonon mode to lower wavenumbers [199]. Therefore, µ-Raman spectroscopy is a contactless and non-destructive method to investigate the changes in composition and strain in solids. In analyzing the phonon spectra, the coexistence of different phenomena that can compensate for the changes by each other has to be taken into account. On the other hand, the pseudomorphic growth of $Ge_{0.89}Sn_{0.11}$ on Ge by MBE

causes in-plane biaxial compressive strain. Therefore, the peak position of the as-grown $Ge_{0.89}Sn_{0.11}$ layer is located at 296.6 cm^{-1}, instead of $\omega_{p,Ge0.89Sn0.11}$ = 291.3 cm^{-1} according to the theoretical calculation (see the vertical dashed line in Fig. 4.1 - 6). The PLA-treated sample with 0.15 J cm^{-2} shows results similar to those of the as-grown state. Hence, PLA below the melting point neither changes the strain nor causes elemental redistribution (see Fig. 8.2 - 1). The first significant peak shift to lower wavenumbers is observed for 0.2 J cm^{-2}, which indicates the first strain relaxation and elemental redistributions at energy densities close to the melting point. After 0.25 J cm^{-2}, a massive peak shift below the theoretical peak position is visible. This can be explained by an increased Sn concentration on the sample surface (see the highlighted RBS-R Sn peak in Fig. 4.1 - 2 a)) in combination with an effective strain relaxation. All other samples annealed with a pulsed laser energy density higher than 0.25 J cm^{-2} show the main phonon mode at about 291 ± 1 cm^{-1}, which is close to the theoretical peak position of strain-relaxed $Ge_{0.89}Sn_{0.11}$.

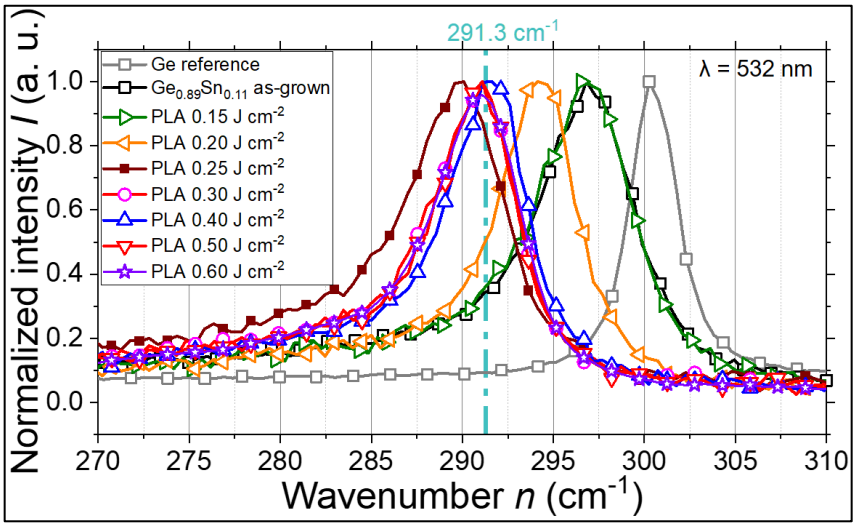


Fig. 4.1 - 6: Normalized µ-Raman spectra*4 for the Ge-Ge optical phonon mode of the as-grown $Ge_{0.89}Sn_{0.11}$ and PLA-treated $Ge_{1-x}Sn_x$ alloys with energy densities of 0.15, 0.20, 0.25, 0.30, 0.40, 0.50 and 0.60 J cm^{-2}. The Raman spectrum of Ge is shown for reference. The peak position of each spectrum was fitted with the Lorentzian peak function. The vertical light blue dashed line highlights the theoretically expected peak position of strain-relaxed $Ge_{0.89}Sn_{0.11}$ at 291.3 cm^{-1}. The Ge-Ge peak broadening towards lower wavenumbers is caused by a disorder mode [200].

The in-plane strain $\varepsilon_{II,Raman}$ can be calculated by Eq. 4.1 - 2, where $\omega_{p,measurement}$ is the measured phonon frequency of the $Ge_{1-x}Sn_x$ alloy (see Table 4.1 - 3), b_d is the disorder parameter, which is reported as b_d = -83.11 [201], b_ε is the strain coefficient, which is reported as b_ε = -374.53 [201] and c_{Sn} is the Sn concentration of the $Ge_{1-x}Sn_x$ alloy. More

*4 The full Raman spectra also contains phonon modes of Ge-Sn (250-260 cm^{-1}) and Sn-Sn (170 - 180 cm^{-1}). However, both peaks are weak and broad, which does not allow a reliable peak fit. Fortunately, all three observed phonon modes show a very similar dependence on the Sn concentration and strain on the peak position [200].

details about the strain calculation can be obtained in **appendix 8.5**. The analysis results for the as-grown state and the PLA states are shown in Table 4.1 - 3.

$$\varepsilon_{II,Raman} = \frac{\omega_{P,measurement} - \omega_{p,Ge} - b_d \cdot c_{Sn}}{b_\varepsilon} \qquad \text{Eq. 4.1 - 2}$$

Table 4.1 - 3: Strain calculation results using the Ge-Ge phonon mode of the $Ge_{1-x}Sn_x$ alloys. $\omega_{p,measurement}$ is the obtained mode position after Lorentzian fitting of the spectra presented in Fig. 4.1 - 6. The Sn concentration is determined by XRD $c_{Sn,XRD}$ and RBS $c_{Sn,RBS}$. The "black" concentrations were taken into account for in-plane Raman strain $\varepsilon_{II,Raman}$ calculations. $\varepsilon_{II,XRD}$ is reprinted from Table 4.1 - 2.

Sample	$\omega_{p,measurement}$ (cm^{-1})	$c_{Sn,XRD}$ (at.%)	$c_{Sn,RBS}$ (at.%)	$\varepsilon_{II,Raman}$	$\varepsilon_{II,XRD}$
As-grown	296.2	11.1 ± 0.5	11.5 ± 0.1	-0.0142	-0.0100
PLA 0.20 J cm^{-2}	294.0	-	10 ± 1	-0.0049	-
PLA 0.25 J cm^{-2}	289.3	-	13 ± 1	0.0010	-
PLA 0.30 J cm^{-2}	290.4	-	11 ± 1	0.0023	-
PLA 0.40 J cm^{-2}	291.2	9.6 ± 0.5	11 ± 1	0.0035	-0.0003
PLA 0.50 J cm^{-2}	290.6	10.2 ± 0.5	11 ± 1	0.0038	0.0028
PLA 0.60 J cm^{-2}	290.7	8.9 ± 0.5	11 ± 1	0.0064	0.0038

The calculated $\varepsilon_{II,Raman}$ results suggest an in-plane strain relaxation due to PLA with E_d > 0.15 J cm^{-2} and a conversion into tensile strain after PLA with $E_d \geq$ 0.25 J cm^{-2}. Additionally, the tensile strain increases with increasing E_d, which correlates with the XRD results. The origin of the tensile strain might be a combination of the strain relaxation via defect formation, the formation of the Sn-depleted interface layer, and the higher thermal expansion coefficient of $Ge_{1-x}Sn_x$ [202] compared to the Sn-depleted interface layer. A similar thermal expansion effect is known for tensile strained epitaxial $Ge_{1-x}Sn_x$ or Ge films on Si substrates after cooling [97, 203]. At this place, it must be mentioned that the determination of the Sn concentration $c_{Sn,XRD}$ by (224) XRD-RSM for PLA E_d < 0.4 J cm^{-2} was not possible due to the $GeSn_{PLA}$ reflection intensity reduction towards smaller E_d or PLA-affected layer thickness (see Fig. 4.1 - 5 b)). Therefore, $c_{Sn,RBS}$ was approximated by RBS for these samples with E_d < 0.4 J cm^{-2}, as shown in Table 4.1 - 3. However, SIMNRA fitting of thin films and the presence of the Sn-rich clusters or filaments causes larger uncertainties. Hence, the $c_{Sn,XRD}$ estimation is assumed to be more precise for the molten layers. For the as-grown state, similar c_{Sn} were obtained by RBS, XRD, and TEM-EDXS analysis. By comparing the $\varepsilon_{II,XRD}$ and $\varepsilon_{II,Raman}$ of the as-grown state and PLA $E_d \geq$ 0.4 J cm^{-2} in Table 4.1 - 3, it can be concluded that the $Ge_{1-x}Sn_x$ layer is compressively strained before annealing and tensile strained after annealing. In fact, the strain values obtained by XRD and µ-Raman for the PLA samples are different, but the different penetration depths of the methods can explain this. Additionally, the disorder parameter b_d and the strain coefficient b_ε are also

determined for $Ge_{1-x}Sn_x$ alloys with x = 0.025 and 0.077 [201]. In our case, the Sn concentration is significantly higher. Therefore, slight differences can be expected. Furthermore, by converting the in-plane strain into an in-plane lattice parameter using Eq. 4.1 - 1 and adding this value in Fig. 4.1 - 5, it is visible that some surface-generated tail regions of the RSM $Ge_{1-x}Sn_x$ (224) reflection match the µ-Raman results.

The change of the fundamental optical transition in $Ge_{1-x}Sn_x$ alloys after PLA with 0.4 and 0.5 J cm^{-2} is investigated by low-temperature photo-reflectance (PR) spectroscopy at 30 K in a "bright configuration" experimental setup by Dr. Herbert Maczko at the University of Science and Technology in Wroclaw, Poland. Samples were excited by continuous-wave 405 nm laser with 100 mW power chopped with the frequency of 280 Hz. A phase-sensitive detection of the low-temperature PR signal is accomplished using a lock-in amplifier. The obtained low-temperature PR signal in Fig. 4.1 - 7 a) - c) is fitted with the low-field electromodulation Lorentzian line-shape function known as the Aspnes formula in Eq. 4.1 - 3 [204].

$$\frac{\Delta R}{R}(E) = Re\left[\sum_{j=1}^{N_r} C_j \mathrm{e}^{i'\theta_j}(\mathrm{h}f - E_j + i'\Gamma_j)^{-m_j}\right], \qquad \text{Eq. 4.1 - 3}$$

where $\frac{\Delta R}{R}(E)$ is the energy dependence from the real part (*Re*) of the PR signal, N_r is the number of PR resonances used to simulate the PR signal, hf is the photon energy of the probe beam, E_j is the energy of optical transition, i' is the imaginary unit, and Γ_j, C_j, and θ_j are the broadening, amplitude and phase angle of PR resonance, respectively. At 30 K, the nature of optical transitions (PR resonances) in $Ge_{1-x}Sn_x$ alloys is excitonic. Therefore, the exponent m_j is assumed to be 2. The fitting curves are plotted in Fig. 4.1 - 7 a) - c) by color lines together with the moduli of the individual PR resonances (color lines with filling), which are obtained from the Eq. 4.1 - 3 with parameters derived from the fit according to the Eq. 4.1 - 4.

$$\Delta\rho_j(E) = \frac{|C_j|}{\left[(hf - E_j)^2 + \Gamma_j^2\right]^{\frac{m_j}{2}}} \qquad \text{Eq. 4.1 - 4}$$

Here, $\Delta\rho_j(E)$ is a quantitative parameter used to describe the inhomogeneous broadening of each optical transition [205]. So far, the Aspnes formula has been widely used to analyze electro-reflection spectra in a variety of semiconductor materials, including $Ge_{1-x}Sn_x$ [206-208].

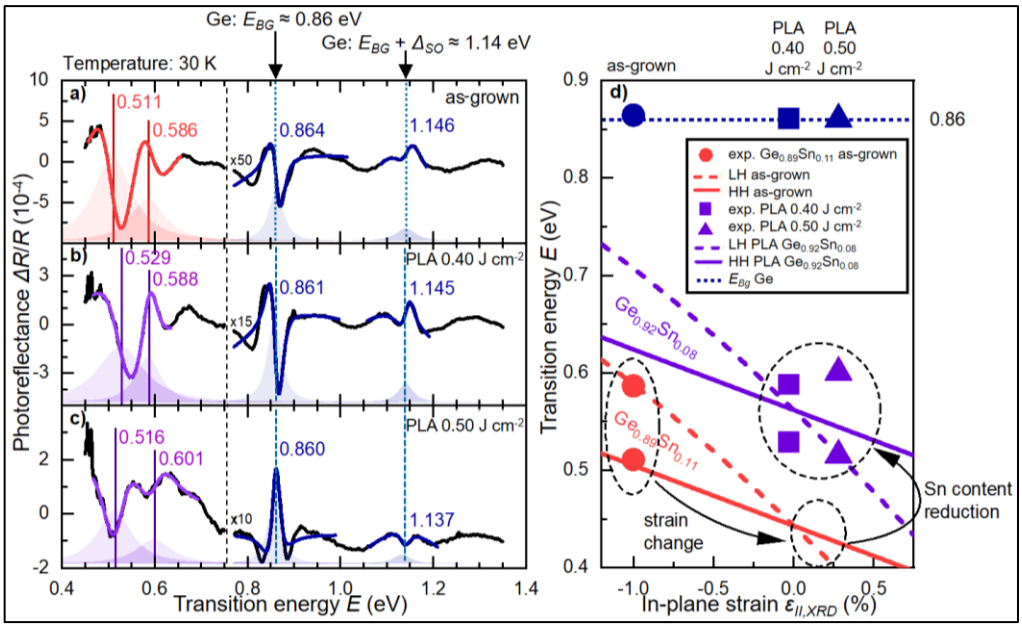


Fig. 4.1 - 7: Photo-reflectance spectra of the $Ge_{0.89}Sn_{0.11}$ in the as-grown state a), after PLA with 0.4 J cm^{-2} b), and after PLA with 0.50 J cm^{-2} c). The experimental results were marked by solid black lines and fitted to the strongest resonances. The fittings are depicted by colored solid lines for the optical transitions in Ge (blue) and $Ge_{1-x}Sn_x$ (red and purple). Moduli of every single-resonance are presented by area charts below the corresponding fitted lines with the same value scale as for photo-reflectance. The moduli are plotted with an offset, such that zero value is at the bottom of each chart. The optical transition energies measured at 30 K obtained from a) - c) are plotted as a function of in-plane strain $\varepsilon_{II,XRD}$ d). Calculated energies of optical transitions involving heavy holes HH (solid lines) and light holes LH (dashed lines) are plotted for $Ge_{0.89}Sn_{0.11}$ (red) and $Ge_{0.92}Sn_{0.08}$ (purple) alloys.

Fig. 4.1 - 7 a) – c) shows the PR results of $Ge_{1-x}Sn_x$ in the as-grown state and after PLA with 0.4 and 0.5 J cm^{-2}. Resonances at around 0.86 and 1.14 eV are related to optical transitions in the Ge layer beneath the $Ge_{1-x}Sn_x$ layer. The resonance at 0.86 eV is associated with the direct-band-gap of Ge [209], while the resonance at 1.14 eV is separated from it by the value of spin-orbit split-off energy Δ_{SO} of Ge [204]. The resonances at around 0.5 and 0.6 eV are related to $Ge_{1-x}Sn_x$. Fig. 4.1 - 7 d) shows the extracted transition energies in dependence on the in-plane strain $\varepsilon_{II,XRD}$ (see Table 4.1 - 2). The energies assigned to resonances at around 0.55 eV for as-grown samples are in good agreement with the values calculated for $Ge_{0.89}Sn_{0.11}$ at 30 K when the biaxial compressive strain of -1% is applied. Therefore, in the as-grown state, the PR resonance at 0.51 eV is attributed to the optical transition between the HH band and the CB, while the resonance at 0.58 eV is attributed to the optical transition between the LH band and the CB. As explained in detail in **section 2.3.2**, tensile strain and an increasing Sn concentration in the $Ge_{1-x}Sn_x$ alloy decrease the direct-band-gap energy. Furthermore, the LH band moves above the HH band due to tensile strain. It is worth noting that the $Ge_{1-x}Sn_x$ related resonances in Fig. 4.1 - 7 a) - c) may show a Franz-Keldysh oscillation [204], which complicates the analysis of PR spectra with two Aspnes resonances and the determination of the optical transition at higher energy due

to the strain-related LH-HH transition. Therefore, it is difficult to interpret the optical transition energies for $Ge_{1-x}Sn_x$ after PLA due to the more complex structure of the materials after the melting process and the possible Franz-Keldysh oscillations in the measured spectra. Nevertheless, these spectra are fitted with two resonances, and the obtained values undoubtedly support the simultaneous reduction of Sn in $Ge_{1-x}Sn_x$ and the earlier observed in-plane strain relaxation after PLA.

4.1.4 Electrical properties and defect analysis

Since the electrical properties of fabricated devices highly depend on the defect density, it is important to understand the influence of the melting process on the defect concentration and distribution. Therefore, the influence of PLA on the electrical properties, point defect concentration, and defect depth distribution was examined on selected samples by Hall-effect measurements, DB-VEPAS, and VEPALS.

The Hall-effect measurement results are summarized in Table 4.1 - 4. The hole concentration n_{h+} at 300 K in the as-grown state is 3.3×10^{18} cm^{-3} because of unintentional p-type doping during the growing process of $Ge_{1-x}Sn_x$ (see **section 2.3.3**). This background doping is already one magnitude higher than indicated in earlier reports [37]. After PLA, the hole concentration is increased to 4.1×10^{18} cm^{-3} (0.4 J cm^{-2}) and 4.9×10^{18} cm^{-3} (0.5 J cm^{-2}). Simultaneously, the mobility μ_{h+} is reduced from 304 cm² V^{-1}s^{-1} down to 231 cm² V^{-1}s^{-1}. Three effects can cause the reduced μ_{h+} after PLA: i) Coulomb scattering, ii) reduction of substitutional Sn, and iii) formation of tensile strain [210]. Especially the Coulomb scattering might play an important role because of the higher background doping and the generally lower crystal quality after PLA above the melting point (see Table 4.1 - 1). Additionally, by measuring the carrier concentration, it is possible to rule out a significant influence of doping level on the band-gap since the material is p-type, and the Borstein-Moss effect (see **section 2.3.3**) becomes significant for doping levels above 10^{19} cm^{-3}.

Table 4.1 - 4: Carrier concentration n_{h+} and mobility μ_{h+} of the $Ge_{1-x}Sn_x$ samples in the as-grown state and after PLA with 0.4 J cm^{-2} and PLA 0.5 J cm^{-2} measured at 300 K. Details about the parameter extraction can be found in **appendix 8.6**.

Sample	n_{h+} ($\times 10^{18}$ cm^{-3})	μ_{h+} (cm² V^{-1}s^{-1})
$Ge_{0.89}Sn_{0.11}$ as-grown	3.3	304
PLA 0.4 J cm^{-2}	4.1	267
PLA 0.5 J cm^{-2}	4.9	231

The type of defects, their concentration, and depth distribution in the $Ge_{1-x}Sn_x$ alloys were investigated by DB-VEPAS and VE-PALS with the setup explained in **section 3.11**. Positrons implanted into a solid material thermalize and shortly diffuse until they finally annihilate with electrons in delocalized lattice sites (interstitials) or localize in

vacancy-like defects and interfaces. As a consequence of annihilation, two anti-collinear 511 keV gamma photons are emitted. Since at the annihilation site, thermalized positrons have very small momentum compared to the electrons, a broadening of the 511 keV line is observed mostly due to the momentum of the electrons, which is then measured with a high-purity Ge detector (overall energy resolution of 1.09 ± 0.01 keV at 511 keV). This broadening is characterized by two distinct parameters, *S* and *W*, defined as fractions of the annihilation line in the middle (511 ± 0.74 keV) and outer regions (508.7 ± 0.30 keV and 513.30 ± 0.30 keV), respectively. The relative changes in defect density (the *S*-parameter) and elemental decoration of defects (the *W*-parameter) across the sample thickness were studied by DB-VEPAS (see Fig. 4.1 - 8). The *S*-parameter Fig. 4.1 - 8 a) is the fraction of positrons annihilated with low momentum valence electrons and represents vacancy-type defects and their concentration. In general, the plotted annihilation line parameter *S* in Fig. 4.1 - 8 a) is directly proportional to the defect concentration. However, it depends on the defect size and tends to saturate for larger defect concentrations. An increase of *S* as a function of PLA energy density applied on the film is observed, and a variation of the maximum $S(E_p)$ position reflects changes across the $Ge_{1-x}Sn_x$ layer thickness. This correlates with the higher number of defects between 50 and 200 nm in the PLA 0.5 J cm^{-2} sample observed in the TEM results (see Fig. 4.1 - 3 b) or Fig. 8.3 - 1 d)). The concentration of open-volume defects is higher after PLA compared to the as-grown state (lower slope and a maximum at E_p = 7 keV) and a Ge reference sample (lowest slope, no maximum). Interestingly, the *S*-parameter at E_p = 0.05 keV is very similar for all PLA samples, as visible in Fig. 4.1 - 8 a) and Table 4.1 - 5. Similar surface properties were previously assumed from the µ-Raman results in Fig. 4.1 - 6 for PLA $E_d \geq 0.25$ J cm^{-2}.

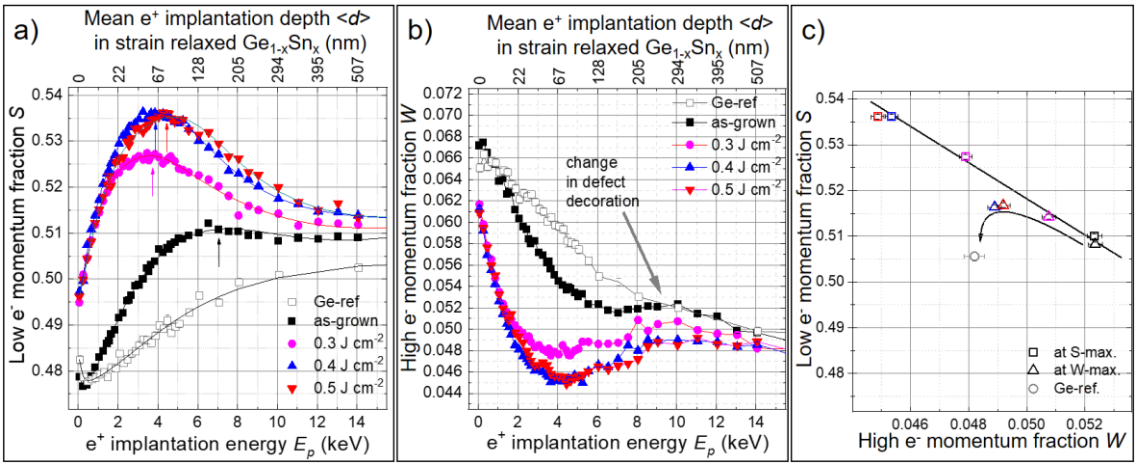


Fig. 4.1 - 8: Annihilation line parameter *S* a) and *W* b) of the Ge reference, as-grown $Ge_{0.89}Sn_{0.11}$ and after PLA with E_d = 0.3, 0.4, and 0.5 J cm^{-2} a) as a function of positron implantation energy E_p and mean positron implantation depth <*d*> calculated by Eq. 3.11 - 1 with the corresponding fits. S-W plot c) of the maximum values from $S(E_p \approx 4$ or 7 keV) and $W(E_p \approx 10$ keV) dependencies compared to the bulk value (E_p = 35 keV) of the Ge reference sample.

The *W*-parameter in Fig. 4.1 - 8 b) approximates the overlap of the positron wavefunction with the high-momentum core electrons, enabling the direct analysis of defect-decorated atoms in the matrix. Hence, the *W*-parameter can be used to evaluate the atomic environment at the positron annihilation site. At E_p = 10 keV is a peak, which can be allocated to the $Ge_{0.9}Sn_{0.1}$ / Ge interface because the *W* value of the $Ge_{0.89}Sn_{0.11}$ approaches the *W* value of the Ge reference sample. For the PLA-treated samples, there is additionally the Sn depletion region between the PLA-affected $Ge_{1-x}Sn_x$ and unaffected $Ge_{0.89}Sn_{0.11}$ layer (see Fig. 4.1 - 3 e)), which is, however, not clearly visible in Fig. 4.1 - 8 b). This is likely due to the fact that the Sn-depleted layer is too thin and deeply buried for positrons to resolve it. In order to compare changes in defect density (*S*) and the defect decoration types (*W*), it is suitable to plot *S* versus *W* (see Fig. 4.1 - 8 c)) at two characteristic depths of each sample [211]. The discussed depths are i) the lower depth corresponding to the $S(E_p)$ maximum (indicated by the arrow in Fig. 4.1 - 8 a)) and ii) the deeper depth – W ($E_p \approx$ 10 keV) (see Fig. 4.1 - 8 b)). The data points from the smaller depth exhibit a linear relation to each other in Fig. 4.1 - 8 c), indicating that PLA-treated samples share a similar defect type as the as-grown state. Deeper in the film, a trend in the direction toward the Ge reference sample is found. Hence, the observed change at $E_p \approx$10 keV is related to the increased defect decoration by Ge (less decoration of Sn). Moreover, the local stoichiometry must contain Sn atoms for both considered depths, as no apparent linear relation can be drawn between the Ge reference and $Ge_{1-x}Sn_x$ data points.

The VEPFit code [212] has been utilized for the analysis of positron diffusion length L_+, which is inversely proportional to defect concentration c_v. The code enables the evaluation of defect densities as a function of depth in multilayer systems. The $S(E_p)$ curves in Fig. 4.1 - 8 a) were fitted assuming a four-layer system by using the layer stack presented in Fig. 4.1 - 1 a) and c) consisting of the strain-relaxed $Ge_{1-x}Sn_x$ (including Sn-depleted $Ge_{1-x}Sn_x$), unaffected $Ge_{0.89}Sn_{0.11}$, Ge, and Si substrate. The selected parameters and calculation results are summarized in Table 4.1 - 5. The layer thickness d_1 of $Ge_{1-x}Sn_x$ and $Ge_{0.9}Sn_{0.1}$ was determined by RBS (see Fig. 4.1 - 2 b)) and TEM (see Fig. 4.1 - 3) and was fixed to these values for the calculation. Details about the calculation of c_v, material densities of the strained $Ge_{0.89}Sn_{0.11}$ and strain-relaxed $Ge_{1-x}Sn_x$ layers, and the assumed layer stack can be obtained from **appendix 8.7**. L_+ for the Ge-buffer layer and Si-substrate was fixed to 111 nm and 220 nm, respectively, based on the Ge single-crystal substrate measurement and literature [213]. The boundary between the Ge-buffer layer and the substrate was kept constant at a depth of 700 nm, according to planned deposition conditions. For simplicity, 15 nm was added to d_1 in the

case of PLA samples to account for the thickness of the depleted layer. Such a thin layer has negligible influence on the positron annihilation as no clear variation of the $S(E_p)$ curve shape in Fig. 4.1 - 8 a) has been observed around this depth. Based on the fitting results, the calculated positron diffusion lengths of the PLA-treated films are too short for positrons to arrive directly at the depleted layer. Hence, the defect density in the Sn-depleted layer must be similar to the PLA-treated $Ge_{1-x}Sn_x$ top or the $Ge_{0.89}Sn_{0.11}$ bottom layers. d_1 for the as-grown $Ge_{0.89}Sn_{0.11}$ was fixed to 290 nm and the obtained $L_{+,1}$ = 37.4 nm served as a reference for the unaffected $Ge_{0.89}Sn_{0.11}$ layer in the PLA-treated samples (see Fig. 4.1 - 1 c)). Hence, the only free-fitting parameter was the effective diffusion length $L_{+,1}$ in the $Ge_{1-x}Sn_x$ top layer.

Table 4.1 - 5: The calculated S_{surf}, S_1, thickness d_1, effective diffusion length $L_{+,1}$, and vacancy-related defect concentration c_V for the Ge reference sample, $Ge_{0.89}Sn_{0.11}$ as-grown state, and $Ge_{1-x}Sn_x$ samples after PLA with 0.3, 0.4, and 0.5 J cm^{-2}, respectively, were calculated with VEPFit code [212]. A standard deviation for the last digit after the comma is shown in brackets for S_{surf} and S_1. S_{surf} was calculated close to the sample surface at (E_p = 0.05 keV).

Sample name	S_{surf}	S_1	d_1 (nm)	$L_{+,1}$ (nm)	c_V (x 10^{-5} atom^{-1})
Ge reference	0.4770 (2)	0.5048 (3)	-	111 ± 3	<1
$GeSn_{as\text{-}grown}$	0.475 (2)	0.514 (2)	290	37 ± 3	3.5 ± 0.3
$GeSn_{PLA\ 0.30\ J\ cm^{-2}}$	0.499 (3)	0.528 (1)	100	10 ± 2	54 ± 11
$GeSn_{PLA\ 0.40\ J\ cm^{-2}}$	0.506 (4)	0.538 (1)	140	14 ± 2	27 ± 4
$GeSn_{PLA\ 0.50\ J\ cm^{-2}}$	0.506 (3)	0.538 (1)	195	18 ± 3	16 ± 3

The calculated defect concentration in the $Ge_{0.89}Sn_{0.11}$ as-grown sample is relatively low ($c_V \approx 3.5 \times 10^{-5}$ atom^{-1}) due to a large $L_{+,1}$ = 37±3 nm, but is still three times larger than for the undoped Ge reference crystal. The slight loss of crystal coherency compared to the Ge reference is unsurprising for materials grown by MBE since surface defects in the buffer or strain relaxation events in the $Ge_{0.89}Sn_{0.11}$ layer can lead to defects at the interface. After PLA with 0.3 J cm^{-2}, when the molten layer is about 100 nm thick, the defect concentration increases about 15 times to $c_V \approx 54 \times 10^{-5}$ atom^{-1}). This suggests that the presented strain relaxation events lead to an abrupt formation of open-volume defects. Increasing the PLA energy densities to 0.4 J cm^{-2} and 0.5 J cm^{-2} decreases the c_V. At first glance, the general increasing trend of the calculated S parameter as a function of PLA E_d seems to contradict the drop in c_V. However, the rising density of larger vacancy clusters (see Fig. 4.1 - 9 c)) after PLA is likely the main cause of the S-parameter increase, as explained below. These results indicate that the high diffusion coefficient in the molten film, may be also in combination with the assumed pipe diffusion

mechanism reported by Abdi et al. is an effective way for strain relaxation and open-volume defects agglomeration [126].

In addition, the defect depth distribution in the $Ge_{0.89}Sn_{0.11}$ as-grown and PLA annealed samples was studied using VE-PALS. Fig. 4.1 - 9 a) shows the average positron annihilation lifetime τ_{av}, which is the weighted average defect size, across sample thickness. τ_{av} can be expressed by Eq. 4.1 - 5. The positron annihilation lifetime τ_N refers to the characteristic annihilation sites (vacancy-like defects of different sizes) and I_N is the relative number of positrons trapped at these defect types. In other words, τ_{av} indicates the density of vacancy-like (open-volume) defects.

$$\tau_{av} = \sum_N \tau_N I_N \qquad \text{Eq. 4.1 - 5}$$

In general, the positron lifetime increases with increasing the size of the open-volume defects and negativity of the defect charging state (more negative – slightly longer lifetime) [214]. The τ_{av} results in Fig. 4.1 - 9 a) at 3 keV (~42 nm) increase from ~275 ps in the as-grown sample to about ~293 ps and ~284 ps after PLA with E_d = 0.4 J cm^{-2} and 0.5 J cm^{-2}, respectively. For positron implantation energies lower than 2 keV, all curves in Fig. 4.1 - 9 a) show a longer lifetime (close to the sample surface) because the signal is superimposed by the surface and its defect states [215-217]. For higher positron implantation energies, only the defect states are visible (purest defect contributions can be obtained at the *S*-parameter maximum in Fig. 4.1 - 8 a)).

Eq. 4.1 - 5 shows that τ_{av} is a combination of the discrete positron lifetime components τ_N (τ_1 and τ_2), obtained by the spectra decomposition in Fig. 4.1 - 9 b) and their relative intensities I_1 and I_2 in Fig. 4.1 - 9 c). In general, positron lifetime scales with the local electron density, which is influenced by the size of open-volume defects and their chemical composition, carrier concentration, and the defect charge state [214]. In our case, τ_1 is not straightforward to define as it could represent a defect-free $Ge_{1-x}Sn_x$ material (bulk annihilation in Fig. 4.1 - 9 b)), a fully Sn-decorated Ge-mono-vacancy (V_{Ge}+*N* Sn_{Ge}, where *N* is the number of Sn atoms substituting Ge) or $Ge_{1-x}Sn_x$ with shallow trapping dislocations [218]. On the other hand, τ_2 describes vacancy agglomeration (clusters containing a certain number of vacancies). The positron lifetime components τ_1 and τ_2 as a function of depth reveal a defect size evolution due to annealing (see Fig. 4.1 - 9 b)). In comparison with the as-grown sample, the first lifetime component τ_1 increases by about ~16 ps across the depth after PLA with 0.4 J cm^{-2} and about ~8 ps after PLA with 0.5 J cm^{-2}. This is accompanied by a reduction of its relative intensity I_1 by not more than ~10%, indicating an overall reduction of small defect states related to τ_1.

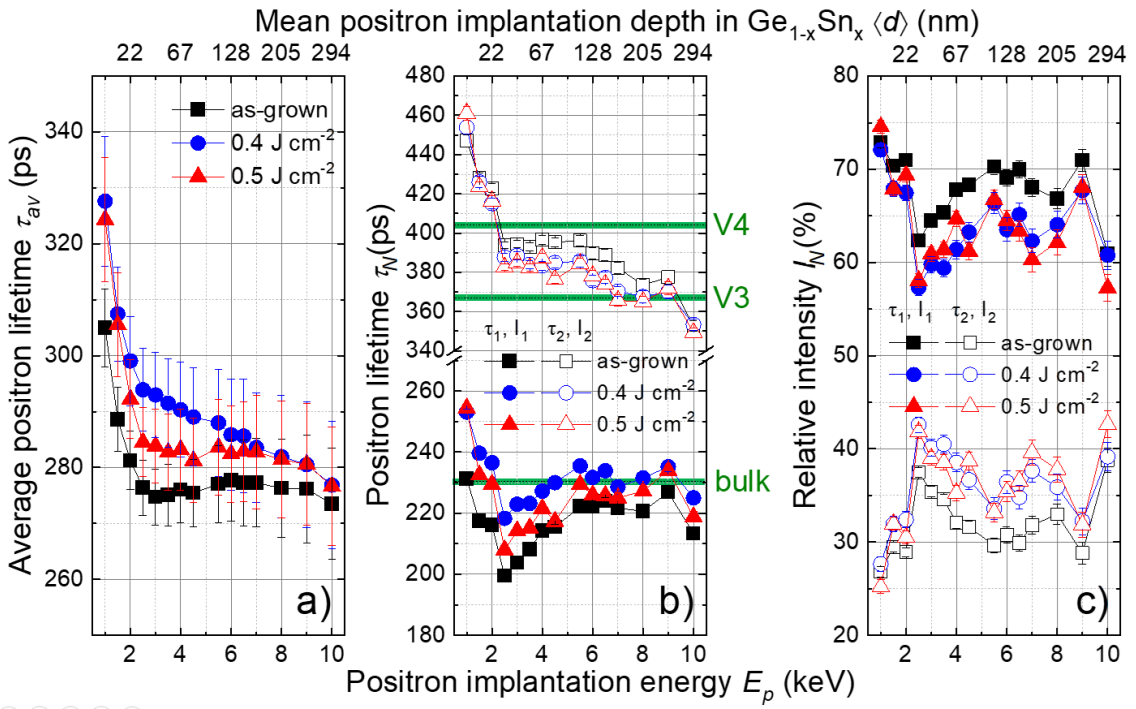


Fig. 4.1 - 9: Average positron annihilation lifetime τ_{av} of the $Ge_{0.89}Sn_{0.11}$ samples in the as-grown state and after PLA with an energy density of 0.4 J cm^{-2} and 0.5 J cm^{-2} as a function of positron implantation energy E_p and mean positron implantation depth <*d*> a). Discrete positron lifetime components τ_1 (closed symbols) and τ_2 (open symbols) obtained by spectra decomposition of τ_{av} b). The ATSUP simulated positron lifetimes of bulk $Ge_{0.9}Sn_{0.1}$ (bulk) and vacancy clusters of 3 vacancies (V3) and 4 vacancies (V4) obtained from Fig. 4.1 - 10 c) are highlighted in green. The relative intensities I_1 (closed symbols) and I_2 (open symbols) of the lifetime components τ_1 and τ_2 c).

To understand the change of τ_1, the so-called atomic superposition (ATSUP) [219] calculations were performed for Ge and $Ge_{0.9}Sn_{0.1}$ cubic crystals. In these simulations, $Ge_{0.9}Sn_{0.1}$ was used because XRD-RSM (see Table 4.1 - 2) and TEM line scan (see Fig. 8.3 - 1 f)) of the PLA-treated $Ge_{1-x}Sn_x$ showed that the Sn concentration in the matrix between filaments is slightly lower than that in the as-grown sample. The calculated positron lifetime as a function of the in-plane lattice parameter and the number of Sn atoms decorating V_{Ge} are plotted in Fig. 4.1 - 10 a), b), and c). Details about the simulations and the calculation results can be found in **appendix 8.7**.

From the ATSUP calculation, we obtain that the calculated lifetime in $Ge_{0.9}Sn_{0.1}$ is increasing with the in-plane lattice parameter for both bulk and V_{Ge} (see Fig. 4.1 - 10 a)). The number of Sn atoms substituted by Ge in $Ge_{0.9}Sn_{0.1}$ has only a minor influence on the bulk positron lifetime. In contrast, a substantial reduction of positron annihilation lifetime is observed for Sn atoms substituted by V_{Ge} (Fig. 4.1 - 10 b)). Finally, positron lifetime scales with the vacancy cluster size in a similar way for $Ge_{0.9}Sn_{0.1}$ as for Ge as shown in Fig. 4.1 - 10 d).

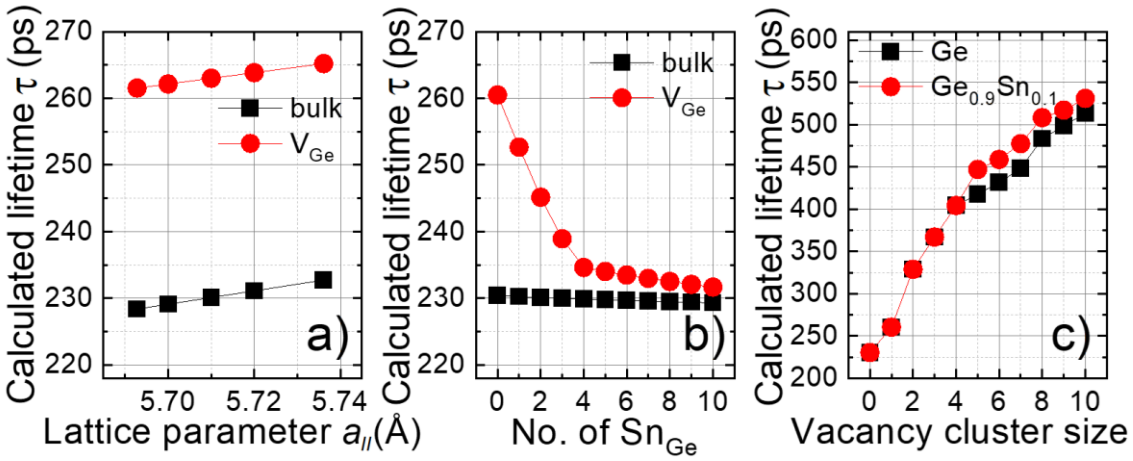


Fig. 4.1 - 10: ATSUP calculations of positron lifetime τ as a function of the in-plane lattice parameter $a_{//}$ for bulk $Ge_{0.9}Sn_{0.1}$ and Ge-mono vacancy V_{Ge} configurations a) obtained from Table 8.7 - 3. The number of Sn nearest-neighbors (≤4) and next-nearest-neighbors donors decorating Ge atom and V_{Ge} in bulk $Ge_{0.9}Sn_{0.1}$ b) is obtained from Table 8.7 - 4. Calculated positron lifetime τ as a function of the vacancy accumulated cluster size for Ge and $Ge_{0.89}Sn_{0.11}$ crystals c).

With these results, we reveal that the change of τ_1 in Fig. 4.1 - 9 b) is likely a superposition of $a_{//}$ variation shown in Fig. 4.1 - 10 a) and a change of the Sn distribution at V_{Ge}, as shown in Fig. 4.1 - 10 b). Therefore, the component τ_1 combines the positron annihilation in bulk and at the Sn-decorated V_{Ge}. Experimentally, the reference lifetime in bulk Ge is in the range of 224–228 ps [220] and decreases with increasing Sn concentration [221], which is in line with our calculations. Moreover, we assume that the average area of filaments, i.e., regions with high Sn content (equivalent to the shorter positron lifetime due to larger Sn decoration of V_{Ge}), increases with PLA energy density. Such Sn-rich filaments are not observed in the as-grown sample at all. There, the positron lifetime is the shortest and likely represents bulk annihilation lifetime. On the other hand, the slight variation of lifetime between samples annealed with different PLA energy densities is likely related to a variation in the average number of Sn atoms bonded with V_{Ge}. Furthermore, the relative intensity I_1 decreases after the PLA (see Fig. 4.1 - 9 c)), which reflects the overall reduction of the Sn-vacancy complex concentration. In general, after PLA, τ_2 is reduced in all samples. This means that the average size of larger vacancy clusters decreases, but simultaneously, the relative intensity I_2 increases (see Fig. 4.1 - 9 c)), indicating a larger fraction of positrons annihilating with vacancy agglomerations modified due to PLA. The τ_2 is in the order of 400 ps, referring to the vacancy clusters with about three to four agglomerated vacancies (see Fig. 4.1 - 9 b)). A larger concentration of vacancy clusters can increase scattering and reduce the mobility of charge carriers, as shown by the Hall-effect measurements [222].

4.1.5 Strain-relaxed $Ge_{1-x}Sn_x$ as virtual substrates

The previous section shows that post-growth PLA with $E_d \geq 0.25$ J cm^{-2} applied on $Ge_{0.89}Sn_{0.11}$ causes strain relaxation but reduces the overall layer quality. However, strain-relaxed layers with a high-quality are desired to achieve a direct optical BG and for lateral n-type electrical devices. Both might be achievable when strain-relaxed PLA-treated $Ge_{1-x}Sn_x$ is used as a buffer layer for epitaxial growth of high-quality $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$. In previous experiments, $Ge_{0.92}Sn_{0.08}$ could be grown by MBE epitaxially on a CVD-grown partly strain-relaxed $Ge_{0.92}Sn_{0.08}$-buffer [223]. This section discusses the possibilities of fabricating MBE-grown $Ge_{0.89}Sn_{0.11}$ on the PLA-treated strain-relaxed $Ge_{1-x}Sn_x$-buffer.

For this purpose, a new $Ge_{0.89}Sn_{0.11}$ material with improved MBE growing conditions was fabricated using the approach described in **section 3.1** and the conditions summarized in **appendix 8.1**. The 35 x 35 mm² samples with the layer stack presented in Fig. 4.1 - 1 a) were treated with PLA with E_d = 0.5 J cm^{-2}. After PLA, the strain relaxation effect was confirmed by µ-Raman (see **appendix 8.8)**. The surface conditions after PLA are the most critical obstacle for a successful epitaxial growth of $Ge_{0.89}Sn_{0.11}$ or, in general, $Si_{1-x-y}Ge_ySn_x$ layers on the strain-relaxed PLA-treated virtual substrate. Before and after PLA, the surface topography was imaged by atomic force microscopy (AFM), presented in Fig. 4.1 - 11, performed by Dr. Denise Erb under ambient conditions. For this, a Bruker MultiMode8 setup in tapping mode was used with the cantilever resonance frequency of 160 kHz and the tip curvature radius of 10 nm.

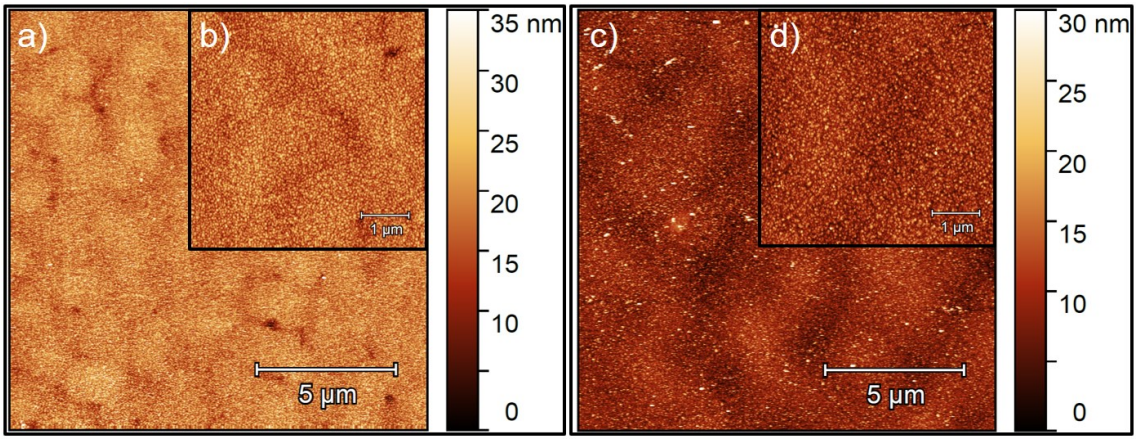


Fig. 4.1 - 11: AFM mappings of the $Ge_{0.89}Sn_{0.11}$ as-grown state a), b) and after PLA with 0.5 J cm^{-2} c), d) with an investigation area of 15 x 15 µm² a), c) and 6 x 6 µm² b), d).

As visible in Fig. 4.1 - 11 a) and b), the surface topology before PLA consists of rectangular structures with an averaged root-mean-square (*RMS*) roughness of 3 nm. After PLA, the surface is smoothed in Fig. 4.1 - 11 c) and d), and the roughness is reduced to RMS = 2.3 nm. A similar surface smoothening trend could be earlier

observed in cross-sectional TEM images (see Fig. 4.1 - 3 a) - e)). This roughness is similar to the reported RMS of 1 and 5 nm roughness of CVD as-gown samples [119] and is, in general, of an acceptable quality for a second MBE growth.

In the next fabrication step, the native $Ge_{1-x-y}Sn_xO_y$ oxide on the $Ge_{1-x}Sn_x$ surface was removed by etching for 15 s in 2% HF diluted in deionized water (DI) or for 30 s in 8% Hydrochloric acid (HCl) followed by a DI dip, as reported in ref. [223]. Afterward, the hydrogen-terminated surface was removed with an *in situ* thermal desorption at different substrate temperatures between 250 and 260 °C in the MBE chamber. Pre-experiments performed by Dr. Daniel Schwarz at the University of Stuttgart have shown that these temperatures are the lower limit to remove the H dangling bonds on the surface, which appear after HF etching. However, the *in situ* thermal treatment generated massive Sn segregation on the sample surface since the temperatures were for a long time above the eutectic temperature (see Fig. 2.1 - 1). The newly grown $Ge_{1-x}Sn_x$ layer with substrate temperatures of 120 °C appeared milky with Sn segregations. Subsequent experiments to reduce the desorption temperatures below 250 °C resulted in polycrystalline $Ge_{1-x}Sn_x$ films. For further experiments using this approach, the following solutions are suggested: i) The Sn concentration of the PLA-treated $Ge_{1-x}Sn_x$ virtual substrate can be reduced. This would lead to a smaller lattice parameter mismatch to the next grown layer but will increase, on the other hand, the thermal stability of the virtual substrate to prevent Sn segregation during the growth. The appearance of the reported strain relaxation effect for $Ge_{1-x}Sn_x$ with a lower Sn concentration ($x \approx 3$ and 6 at.%) was confirmed during this thesis and published in collaboration with F. Berkmann in ref. [159]. ii) Further etching approaches, like etching with diluted acetic acid, could be performed [224]. iii) MBE cluster tools equipped with either an inert gas sputtering possibility to remove the H dangling bonds or a PLA setup could be used. On the other hand, there is also the possibility that the CVD-grown $Ge_{1-x}Sn_x$ layers, which are generally grown at higher temperatures (350 – 400 °C), might be more stable against Sn segregations than the MBE-grown PLA-treated $Ge_{1-x}Sn_x$ layers.

4.1.6 Conclusion

Compressively strained single-crystalline $Ge_{0.89}Sn_{0.11}$ was successfully fabricated via MBE on Si with the help of a Ge virtual substrate and Ge-buffer layer. However, the growth process needs to be further optimized since the as-grown $Ge_{0.89}Sn_{0.11}$ layer has a texture, contains many defects, and is not fully pseudomorphically grown on the Ge-buffer. Post-growth PLA below the melting threshold ($E_d > 0.15$ J cm^{-2}) changes neither the crystal quality nor the elemental distribution. Post-growth PLA close or above the melting threshold ($E_d \leq 0.2$ J cm^{-2}) causes elemental redistribution and strain

relaxation. The melting depth depends linearly on the applied energy density of the ns-laser pulse. After laser melting and liquid phase epitaxy, the former $Ge_{0.89}Sn_{0.11}$ layer can be divided from the bottom to the top into three horizontal layers with different microstructures. i) The bottom layer is the almost unaffected $Ge_{0.89}Sn_{0.11}$ layer. ii) There is a thin Sn-depleted layer between the molten and the unaffected bottom layer. iii) The upper part is the molten and strain-relaxed $Ge_{1-x}Sn_x$ surface layer, which contains Sn-rich cluster and vertical Sn-rich filaments in a slightly Sn-depleted single-crystalline $Ge_{1-x}Sn_x$ matrix (about 1% lower Sn concentration as in the as-grown state). These Sn-related defects, in combination with point defects, lower the overall layer quality after PLA at $E_d \leq 0.2$ J cm^{-2}. In the case of PLA at high energy densities ($E_d \leq 0.5$ J cm^{-2}), a conversion from the in-plane compressive strain of the as-grown state into tensile strain was found XRD-RSM. This strain relaxation phenomenon was also recently confirmed by other researchers for different $Ge_{1-x}Sn_x$ compositions [126, 159, 182, 194]. Owing to the strain in the as-grown and PLA-treated $Ge_{1-x}Sn_x$ layers, the valence band is divided into light and heavy holes. In the case of compressively strained as-grown material, an optical transition between heavy holes to the conduction band takes place at 0.51 eV. In contrast, after PLA in the tensely strained material, the transition occurs at around 0.52 eV (E_d = 0.5 J cm^{-2}) and E_d = 0.53 eV (0.4 J cm^{-2}), respectively. This is explained by the change of strain and Sn concentration in the molten layer. Using positron annihilation spectroscopy, the overall defect concentration in the as-grown sample was determined to be about 3.5 x 10^{-5} atom^{-1}. After PLA at 0.3 J cm^{-2}, the defect density increases to ~54 x 10^{-5} atom^{-1}, followed by a substantial decrease for higher energies to ~27 x 10^{-5} atom^{-1} for 0.4 J cm^{-2} and ~16 x 10^{-5} atom^{-1} for 0.5 J cm^{-2}. Additionally, the fraction of larger vecancy clusters increased after PLA, while the fraction of smaller vacancies decreased. This vacancy agglomertion process can be understood as a purification process, which can allow higher carrier mobilities. However, Hall-effect results showed a decreasing mobility after PLA. This could be related to the presence of Sn-clusters, more electrically active p-type dopants, or the slightly reduced Sn concentration of the $Ge_{1-x}Sn_x$ matrix. The highest defect concentrations were found between 50 and 100 nm below the sample surface, depending on the used laser energy density. Close to the surface, the defect concentration drops down and reaches similar values for all investigated PLA annealing states. AFM measurements confirm a reducing surface roughness from 3 nm of the as-grown state to 2.3 nm after PLA with 0.5 Jcm^{-2}. The combination of the simple and effective strain relaxation approach with a smooth surface layer makes the presented post-growth PLA promising for novel virtual substrates. However, the removal of the $Ge_{1-x-y}Sn_xO_y$ oxide still causes problems and prevents the successful epitaxial growth of high-quality tensile strained $Si_{1-x-y}Ge_xSn_y$

alloys on the PLA-treated virtual substrate. A recent publication has shown that good as-grown material properties can be maintained after PLA when a high-quality CVD-grown layer is used [194]. However, the local formation of Sn-rich clusters makes the presented ns-melting approach unsuitable for nanoelectronic applications with homogeneous properties.

4.2 Post-growth flash lamp annealing

The second studied method to improve the as-grown layer quality of MBE-grown $Ge_{1-x}Sn_x$ alloys is millisecond FLA. Compared to PLA, this approach uses a much longer pulse length and a broader wavelength spectrum for the thermal treatment, which allows the movement of point defects without causing Sn segregations. A general introduction to this annealing method is given in **section 2.4.2**. Until today, not much has been published about the influence of post-growth FLA on grown $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ layers since FLA is not widely used yet. On the other hand, this annealing method could cause multiple effects like diffusion, phase separation, strain relaxation, activation or deactivation of dopants, healing defects, etc. Therefore, these topics will be addressed in the present section by RBS-R/C, µ-Raman, PAS, Hall-effect, SIMS, and electrochemical capacitance-voltage measurement (ECV) measurements.

4.2.1 Material fabrication and r-FLA annealing

Various $Ge_{1-x}Sn_x$ (x ≥ 8 - 16 at.%) alloys with and without *in situ* doping were grown by MBE, as discussed in detail in ref [93]. The $Ge_{1-x}Sn_x$ layers are approximately 200 nm thick and grown on a Ge-buffered Si substrate, as schematically shown in Fig. 4.2 - 2. MBE *in situ* doping was done by adding Sb for n-type and B for p-type. Details about the growth process and parameters can be found in **section 3.1**, **appendix 8.1**, and ref. [93], respectively. Three representative $Ge_{1-x}Sn_x$ (x = 9, 12, and 16 at.%) alloys were selected out of these sample batches to explain the impact of ms-r-FLA. Table 4.2 - 1 summarizes the properties of the as-grown states from ref. [93].

Table 4.2 - 1: Property overview of the selected $Ge_{1-x}Sn_x$ (x = 9, 12, and 16 at.%) alloys obtained from ref. [93]. Strain and layer composition was determined by (004) HR-XRD and asymmetrical (224) XRD-RSM. The Sn concentration c_{Sn} and the in-plane strain ε_{II} of $Ge_{0.88}Sn_{0.12}$ and $Ge_{0.84}Sn_{0.16}$ are divided into the partially stain-relaxed top layer (first value) and the pseudomorphically grown bottom layer (second value).

Alloy	$Ge_{0.91}Sn_{0.09}$	$Ge_{0.88}Sn_{0.12}$	$Ge_{0.84}Sn_{0.16}$
Sn concentration c_{Sn} (at.%)	8.74	12.46; 11.43	15.84; 15.26
Dopant type	n-type	n-type	p-type
Dopant	Sb	Sb	B
Dopant concentration n (cm^{-3})	1×10^{20}	1×10^{20}	1×10^{20}
Layer thickness d (nm)	200	200	200
In-plane strain ε_{II} (%)	-1.28	-0.71; -1.50	-0.49; -2.14

Sample $Ge_{0.91}Sn_{0.09}$ is fully pseudomorphically grown on the strain-relaxed Ge-buffer and is, therefore, highly in-plane compressive strained (ε_{II} = -1.28). The $Ge_{1-x}Sn_x$ (x = 12 and 16 at.%) samples are highly compressive strained close to the $Ge_{1-x}Sn_x$/Ge interface and experience a partial strain relaxation when the composition-dependent critical thickness

for strain relaxation (see **section 2.2 – I**) is exceeded. The presented alloys are highly n-type (Sb = 1 x 10^{20} cm^{-3}) or p-type (B = 1 x 10^{20} cm^{-3}) doped according to the planned growth conditions.

The FLA process was performed for all samples from the rear-side (r-FLA) in N_2 atmosphere with a fixed pulse length of 3.2 ms since previous experiments have shown that 3.2 ms is short enough to fabricate $Ge_{1-x}Sn_x$ (x = 3 at.% and 4.5 at.%) alloys by Sn implantation into Ge without Sn segregations [104, 225]. The flash energy density was systematically increased until the sample surface was locally molten (upper annealing limit) in the corners or edges. Then, annealing conditions slightly below the melting conditions were selected for further investigations. The $Ge_{1-x}Sn_x$ top surface was protected by placing the sample on a clean Si dummy wafer. The COMSOL code [175] was used to simulate the r-FLA temperature in the $Ge_{1-x}Sn_x$ layers. The simulated temperatures, presented in Fig. 4.2 - 3 b), vary between 428 °C and 506 °C. Thus, the annealing temperatures are significantly above the growth temperatures and the eutectic temperature of 231 °C. However, the simulation result should be treated as a rough estimation instead of a precise calculation, as explained in **appendix 8.9**.

4.2.2 Alloy composition and strain analysis

The r-FLA annealing test was accompanied by optical microscopy, RBS, and µ-Raman investigations since annealing can cause various effects like Sn segregations, elemental redistribution, and strain relaxation.

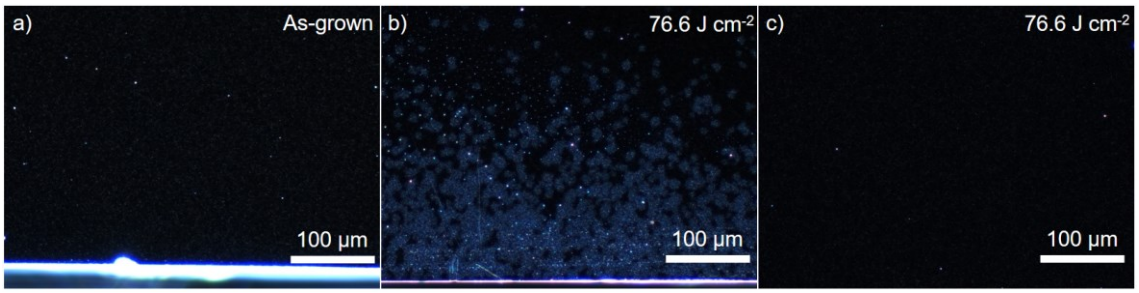


Fig. 4.2 - 1: Exemplary dark field images of the $Ge_{0.88}Sn_{0.12}$ sample in the as-grown state a) and after r-FLA with E_d = 76.6 J cm^{-2} b), and c). Images a) and b) were taken at the sample edge and c) close to the sample center.

The optical microscopy images, like in Fig. 4.2 - 1, are used to observe first Sn segregations or the formation of the molten fringes on the $Ge_{1-x}Sn_x$ layer surface. The exemplary selected $Ge_{0.88}Sn_{0.12}$ material shows in the as-grown state in Fig. 4.2 - 1 a) only minor surface defects in a homogeneous matrix. After r-FLA with 76.6 J cm^{-2}, first local molten fringes appear close to the corners and edges on the $Ge_{1-x}Sn_x$ surface (see blueish contributions in Fig. 4.2 - 1 b)) because of higher temperatures (enhanced light absorption) on the sample edges. However, the surface in the sample center (see

Fig. 4.2 - 1 c)) has a similar perfection as the as-grown state. Further increase of the applied r-FLA E_d overheats the entire $Ge_{0.88}Sn_{0.12}$ layer. For this experiment, the melting fringes shown in Fig. 4.2 - 1 b) were used to prove a sufficient annealing close to the material limit. The following material investigations were performed close to the center of the 10 x 10 mm² specimens.

RBS-R/C measurements were performed to investigate elemental distributions and verify the crystal quality before and after r-FLA. The RBS-R measurements in Fig. 4.2 - 2 have a constant Sn and Ge intensity before and after annealing, which confirms $Ge_{1-x}Sn_x$ layers with a constant Ge and Sn depth profile. Additionally, the Sn intensity increases while the Ge intensity decreases according to the expected $Ge_{1-x}Sn_x$ alloy composition.

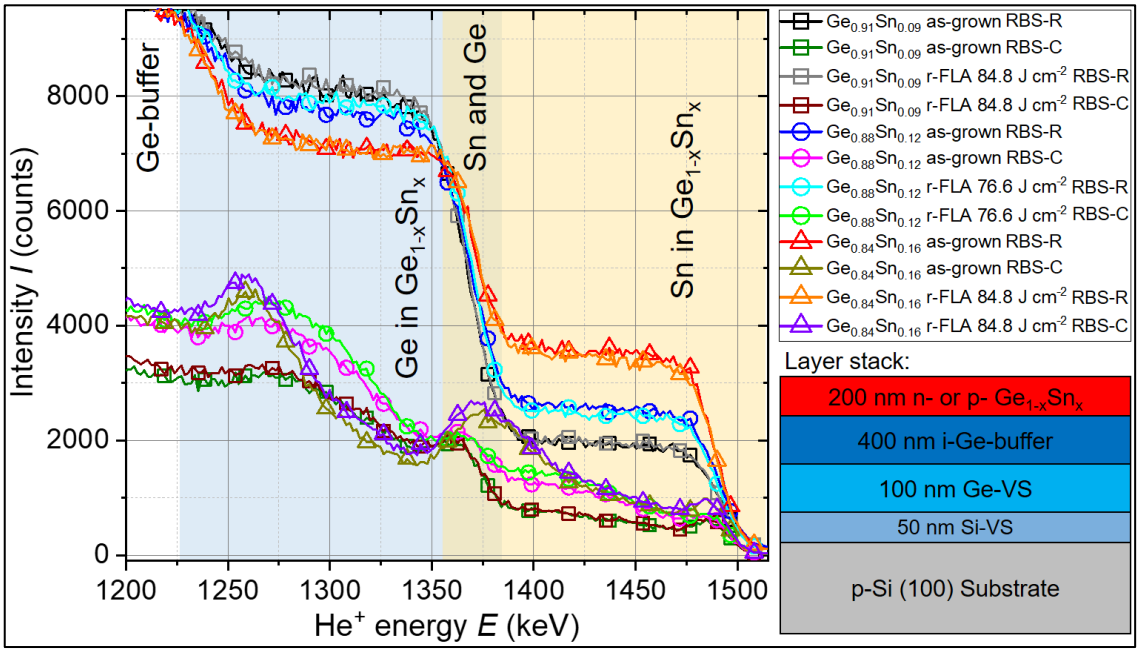


Fig. 4.2 - 2: RBS-R/C results of the $Ge_{1-x}Sn_x$ (x = 9, 12 and 16 at.%) before and after r-FLA and a schematic of the fabricated layer stack. The Ge (1225 - 1380 keV blue background filling) and Sn (1360 - 1515 keV orange background filling) spectra contributions of the $Ge_{1-x}Sn_x$ layer supersaturate each other between 1360 and 1380 keV. The RBS-C measurements are aligned along the [001] axis.

Additionally, SIMNRA [188] simulations on RBS-R spectra were performed to confirm the layer thickness and chemical composition. The results presented in Table 4.2 - 2 confirm the expected layer thickness but reveal a slightly higher Sn concentration compared to the $Ge_{1-x}Sn_x$ layer composition in ref. [93] (see Table 4.2 - 1) calculated by (224) XRD-RSM. These small deviations can be expected due to the high doping level and the different extraction methods. The (224) XRD-RSM calculation approach uses the lattice parameter, which is influenced by many error-causing parameters such as alloy composition (Ge, Sn, and dopants) and strain (see **appendix 8.4**). On the other hand, RBS of the highly Sb-doped $Ge_{1-x}Sn_x$ ($x \approx 9$ and 12 at.%) suffers from the

superposition of Sn and Sb in the spectra. After r-FLA, the Sn concentration in $Ge_{1-x}Sn_x$ (x ≈ 12 and 16 at.%) reduces slightly. This might be related to a slight inhomogeneity across the 35 x 35 mm² grown sample since no Sn segregations or redistributions were observed as possible reasons for the reduced Sn concentration in Fig. 4.2 - 2. The RBS-C spectra in Fig. 4.2 - 2 of the investigated samples show a surface peak in the Ge and Sn contribution, which is a well-known phenomenon caused by surface defects. Afterward, the channeling spectrum reaches a minimum and increases later towards deeper layer depth. The rise is more pronounced for $Ge_{0.88}Sn_{0.12}$ and $Ge_{0.84}Sn_{0.16}$ since the reported strain relaxation (see Table 4.2 - 1) takes place by defect formation. The channeling yield χ is calculated by Eq. 3.6 - 1 and presented in Table 4.2 - 2 for Ge (1335 - 1355 keV) and Sn (1455 - 1475 keV). The values of χ_{Sn} and χ_{Ge} are in the range of 23 to 30%, indicating a generally low $Ge_{1-x}Sn_x$ layer quality. After r-FLA, χ_{Sn} and χ_{Ge} increase slightly compared to their as-grown states. This could be related to a slight defect generation due to strain relaxation events or the formation of small clusters. Therefore, the substitutional fraction of Sn ξ_{Sn} in the $Ge_{1-x}Sn_x$ host lattice is calculated by Eq. 4.2 - 1 [168, 226] and presented in Table 4.2 - 2.

$$\xi_{Sn} = \frac{(1 - \chi_{Sn})}{(1 - \chi_{Ge})} \qquad \text{Eq. 4.2 - 1}$$

ξ_{Sn} is close to 100%, indicating that essentially all the Sn in the film is located in substitutional lattice sites. Only sample $Ge_{0.88}Sn_{0.12}$ has a reduced Sn incorporation rate, which might be related to a slight Sn cluster formation or displacement in the lattice. Apart from that, it can be concluded that the observed low layer quality is mainly caused by growing defects rather than the presence of Sn in interstitial sites. The significant influence of defects can be obtained in the RBS-C spectra of the Ge fraction (1250 – 1300 keV) in $Ge_{0.84}Sn_{0.16}$, where a reasonable number of defects is generated due to strain relaxation. It is also possible to exclude the influence of dopants since the layer quality of the not-presented intrinsic materials is in a similar range.

Table 4.2 - 2: RBS analysis results of the three selected $Ge_{1-x}Sn_x$ (x = 9, 12, and 16 at.%) alloys before and after r-FLA. The Sn concentration c_{Sn} and layer thickness d are simulated by SIMNRA. The minimum channeling yield for Ge χ_{Ge} and Sn χ_{Sn} and the substitutional fraction of Sn ξ_{Sn} is calculated for the integration interval between 1455 and 1475 keV for Sn and 1335 and 1355 keV for Ge.

Sample		$c_{Sn,RBS}$ (at.%)	d (nm)	χ_{Ge} (%)	χ_{Sn} (%)	ξ_{Sn} (%)
$Ge_{0.91}Sn_{0.09}$	as-grown	9.2 ± 0.1	200 ± 5	24.9	25.8	98
	84.8 J cm^{-2}	9.2 ± 0.1	199 ± 5	25.5	26.1	99
$Ge_{0.88}Sn_{0.12}$	as-grown	12.1 ± 0.1	198 ± 5	29.2	28.1	100
	76.6 J cm^{-2}	11.7 ± 0.1	202 ± 5	28.1	31.9	95
$Ge_{0.84}Sn_{0.16}$	as-grown	17.3 ± 0.1	195 ± 5	23.7	23.1	100
	84.8 J cm^{-2}	17.0 ± 0.1	200 ± 5	26.3	25.8	100

µ-Raman spectroscopy is a sensitive and fast method to observe any changes in the layer composition and strain distributions that might occur due to FLA. Fig. 4.2 - 3 a) shows the Ge-Ge optical phonon mode of the three investigated sample types in different annealing states. As expected, the Ge-Ge mode intensity decreases with increasing Sn concentration, and the peak position is shifted to lower wavenumbers. The intensity reduction can be explained by the softening of the Ge-Ge phonon mode and the reduced total amount of Ge-Ge vibration modes with increasing the Sn concentration due to the increasing fraction of Ge-Sn and Sn-Sn modes. Additionally, the higher Sn concentration increases the distance between the Ge atoms in the $Ge_{1-x}Sn_x$ lattice, which reduces the phonon vibration frequency and shifts the peak position towards lower wavenumbers. On the other hand, the compressive strain of each sample reduces the lattice parameter and shifts the peak position towards higher wavenumbers. An additional feature of all Raman spectra is the asymmetrical Ge-Ge mode shape, which is a superposition of a disorder mode [200] due to alloying Ge with Sn and Fano broadening [227] due to constructive resonance of electrically activated dopants.

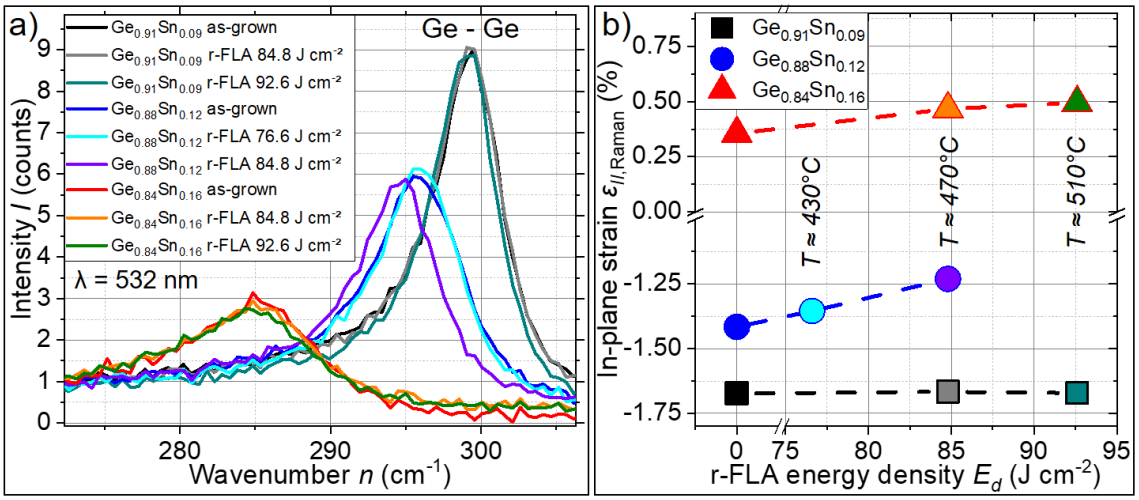


Fig. 4.2 - 3: µ-Raman results of the Ge-Ge phonon mode with two selected r-FLA annealing energy densities close to the melting temperature for $Ge_{1-x}Sn_x$ (x ≈ 9, 12 and 16 at.%) alloys a). Calculated in-plane strain $\varepsilon_{II,Raman}$ as a function of the used r-FLA energy density E_d with a pulse length of 3.2 ms b). The r-FLA temperature T for the selected E_d was approximated by COMSOL simulations on a simplified layer stack (see **appendix 8.9**).

The comparison of the peak position before and after annealing shows a peak shift towards lower wavenumbers for the highest applied r-FLA E_d. This coincides with the significant appearance of the molten fringes on the sample edges. However, the peak position of the samples with slightly lower E_d settings is almost the same as the as-grown state. The in-plane strain $\varepsilon_{II,Raman}$ was calculated using the procedure explained in **appendix 8.5.** The Ge-Ge shift was extracted by Lorentzian fitting of the spectra presented in Fig. 4.2 - 3 a), and the $Ge_{1-x}Sn_x$ alloy composition was measured for each sample by RBS-R. In the case of the $Ge_{0.91}Sn_{0.09}$ and $Ge_{0.88}Sn_{0.12}$ as-grown states, a

slightly larger compressive strain of -1.67% and -1.42% was calculated compared to the XRD results in Table 4.2 - 1. The $Ge_{0.84}Sn_{0.16}$ as-grown state is even slightly in-plane tensile strained. These discrepancies are mainly caused by the different Sn concentrations (RBS or XRD determined), inaccuracies in the Raman disorder parameter and strain coefficient for alloys with high Sn concentrations, and very high doping levels. Hence, $\varepsilon_{II,Raman}$ in Fig. 4.2 - 3 b) can only be analyzed qualitatively. The pseudomorphically grown $Ge_{0.91}Sn_{0.09}$ shows no strain relaxation after r-FLA. On the other hand, the partly strain-relaxed $Ge_{1-x}Sn_x$ with x ≈ 12 and 16 at.% show a proceeding strain relaxation with increasing r-FLA E_d. These fundamental different strain relaxation behaviors between fully pseudomorphic and partly strain-relaxed grown $Ge_{1-x}Sn_x$ goes in line with the *in situ* (224) XRD-RSM thermal treatment strain relaxation experiments performed by Zaumseil et al. [169]. However, in their equilibrium thermal treatment experiment, they observed Sn segregations in CVD-grown $Ge_{1-x}Sn_x$ with x ≈ 9 and 12 at.% at around 400 °C (close to the selected $Ge_{1-x}Sn_x$ growth temperature). These reported temperatures are below our COMSOL simulated r-FLA temperatures (430 - 510 °C), as inserted in Fig. 4.2 - 3 b), due to strong non-equilibrium conditions during FLA. Furthermore, the maximum r-FLA parameters for strong molten fringes also seem to depend on the dopant type since the $Ge_{0.84}Sn_{0.16}$:B could sustain higher temperatures than $Ge_{0.88}Sn_{0.12}$:Sb.

4.2.3 Defect investigation

The defect type, concentration, and depth distribution of the $Ge_{1-x}Sn_x$ alloys before and after r-FLA were investigated by DB-VEPAS and VE-PALS with the setup explained in **section 3.11**. The DB-VEPAS results are presented in Fig. 4.2 - 4. The *S*-parameter in Fig. 4.2 - 4 a) increases as expected with the Sn concentration since incorporating large Sn atoms causes vacancy-like defects. The comparison between the as-grown and annealed states reveals slightly higher defect concentration after r-FLA for all samples. However, the difference is tiny compared to the molten states presented in the previous section (see Fig. 4.1 - 8 a)). The *W*-parameter in Fig. 4.2 - 4 b) shows a strong dependence on the Sn concentration since the environment around the defects changes with increasing Sn concentration. The small difference between the r-FLA-treated samples and the as-grown states indicates no significant changes in the surroundings around the defect due to r-FLA.

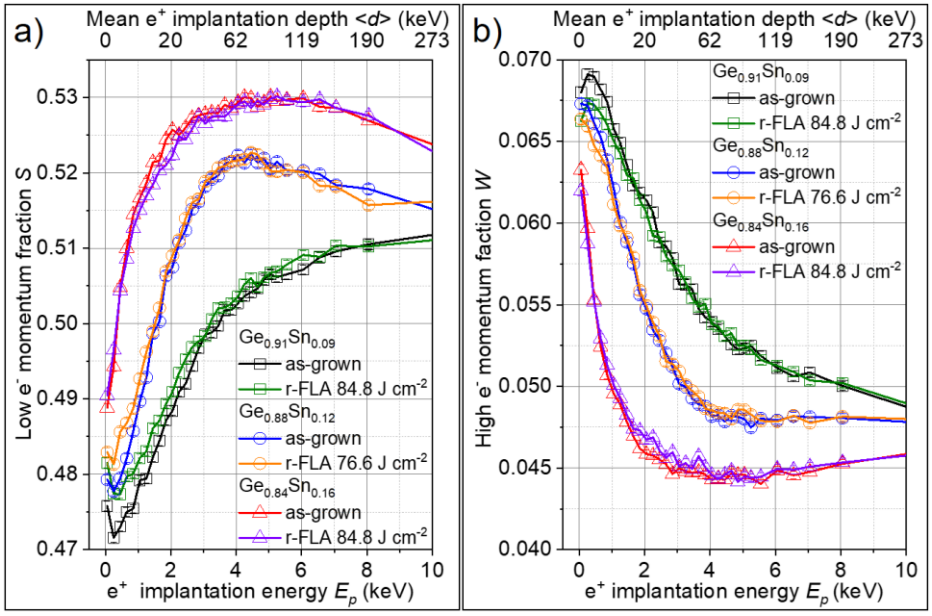


Fig. 4.2 - 4: Doppler broadening results of the low e⁻ momentum fraction *S* a) and the high e⁻ fraction *W* b) for $Ge_{1-x}Sn_x$ (x ≈ 9, 12, and 16 at.%) before and after r-FLA.

In addition, the defect depth distribution of the $Ge_{1-x}Sn_x$ (x ≈ 9, 12, and 16 at.%) in as-grown and annealed states was studied using VE-PALS. Fig. 4.2 - 5 a), d), and g) shows the depth change of the average positron annihilation lifetime τ_{av}, which is the weighted average defect size across sample thickness. All three $Ge_{1-x}Sn_x$ alloys have a relatively low τ_{av} ≈ 300 ps close to the GeSn/Ge interface. Afterward, the lifetime increases towards the surface. This might be related to the observed temperature rise during the growth due to the additional heat of the MBE sources, as reported in ref. [93]. After r-FLA, the τ_{av} increases for all three alloys. To understand this increasing trend in τ_{av}, it is necessary to decompose the τ_{av} into two lifetimes, τ_1 and τ_2, and their relative intensities, I_1 and I_2, as explained in detail in **section 4.1.4**. The deconvolution results are presented in Fig. 4.2 - 5 b), c), e), f), h) and i). For the $Ge_{0.91}Sn_{0.09}$ sample in Fig. 4.2 - 5 b), τ_1 is in the range of V_{Ge}+N x Sn_{Ge} where *N* = 1 or 2. After r-FLA τ_1 is slightly reduced, hence, more Sn atoms are associated with V_{Ge}, but their concentration in Fig. 4.2 - 5 c) is reduced (lower I_1). Nevertheless, more positrons are trapped (I_2 increases) in the larger defect type (τ_2), which is in the range of 3 x V_{Ge}. This means that a reasonable amount of the smaller vacancy-like defects (τ_1) agglomerate to bigger vacancy clusters (τ_2) during r-FLA. This indicates an improvement of the $Ge_{0.91}Sn_{0.09}$ layer after r-FLA due to a vacancy purification process that reduces the overall carrier scattering possibilities. This purification process was already observed for other semiconductor materials like SiTe [222] or heavily doped Ge [228].

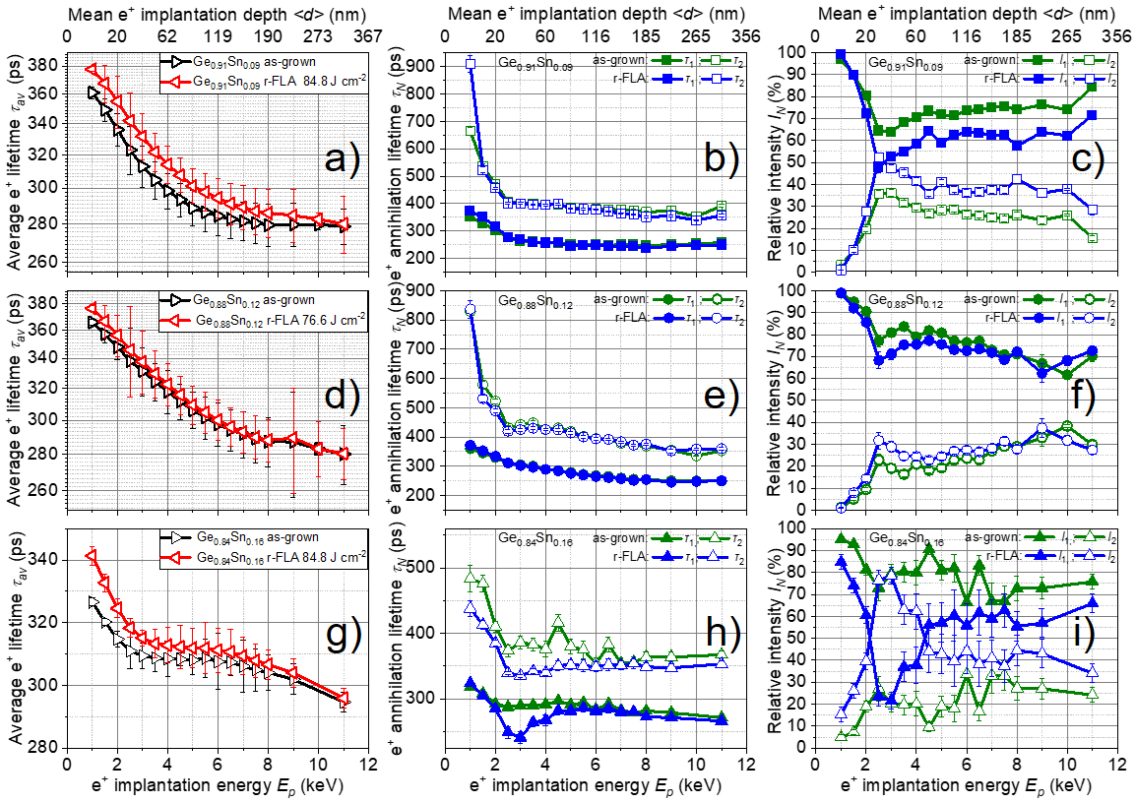


Fig. 4.2 - 5: Positron annihilation lifetime results of the $Ge_{1-x}Sn_x$ alloys x ≈ 9 at.% a) - c), x ≈ 12 at.% d) - f), and x ≈ 16 at.% g)-h) before and after r-FLA. The discrete e⁺ lifetimes τ_1 (closed symbols) and τ_2 (open symbols) in b), e) and h) and their relative intensities I_1 (closed symbols) and I_2 (open symbols) in c), f) and i) are extracted from the average e⁺ lifetime τ_{av} in a), d) and g) by using Eq. 4.1 - 5.

For the $Ge_{0.88}Sn_{0.12}$ sample, the defect lifetime τ_1 in Fig. 4.2 - 5 e) is close to V_{Ge}+1 x Sn_{Ge}, and τ_2 is in the range of a vacancy complex consisting of 3-4 V_{Ge} empty sites. After r-FLA, only a slight increase of τ_2 and I_2 in the first ~100 nm can be obtained, which can be explained by the vacancy agglomeration process. The depth dependence of this effect might be related to the different strain relaxation states in the as-grown layer (see Table 4.2 - 1). In the case of $Ge_{0.84}Sn_{0.16}$, the τ_1 is in the range of 272 - 297 ps (see Fig. 4.2 - 5 h)) that annihilation time is longer than typically observed for single V_{Ge}, but shorter than for 2 x V_{Ge}. Therefore, τ_1 represents bi-vacancy defects decorated by Sn. After r-FLA, τ_1 has a non-monotonic depth profile, which can be caused again by the different strain relaxation states across the depth of the $Ge_{0.84}Sn_{0.16}$ layer. τ_2 is typical for 3 x V_{Ge}, and the intensity I_2 is increased in the strain-relaxed upper part of the layer but decreased in the pseudomorphically grown bottom part after r-FLA, as shown in Fig. 4.2 - 5 i). In other words, after r-FLA, the size of the defects increases, but their concentration is reduced. This combination of increasing vacancy cluster size and

decreasing concentration after r-FLA compensates each other for the DB-VEPAS results in Fig. 4.2 - 4 a) and explains the almost unaffected *S*-parameter after r-FLA.

4.2.4 Dopant distribution and activation

Another influence of r-FLA on highly doped $Ge_{1-x}Sn_x$ could be the activation or deactivation of dopants and their redistribution within the $Ge_{1-x}Sn_x$ matrix. Therefore, Hall-effect measurements in the van-der-Pauw configuration were performed to select samples for SIMS and ECV measurements.

The carrier concentrations, determined by Hall-effect measurements, of the as-grown states in Fig. 4.2 - 6 a) uncover a 150% or 200% higher active carrier concentration than expected from the growing process. In the case of Sb-doped samples, this might be caused by an *in situ* over-doping during MBE. The higher hole concentration n_{h+} in $Ge_{0.84}Sn_{0.16}$ might be a combination of three effects: i) Carrier contribution from slightly p-type doped Ge-buffer. ii) The Ge crucible is made of boron nitride (BN), and long MBE processes at elevated temperatures can introduce B into the Ge source. iii) The higher Sn concentration leads to more Sn-related vacancies, which are supposed to be the reason for the observed p-type doping in unintentionally doped $Ge_{1-x}Sn_x$ alloys (see **section 2.1**). These high carrier concentrations are beneficial for the fabrication of ohmic contacts, as discussed later in **section 6.2**. Note that the measurement results would be more precise after deposition and annealing of metal contact. However, this additional annealing step would smear the influence of the r-FLA treatment.

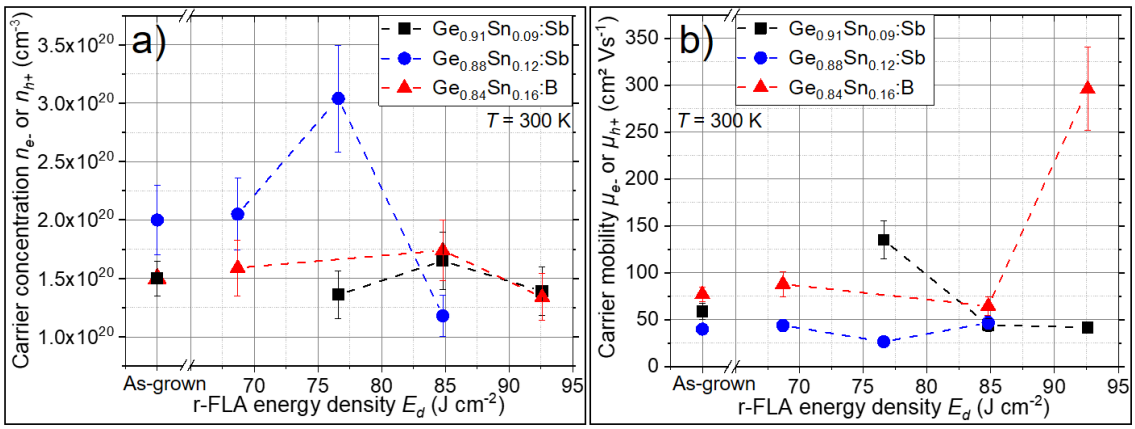


Fig. 4.2 - 6: Calculated Hall-carrier concentration *n* and mobility *μ* for electrons e^- and holes h^+ of the highly *in situ* Sb (1×10^{20} cm^{-3}) and B (1×10^{20} cm^{-3}) doped $Ge_{1-x}Sn_x$ (x ≈ 9, 12, and 16 at.%) alloys with three annealing parameters close to the melting temperature. A 200 nm thick $Ge_{1-x}Sn_x$ layer is selected for the *n* and *μ* calculations (see **appendix 8.6**).

After r-FLA, an increasing trend in the carrier concentration with increasing E_d can be observed. However, the active carrier concentration drops down as soon as the material is overheated with pronounced melting fringes. For $Ge_{0.91}Sn_{0.09}$:Sb annealed at 84.8 J cm^{-2}, an electron concentration of 1.65×10^{20} cm^{-3} was calculated, which is about

10% higher than in the as-grown state. Much better visible is the enhancement in n_{e^-} for $Ge_{0.88}Sn_{0.12}$:Sb after r-FLA at 76.6 J cm^{-2} from 1.50 x 10^{20} cm^{-3} to 3.04 x 10^{20} cm^{-3}. For $Ge_{0.84}Sn_{0.16}$:B n_{h+} reaches the maximum hole concentration of 1.99 x 10^{20}cm^{-3} after r-FLA at 84.8 J cm^{-2}. The Hall-mobilities μ_{e^-} and μ_{h+} presented in Fig. 4.2 - 6 b) are generally relatively low compared to the reported values in Table 1 - 1. This is likely related to the high carrier concentration and moderate material quality of the used $Ge_{1-x}Sn_x$ alloys, which lead to a reduced mean free path length. The higher mobilities of the overheated samples can be caused by the deactivation of dopants due to the formation of dopant clusters or vacancies. Since this is an undesired effect, the samples with the highest carrier concentration were selected for depth profiling.

In the next step, the total donor and acceptor depth distributions before and after r-FLA were determined using SIMS, while the active depth carrier distribution was determined using ECV measurements. The TOF-SIMS measurements are performed with the setup in **section 3.8**, and the results are presented in Fig. 4.2 - 7 a), b), and c). Each of the presented spectra shows at the sample surface (first 10 nm) an excessive concentration of Sn and Sb and a reduced concentration of Ge and B. This is caused by the stabilization process of the sputter yield on the sample surface and can be ignored in the data analysis. Afterward, the yield was very stable and confirmed the expected concentrations of Ge and Sn. The Sb yield in Fig. 4.2 - 7 a) and b) shows a homogeneous concentration-depth profile before and after r-FLA. In the case of $Ge_{0.84}Sn_{0.16}$:B in Fig. 4.2 - 7 c), the total B concentration has an almost constant depth profile and is about 1.5 x 10^{20} at cm^{-3} before and after r-FLA. This is about 1.5 times higher than the expected growth concentration of 1 x 10^{20} at cm^{-3}, but the higher B concentration is consistent with Hall-effect results (see Fig. 4.2 - 6 a)). Hence, almost all B dopants are electrically activated in $Ge_{0.84}Sn_{0.16}$ independently on the annealing conditions. Since the SIMS spectra in Fig. 4.2 - 7 a) - c) before and after r-FLA are almost identical, it can be concluded that r-FLA with a flash duration of 3.2 ms and E_d below the melting point does not influence the elemental depth distribution of the alloys.

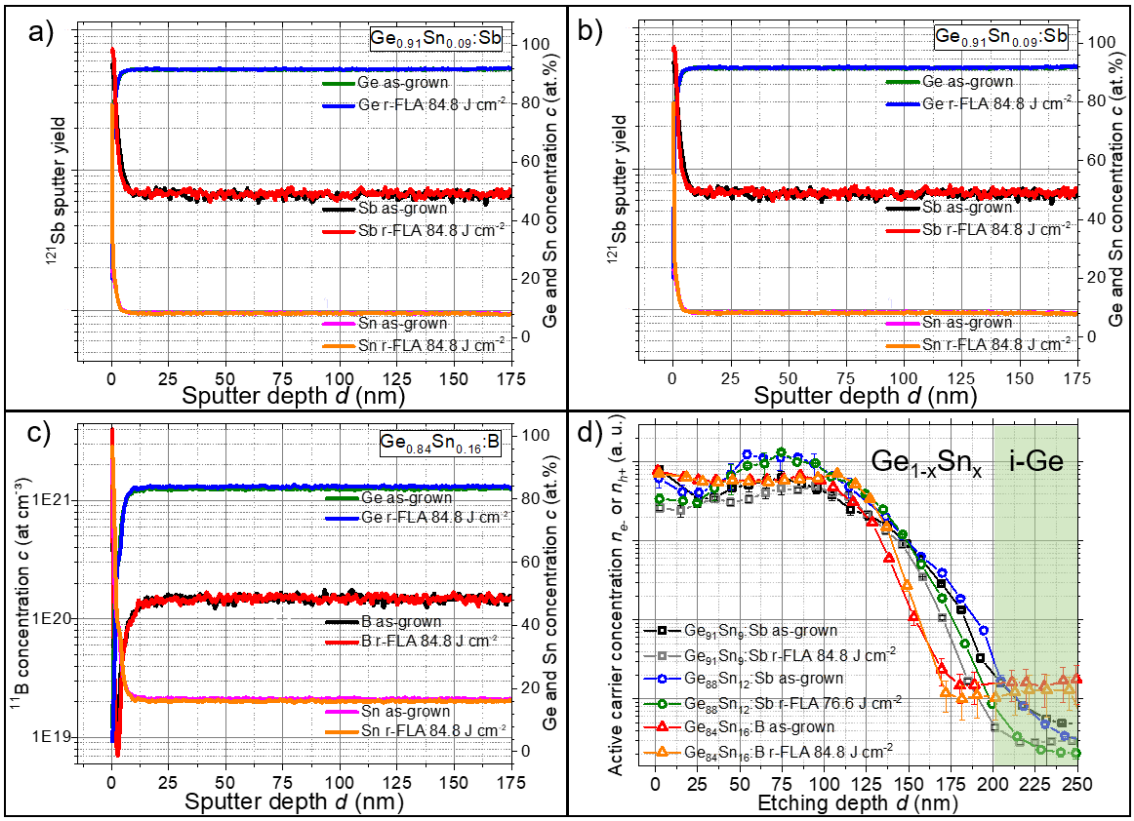


Fig. 4.2 - 7: Elemental depth distribution of the $Ge_{1-x}Sn_x$ alloys before and after r-FLA measured with ToF-SIMS x ≈ 9 at.% a), x ≈ 12 at.% b), x ≈ 0.16 at.% c) and ECV d).

Since the annealing of the electrical contacts for suitable Hall-effect results might cause issues in the result interpretation, ECV measurements were used for active charge carrier depth profiling. The used tool is a Wafer Profiler CVP21 of the company WEP, Germany. For the method, a measurement routine was developed in collaboration with the company WEP, RWTH Aachen, and Ingenierbüro Wolff. More details about the measurement routine and setup can be found in **appendix 8.10**. ECV is based on the formation of a depletion zone at the interface between the semiconductor ($Ge_{1-x}Sn_x$) and the used electrolyte. Under reverse voltage between the semiconductor and the electrolyte, a depletion zone is formed at the contact interface. The capacitance of the Schottky-like contact is used to determine the carrier concentration by a conventional capacitance-voltage approach. However, high carrier concentrations lead to small capacitances and tend to overestimate the active carrier concentration, which was, unfortunately, the case for the highly doped $Ge_{1-x}Sn_x$ samples presented in Fig. 4.2 - 7 d). Therefore, only the relative carrier concentration is shown before and after r-FLA. The Sb-doped samples have a lower carrier concentration within the first 50 nm from the surface than in deeper $Ge_{1-x}Sn_x$ regions. This can be caused by the measurement setup or a reduced electrically active Sb concentration at the sample surface. Between 50 and 100 nm, a constant carrier concentration for all types of samples is achieved. Towards the GeSn/Ge interface, the carrier concentration drops

down again, which might be related to growth defects close to the interface. At depths below 100 nm, the carrier concentration drops down again for an unknown reason. Nevertheless, very similar depth profiles can be obtained by comparing the as-grown and r-FLA-treated counterparts in Fig. 4.2 - 7 d). Therefore, it can be concluded that r-FLA close to the melting point does not change the carrier distribution or the dopant activation level.

4.2.5 Conclusion

Highly p- and n-type doped $Ge_{1-x}Sn_x$ with x ≈ 9 - 16 at.% could be successfully epitaxiallly grown on Ge-buffered Si. Post-growth r-FLA with a flash duration of 3.2 ms and energy densities between 68.7 and 92.6 J cm^{-2} were used to anneal the samples close to their melting points. The used energy density depends on the Sn concentration but also appears to be influenced by their doping and strain relaxation state. RBS investigations have shown that the $Ge_{1-x}Sn_x$ layer compositions are homogeneous before and after r-FLA. Almost all Sn atoms are located in the substitutional sites of the Ge host lattice. However, after r-FLA, a slightly decreased channeling of about 1-2% could be obtained for the partly strain-relaxed $Ge_{0.88}Sn_{0.12}$ and $Ge_{0.84}Sn_{0.16}$. The fully pseudomorphically grown $Ge_{0.91}Sn_{0.09}$ kept their RBS channeling behavior before and after r-FLA. Strain calculations based on µ-Raman measurements confirmed that neither the alloy composition nor strain level was changed in the fully pseudomorphically grown $Ge_{0.91}Sn_{0.09}$ sample due to r-FLA. However, the partly strain-relaxed $Ge_{0.88}Sn_{0.12}$ and $Ge_{0.84}Sn_{0.16}$ samples showed a proceeding strain relaxation due to r-FLA. Positron lifetime measurements revealed an agglomeration of smaller single- or double-vacancies towards larger vacancy clusters. This purification process can improve the carrier mobility but does not reduce the overall density of positively charged defects, which is mainly influenced by the growth process. SIMS, ECV, and Hall-effect measurements were carried out to investigate the influence of r-FLA on the dopant activation and distribution. During the first screening, Hall-effect measurements indicated high active carrier concentrations before and after r-FLA. The obtained SIMS and ECV depth profiles are very similar before and after annealing. This confirms that the selected r-FLA parameters are short enough to avoid elemental redistribution or deactivation of dopants. However, the very high active carrier concentrations measured by the Hall-effect and ECV suggest that most of the dopants are already activated in the as-grown state. Therefore, no further activation of dopants could be obtained after r-FLA.

Overall, it is possible to conclude that the $Ge_{1-x}Sn_x$ layer quality is mainly influenced by their growth conditions. Apart from the vacancy agglomeration/purification process, no

significant improvements can be obtained after post-growth r-FLA with a pulse length of 3.2 ms. Further experiments are necessary to investigate if the layer quality can be improved when longer pulses are used. On the other hand, r-FLA at around 470 °C of the fully pseudomorphically grown $Ge_{0.91}Sn_{0.09}$ did not degrade any of the investigated properties. This observation opens the opportunity to use FLA as an effective approach to achieve ohmic contacts and to improve the interface between gate oxides in device fabrication processes, as further discussed in **Chapter 6**.

5 Fabrication of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys on SOI

The fabrication of lateral thin film devices on an isolated carrier wafer is an established approach to achieve excellent device performance [229, 230]. However, the direct fabrication of $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ on insulators is very challenging because of the low thermal stability of the alloys. Only one research group from the National University of Singapore could show a proof of concept fabricating a single-crystalline GeSnOI with a bond and etch-back approach. In practice, they transferred $Ge_{0.88}Sn_{0.12}$ on ZrO_2 [231] and Al_2O_3 / $Ge_{0.93}Sn_{0.07}$ on SiO_2 [232] or $Ge_{0.96}Sn_{0.04}$ on SiO_2 [233] and etched back the former carrier wafer and Ge-buffer. However, this approach needs further optimization in reproducibility and upscalability. An alternative approach to benefit from the insolated substrates might be the fabrication of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on cheap and commercially available silicon on insulator (SOI) wafers, which will be discussed in this chapter. **Section 5.1** deals with the fabrication of *ex situ* doped $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys via ion beam implantation and FLA. The second approach, evaluated in **section 5.2**, tackles the direct MBE growth of thin *in situ* doped $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ layers on SOI. The fabricated samples are investigated by RBS-R/C, µ-Raman, TEM, XRD, SIMS, and Hall-effect measurements.

5.1 Alloy fabrication with ion beam implantation and FLA

High-fluence ion beam implantation into Ge, $Si_{1-y}Ge_y$, $Ge_{1-x}Sn_x$, or $Si_{1-x-y}Ge_ySn_x$ alloys comes with some challenges, like i) maintaining a smooth surface during ion implantation and ii) overcoming thermal limitations in the recrystallization process, when the dopant concentration exceeds the equilibrium solubility. Especially high concentrations/fluences of heavy elements, like Sn, can damage the surface significantly, and the limited miscibility of the Sn-containing alloys restricts the application of conventional recrystallization annealing approaches like RTA. Some work about the fabrication of single-crystalline $Ge_{1-x}Sn_x$ [102, 104, 142, 234, 235] and $Si_{1-x-y}Ge_ySn_x$ [103] alloys by ion beam implantation in thick films and recrystallization by non-equilibrium thermal treatments were published in the last years. Based on these preliminary studies, few measures to improve the final layer qualities can be deduced.

i) Surface quality:

High-fluence implantation in Ge-based alloys can create deep pits/voids, as shown in Fig. 5.1 - 1 a) by the cross-sectional TEM image and top-view SEM (inset), after implantation of Sn. These pits appear as honeycomb-like structures from the top-view and increase in size and depth with increasing Sn fluence (not shown). Their origin is

mainly attributed to vacancy cluster formation in amorphous Ge during ion implantation. Simultaneously, sputtering reduces the total layer thickness but has a minor influence on the pit formation [236]. Similar implantation pits were also reported for high-fluence implantation of other elements into Ge [236, 237] or the more stable Si [238] substrates. Hence, the pit formation is rather an implantation-related phenomenon than Sn-specific, and the layer stability can be improved by increasing the Si fraction in $Si_{1-y}Ge_y$ or $Si_{1-x-y}Ge_ySn_x$ alloys.

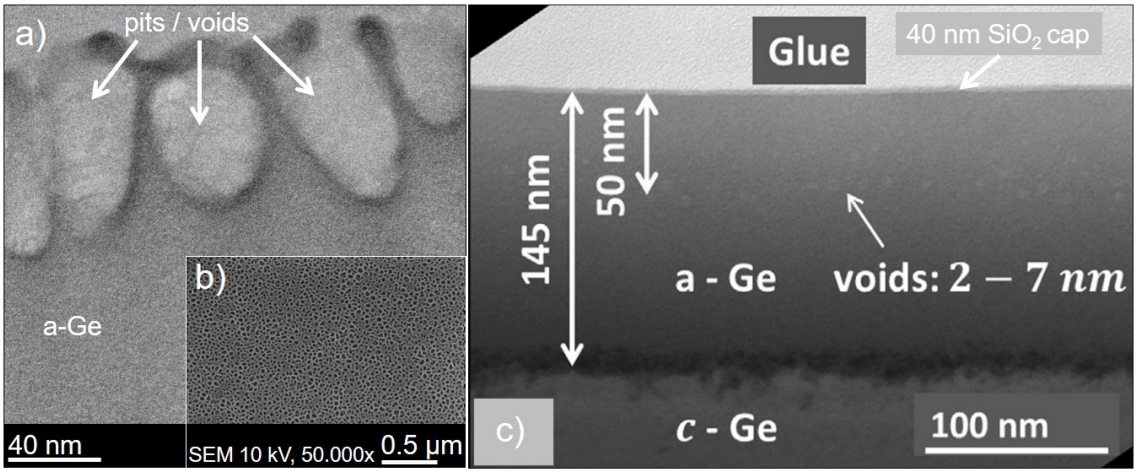


Fig. 5.1 - 1: Cross-sectional TEM image a) of room temperature implanted Ge with Sn (E = 250 kV, D_i = 4 x 10^{16} cm^{-2}) and a representative SEM plane view of the defected Ge surface b). Cross-sectional TEM image of Ge with an SiO_2 capping layer after Sn implantation (E = 120 kV, D_i = 3 x 10^{16} cm^{-2}) with a maintained smooth surface after implantation c) [239].

In order to overcome this pit-formation challenge, a few measures are suggested, like inserting capping layers, reducing the temperature during the implantation, and limiting the ion flux. Stable CMOS-compatible capping layers for group IV semiconductors are Si [240], SiO_2 [104, 142, 241], and Si_3N_4 [241]. Other selection parameters are recoil implantation effects and removability of the capping layers after processing. Recoil implantation leads to an elemental intermixing at the interface between the substrate and capping layer, where some atoms of the capping layer are pushed into the material beneath. This minor effect might be negligible in the case of pure Si caps for Si-containing layers like $Si_{1-y}Ge_y$. Nevertheless, recoil implantation of O and N atoms can lead to oxygen [239] and nitrogen [242] cluster formation in the implanted layer. Both cluster types can reduce the carrier mobility and make the recrystallization more difficult. An example of a successfully maintained smooth surface using an SiO_2 capping layer is shown in Fig. 5.1 - 1 b). However, the authors recognized oxygen-containing voids down to a 50 nm depth, which increases their size by increasing Sn fluence [239]. Interestingly, for shallow N doping, a reduced B [243] and P [244, 245] dopant non-Fickian (anomalous) diffusion during annealing was reported. After the implantation, the capping layers should be removed preferentially using selective wet etching. Pure Si capping

layers can be etched with high selectivity using tetra-methyl-ammonium-hydroxide (TMAH) with high selectivity. Unfortunately, removing Si in this way must be done carefully because the etchant can also etch the Si-containing layer beneath [246]. SiO_2 is easy to remove with diluted HF, and Si_3N_4 is removable with hot phosphoric acid (H_3PO_4) [247] or concentrated HF [248]. Both HF and H_3PO_4 are almost neutral to Si, Ge, $Si_{1-y}Ge_y$, $Ge_{1-x}Sn_x$, and $Si_{1-x-y}Ge_ySn_x$ alloys. Under consideration of these two factors, Si_3N_4 was selected as a capping layer for the following experiments.

ii) Recrystallization process:

Most of the results published in the open literature use nanosecond PLA (see **section 2.4.3**) for post-implantation recrystallization. However, this approach seems to have limitations for higher Sn concentrations. Tran et al. reported vertical filaments (similar to those shown in Fig. 4.1 - 3 e)) after PLA (λ = 355 nm for 6 ns) of $Ge_{1-x}Sn_x$ (x = 4.8, 5.25 and 6 at.%) [142] and significant Sn redistributions in the $Ge_{0.91}Sn_{0.09}$ layer [239]. Additionally, the intermixing of O from the SiO_2 cap with Ge (see Fig. 5.1 - 1 c)) can cause an amorphous surface layer after PLA [239]. In the case of r-FLA at E_d = 65 J cm^{-2} for 3.2 ms of $Ge_{0.955}Sn_{0.045}$, recrystallization could be achieved by solid-phase epitaxy without redistribution of Sn [104]. Additionally, about 95% of Sn atoms were located at Ge substitutional sites. Hence, FLA was selected as a recrystallization annealing method for the following experiments.

5.1.1 $Si_{1-x-y}Ge_ySn_x$ formation via implantation and FLA

The bombardment of $Si_{1-y}Ge_y$ with Sn, P, or Ga ions generates collision cascades and can locally amorphize the implanted material when the fluence is above a critical threshold. Especially the nuclear-stopping mechanisms at low ion velocities cause significant crystal damage and increase the temperature locally due to energy transfer from the implanted ion into the target. The enhanced temperature can cause local *in situ* recrystallization events. The competition between amorphization and recrystallization processes leads to parameter-dependent balance. Since the solid solubility of α-Sn in $Si_{1-x-y}Ge_ySn_x$ alloys is significantly lower than in the binary $Ge_{1-x}Sn_x$ case (see Fig. 2.1 - 1), it seems beneficial to suppress *in situ* recrystallization processes at elevated temperatures during ion implantation. This can be done by reducing the ion current density, inserting implantation breaks, and applying external cooling [104, 235, 239].

The first proof of concept experiments for $Si_{1-x-y}Ge_ySn_x$ alloys fabrication by Sn implantation and FLA were performed with a 600 nm thick $Si_{0.28}Ge_{0.72}$ layer grown on Si by MBE at IHP Frankfurt (Oder). Then co-implantation of Sn (E = 250 kV,

D_i = 1 x 10^{16} cm^{-2}, R_p ≈ 100 nm, T < 100 °C) and P (E = 80 kV, D_i = 3 x 10^{15} cm^{-2}, R_p ≈ 80nm, T < -100 °C) was performed at Maria Curie-Sklodowska University in Lublin (see **section 3.2**) with the ion beam current density below 1 µA cm^{-2} to limit sample heating during the implantation process. After the implantation, the samples were annealed with r-FLA and investigated with µ-Raman und RBS-R/C (see Fig. 5.1 - 2). The implanted $Si_{1-y}Ge_y$ layer surface was converted into an amorphous state since the selected fluence is higher than the amorphization threshold. This is visible in the absence of Ge-Ge and Si-Ge phonon modes in Fig. 5.1 - 2 a). After r-FLA with a pre-heating of 330 °C for 30 s and a flash length of 3.2 ms with E_d = 72.5 J cm^{-2}, the implanted $Si_{0.28-0.5x}Ge_{0.72-0.5x}Sn_x$ layer recrystallizes. Therefore, after annealing, the Ge-Ge and Si-Ge phonon modes appear in the Raman spectra. In comparison to the as-grown state, the Ge-Ge and Si-Ge peak positions of the implanted and r-FLA annealed state are slightly shifted to lower wavenumbers, which indicates an increase of the in-plane lattice parameter due to the incorporation of Sn atoms into the crystal. RBS-R/C measurements (shown in Fig. 5.1 - 2 b)) are performed to confirm the incorporation of Sn in the $Si_{0.28}Ge_{0.72}$ lattice.

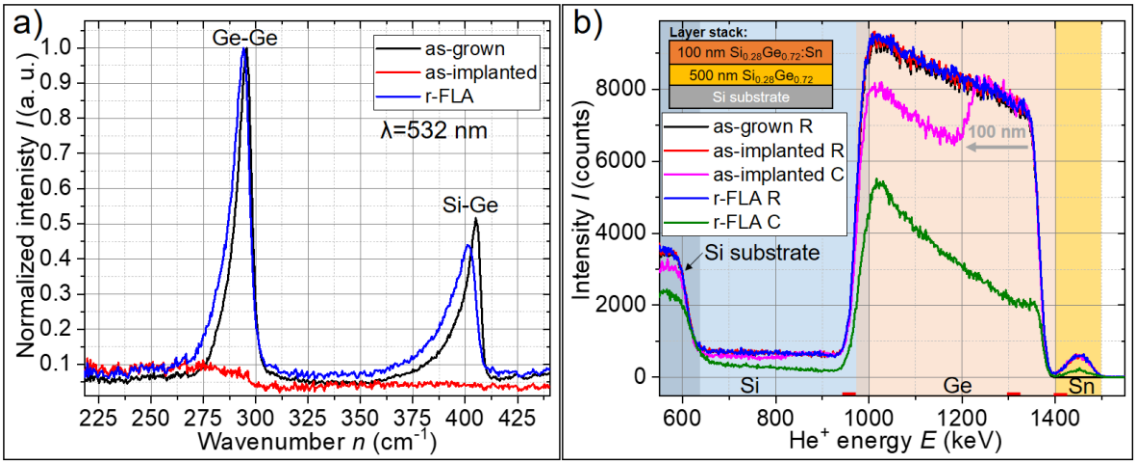


Fig. 5.1 - 2: µ-Raman a) and RBS-R/C measurement b) results of the $Si_{1-x-y}Ge_ySn_x$ alloy in the as-grown state before implantation, after low-temperature Sn and P implantation and after alloy formation via r-FLA with a pre-heating of 330 °C for 30 s and a flash length 3.2 ms with E_d = 72.5 J cm^{-2}. The RBS spectra contain contributions of Sn (1400 - 1500 keV, orange background), Ge (930 - 1400 keV, beige background), and Si (up to 1000 keV, blue background). The RBS-C alignment was carried out along the [001] crystal axis. The red-marked He^+ energy ranges in b) belong to the same $Si_{0.278}Ge_{0.699}Sn_{0.023}$ layer depth used for the RBS-R/C analysis.

The comparison of the Sn fraction of as-grown and as-implanted states proves the successful implantation of about 2.3 at.% of Sn (determined by SIMNRA fitting), which coincides with the expected Sn concentration from the ion beam implantation profile. More information about the implantation parameter can be found in **appendix 8.13**. Furthermore, the RBS-C spectra of the as-implanted state had no channeling in the first 100 nm because of the amorphization during ion bombardment. After r-FLA, the RBS-R

spectra of the as-implanted and annealed states are almost identical. Hence, the selected r-FLA parameters did not cause elemental redistributions. Additionally, the much lower intensity of the RBS-C spectrum for the annealed state proves a successful epitaxial regrow. The analysis of the annealed spectra using Eq. 3.6 - 1 and Eq. 4.2 - 1 reveals an Sn channeling yield χ_{Sn} of 31% and an almost full incorporation of Sn on Ge ($\xi_{Sn,Ge}$ = 95%) and Si ($\xi_{Sn,Si}$ = 100%) sites, respectively. Therefore, it is possible to conclude that ion beam implantation of Sn in $Si_{1-y}Ge_y$ followed by FLA can be used to fabricate SiGeSn alloys.

5.1.2 $Si_{1-x-y}Ge_ySn_x$ on SOI fabrication via implantation and FLA

For the fabrication of thin film $Si_{1-x-y}Ge_ySn_x$ on SOI, commercially available SOI wafers with a 12 nm thick Si layer on a 21 nm SiO_2 were ordered, and a state-of-the-art reduced pressure CVD growth of 15 nm $Si_{0.73}Ge_{0.27}$ was performed at GlobalFoundries Dresden. The layer stack is confirmed with variable angle spectroscopic ellipsometry (see wafer B in **appendix 8.11**). In order to estimate the implantation parameters, simulations with the software code “stopping and range of ions in matter” (SRIM) [249] are performed with different Si_3N_4 capping layer thicknesses of 5, 9, and 15 nm and Sn implantation acceleration voltages between 15 and 50 kV as discussed in **appendix 8.13** in detail. The challenging task is to have, on the one hand, a thick enough capping layer to protect the SiGe surface from degradation (see **section 5.1 i)**) and, on the other hand, the cap should be thin enough to implant the SiGe layer without amorphization of the single-crystalline Si seed layer. In practice, an 8.6 nm thick SiN_x layer was deposited via PECVD at 200 °C and confirmed by ellipsometry. After the low-temperature SiN_x deposition, no significant substrate stress was observed by µ-Raman. Finally, for the Sn implantation, two different fluencies D_I = 5.8 x 10^{14} cm^{-2} (about 1% Sn) and 1.2 x 10^{15} cm^{-2} (about 3% Sn) with an acceleration voltage of 26 kV were selected. The SRIM simulation results for this parameter setup, shown in **appendix 8.13**, correspond to the red curve in Fig. 8.13 - 1. The implantation was performed under an angle of 7° to avoid channeling of the implanted ions, and the sample holder was actively cooled with liquid nitrogen.

5.1.3 Recrystallization of $Si_{1-x-y}Ge_ySn_x$ on SOI by FLA

After the ion implantation, samples were annealed with preheated r-FLA at E_d between 60 and 150 J cm^{-2} and flash lengths of 3.2, 6, and 20 ms. Afterward, the material is investigated with µ-Raman, RBS-R/C, XRD, and TEM. Representative results of the sample series implanted with 3 at.% Sn will be discussed in this section.

An overview of the three different fabrication states (as-grown, as-implanted, and recrystallized by r-FLA) can be obtained from cross-sectional TEM results presented in Fig. 5.1 - 3. TEM images of the as-grown state in Fig. 5.1 - 3 a) - c) show the expected layer stack before implantation and confirm the fabrication of an almost homogeneous high-quality $Si_{0.73}Ge_{0.27}$ layer. After the implantation, regular recurring amorphous pits or wave-like structures appear along the $Si_{1-y-x}Ge_ySn_x$ layer in Fig. 5.1 - 3 d). The interface between the amorphous and crystalline structure is highlighted in Fig. 5.1 - 3 e) and shows a slightly defective but still crystalline $Si_{1-y-x}Ge_ySn_x$ layer next to the amorphous part. The origin of these amorphous structures might be caused by the interplay between the selected dose, current density, implantation depth, heat transfer, sample cooling efficiency, and alloy composition, which caused locally different amorphization or *in situ* recrystallization conditions. Such structures have not yet been reported in the literature. However, the amorphous structures do not influence the surface roughness. Additionally, the Si seed layer could be maintained as single-crystalline. The corresponding EDXS analysis in Fig. 5.1 - 3 f) and g) shows a weak but homogeneous Sn distribution in the $Si_{1-y-x}Ge_ySn_x$ layer. At this stage, it must be mentioned that the X-ray nitrogen-$K_{\alpha1,2}$-Lines located at 392 eV overlap with the Sn-$M_{\zeta2}$ line at 397 eV [250]. Therefore, a stronger Sn contrast appears in the Sn-implanted SiN_x capping layer due to the superposition of these lines.

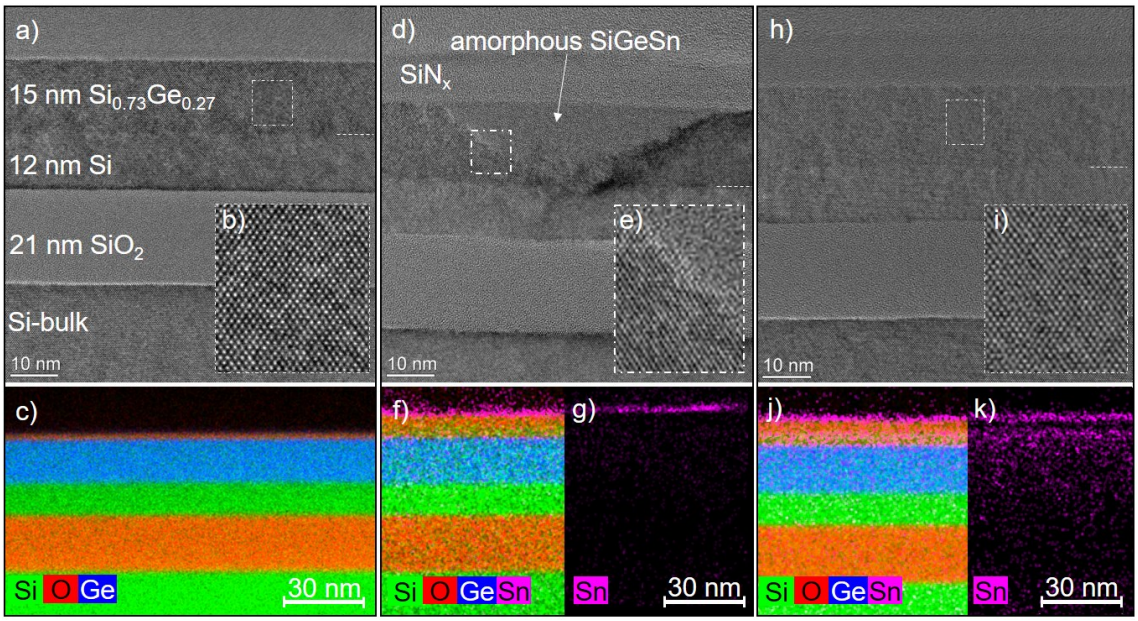


Fig. 5.1 - 3: HR-TEM images (a), b), d), e), h), and i)) and EDXS mappings of the $Si_{1-x-y}Ge_ySn_x$ on SOI in the as-grown state (a) - c)), in the as-implanted state with 3 at.% Sn (d) - g)) and after r-FLA with a peak pre-heating temperature of 570 °C and flash parameter E_d = 120 J cm^{-2} for 6 ms (h) - k)). The SOI and $Si_{1-x-y}Ge_ySn_x$ layer interface is highlighted with a white dashed line on the right edge in a), d), and h). The insets b), e), and i) are enlargements of the outlined areas in their corresponding images a), d), and h), respectively.

After r-FLA, the $Si_{1-y-x}Ge_ySn_x$ layer is completely recrystallized, and the sharp interface between $Si_{1-y-x}Ge_ySn_x$ and the SOI wafer can be maintained as visible in Fig. 5.1 - 3 h) and j). Fig. 5.1 - 3 i) highlights the good crystal quality without any indication of local Sn segregations in the whole TEM lamella. The absence of Sn-segregations is also confirmed by GI-XRD measurements, as shown in **appendix 8.14**. However, the TEM lamella covers only a small portion of the entire sample, and the thin layer thickness, in combination with the small amount of Sn, makes it very difficult to completely exclude Sn segregations.

The influence of different flash parameters at a constant peak pre-heating level of 570 °C will be discussed in the following based on three representative r-FLA annealing pulse lengths (3.2, 6, and 20 ms) and their resulting energy densities of 60, 120, and 150 J cm^{-2}. Their corresponding annealing temperatures can be obtained from Table 5.1 - 1.

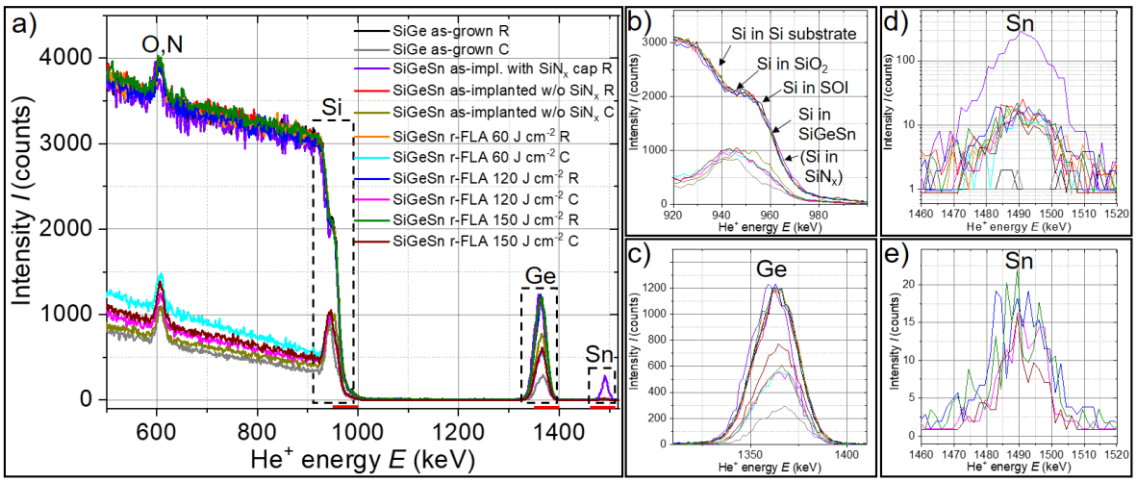


Fig. 5.1 - 4: RBS-R/C results of the SiGe as-grown, as-implanted (with and without SiN_x cap) and after r-FLA with peak pre-heating of 570 °C and energy densities of 60 J cm^{-2} for 3.2 ms, 120 J cm^{-2} for 6 ms and 150 J cm^{-2} for 20 ms a). Enlargements of the SiGeSn related spectra fractions of Si b), Ge c), and Sn d) and e).

The RBS-R/C measurements in see Fig. 5.1 - 4 were performed to approximate the implanted Sn concentration and to evaluate the Sn incorporation in the lattice. The RBS spectra contain contributions from Sn (1460 – 1520 keV), Ge (1330 – 1400 keV), Si (200 – 1000 keV), and O / N (580 – 620 keV) as allocated in Fig. 5.1 - 4 a). The broad Si contribution comes from the whole layer stack (see Fig. 5.1 - 4 b)) and is a mixture of the contributions from i) Si in SiN_x at the surface (case for "SiGeSn as-implanted sample with SiN_x cap" sample), ii) Si in the $Si_{1-x-y}Ge_ySn_x$ alloy, iii) Si of the top SOI layer, iv) Si in the buried oxide (BOX) SiO_2 layer and v) Si of the bulk Si substrate. For a detailed comparison of the $Si_{1-x-y}Ge_ySn_x$ layer properties, the channeling yield χ and the occupation of Sn on Ge or Si sites are calculated and presented in Table 5.1 - 1. The SiGe as-grown RBS-R/C spectra confirm the absence of any Sn in the SiGe layer since

the Sn contribution in Fig. 5.1 - 4 d) is almost zero. Furthermore, the strong channeling of Si (χ_{Si} = 27.2%) and Ge (χ_{Ge} = 25.7%) in Fig. 5.1 - 4 b) and c) confirms the single-crystalline nature of the epitaxially grown $Si_{0.73}Ge_{0.27}$ layer. An additional r-FLA treatment of the SiGe as-grown material resulted in an improved crystal structure since χ_{Si} and χ_{Ge} could be further reduced Table 5.1 - 1. After implantation, a significant Sn signal appeared for the as-implanted state with the SiN_x capping layer. This confirms the implantation of Sn. However, after the removal of the SiN_x layer by etching with 40% HF:DI for 1 min, the Sn contribution is significantly reduced (see Fig. 5.1 - 4 d)). This indicates that a significant amount of Sn was implanted in the SiN_x cap, which coincides with the EDXS results in Fig. 5.1 - 3 g). A poor channeling (χ_{Si} = 48.9%, χ_{Ge} = 63.3%, and χ_{Sn} = 70.6%) could be measured in the as-implanted state due to the *in situ* recrystallization during the implantation process (see Fig. 5.1 - 3 d)). After r-FLA and SiN_x removal, the Ge and Sn peak shape is similar to the as-implanted state. The absence of peak shoulders towards lower He^+ backscattered energies confirms a successful suppression of Ge and Sn diffusion into the top SOI layer. Additionally, the channeling properties of Si ($\chi_{Si} \approx 40\%$) and Ge ($\chi_{Ge} \approx 47\%$) are in a similar range for all three annealing conditions. Compared to the as-implanted state, χ_{Si} and χ_{Ge} are significantly lower after r-FLA because of the recrystallization during r-FLA. With increasing r-FLA energy densities, the χ_{Sn} is further reduced, which indicates an improved Sn incorporation on substitutional lattice sites towards higher temperatures. The RBS-R/C results of the fully recrystallized r-FLA 120 J cm^{-2} with a flash length of 6 ms and 150 J cm^{-2} with a flash length of 20 ms are separately shown in a linear scale Fig. 5.1 - 4 e). In both cases, the incorporation of Sn in the SiGe layer can be confirmed, which is also reflected in the calculated Sn incorporation on Si ($\xi_{Sn,Si}$) and Ge ($\xi_{Sn,Ge}$) substitutional sites.

Table 5.1 - 1: RBS-R/C analysis results of $Si_{0.73}Ge_{0.27}$ as-grown reference, $Si_{0.73}Ge_{0.27}$ reference after r-FLA with 120 J cm^{-2} for 6 ms, SiGeSn alloys in the as-implanted and r-FLA-treated states. The r-FLA peak temperature T_p is simulated by COMSOL (see **appendix 8.9**). The minimum channeling yield for Si χ_{Si}, Ge χ_{Ge}, and Sn χ_{Sn}, as well as the substitutional fraction of Sn on substitutional Si sites $\xi_{Sn,Si}$ and on substitutional Ge sites $\xi_{Sn,Ge}$, is calculated by Eq. 3.6 - 1 and Eq. 4.2 - 1. An integration interval between 950 and 1000 keV for Si, 1340 and 1390 keV for Ge, and 1465 and 1515 keV for Sn was used.

Sample	*r-FLA T_p (°C)*	χ_{Si} (%)	χ_{Ge} (%)	χ_{Sn} (%)	$\xi_{Sn,Si}$ *(%)*	$\xi_{Sn,Ge}$ *(%)*
SiGe as-grown	-	27.2	25.7	-	-	-
SiGe r-FLA 120 J cm^{-2} 6 ms	880	26.2	23.8	-	-	-
SiGe:Sn as-implanted w/o SiN_x	-	48.9	63.3	70.6	57.5	80.1
SiGeSn r-FLA 60 J cm^{-2} 3.2 ms	730	39.6	48.3	72.8	45.0	52.4
SiGeSn r-FLA 120 J cm^{-2} 6 ms	880	39.0	47.2	66.1	55.5	64.1
SiGeSn r-FLA 150 J cm^{-2} 20 ms	960	39.6	47.3	60.4	65.5	75.1

In order to determine the SiGeSn alloy composition, additional RBS-R measurements were performed with an incident angle of 80° on samples after SiNx removal. The SIMNRA simulation results reveal a chemical composition of approximately $Si_{0.681}Ge_{0.308}Sn_{0.011}$. Further details about the simulation can be obtained from **appendix 8.14**.

Since the incorporation of Sn is very small, it is necessary to confirm the obtained RBS results by µ-Raman and XRD. The µ-Raman spectra of the different fabrication states, shown in Fig. 5.1 - 5 a), have Si-Si (≈ 520.7 cm^{-1}) vibrational modes from the SOI substrate and modes originating from the $Si_{1-x-y}Ge_ySn_x$ ($y > 0$) layer, like Ge-Ge (≈ 300 cm^{-1}), Si-Ge (≈ 410 cm^{-1}), Si-Si*5 (≈ 430 cm^{-1}) [251, 252] and Si-Si (≈ 510 cm^{-1}). The (004) HR-XRD scans in Fig. 5.1 - 5 b) contain a broad $Si_{1-x-y}Ge_ySn_x$ (004) reflection between 67° and 68.5°and sharp Si (004) reflections of the substrate and the top SOI layer at 69.15°, which is close to the literature value of pure Si at 69.13° [73].

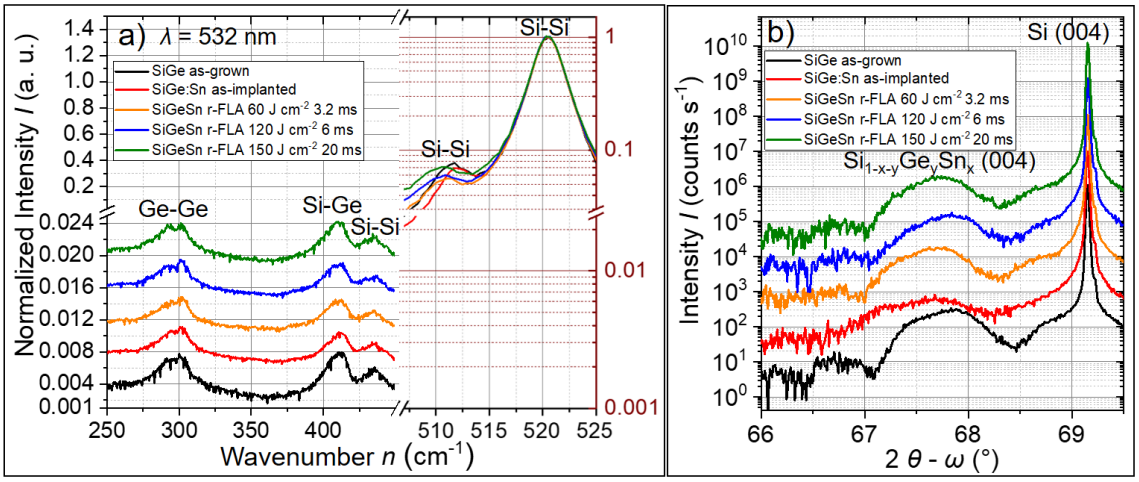


Fig. 5.1 - 5: µ-Raman a) and (004) HR-XRD b) results of the $Si_{1-x-y}Ge_ySn_x$ alloy in the as-grown state, after implantation and after r-FLA with a peak pre-heating temperature of 570 °C and r-FLA parameters of E_d = 60, 120 and 150 J cm^{-2} with a pulse length of 3.2, 6 and 20 ms. The curves gained an offset in their intensity for better visibility.

Both techniques show broad modes or reflections related to the $Si_{1-x-y}Ge_ySn_x$ layer, which indicates either a strain distribution or a chemical gradient across the layer thickness. In the case of the SiGe as-grown state, a fully pseudomorphical growth of $Si_{0.73}Ge_{0.27}$ on SOI can be assumed, which is also later confirmed by (224) XRD-RSM in Fig. 5.1 - 6 a). Therefore, the general broadness is related to the small layer thickness, a small chemical gradient across the SiGe layer, or resulting strain conditions. Especially a large strain gradient in the pseudomorphically grown layer can cause a splitting of the transverse optical (TO) and longitudinal optical (LO) modes in the Raman spectra. The chemical

*5 The Si-Si modes at around 430 cm^{-1} are known from $Si_{1-x}Ge_y$ alloys. Their origin is attributed to Si-Si modes in the neighborhood of one or more Ge atoms [251, 252].

gradient could not be observed in RBS-R because the layer thickness is close to the resolution limit of the RBS setup. After implantation, all $Si_{1-x-y}Ge_ySn_x$ related Raman modes and (004) reflections have a reduced intensity compared to the SiGe as-grown state since the number of active modes with a distinct frequency or number of coherent lattice planes is reduced due to the local amorphization (see Fig. 5.1 - 3 c)). After r-FLA for 6 ms at E_d = 120 J cm^{-2} or for 20 ms at E_d = 150 J cm^{-2}, the layers are fully recrystallized (see Fig. 5.1 - 3 h) and Fig. 5.1 - 7 b) - c)). Therefore, the intensity of the Si-Si (≈ 510 cm^{-1}) mode and the $Si_{1-x-y}Ge_ySn_x$ (004) reflection increase. Additionally, a peak shift towards lower wavenumbers at the Si-Si (≈ 510 cm^{-1}) mode and an extension to smaller diffraction angles, observed in Fig. 5.1 - 5 b), occur due to the incorporation of Sn in the lattice. Another feature in the (004) HR-XRD scans are Laue oscillations [253] of the $Si_{1-x-y}Ge_ySn_x$ (004) reflections in the SiGe as-grown and after r-FLA at E_d = 120 J cm^{-2} for 6 ms and 150 J cm^{-2} for 20 ms. Visible fringes indicate a high layer quality and a sharp interface between layers [253]. In the case of the $Si_{1-x-y}Ge_ySn_x$ E_d = 60 J cm^{-2} 3.2 ms state, the selected r-FLA parameters are too mild for an entire recrystallization (see Fig. 5.1 - 7 a)). Hence, the intensities in Fig. 5.1 - 5 are lower compared to the fully recrystallized samples. On the other hand, the Si-Si (≈ 510 cm^{-1}) mode shows a similar peak shift towards lower wavenumbers in Fig. 5.1 - 5 a) compared to the other annealing states, which can be related to Sn incorporation or strain relaxation in the already crystalline fraction of the $Si_{1-x-y}Ge_ySn_x$ layer.

(224) XRD-RSM scans are performed since the strain can be responsible for the changes in the µ-Raman and (004) HR-XRD results after r-FLA. Fig. 5.1 - 6 shows the results of the SiGe reference samples in the as-grown state a) and after r-FLA b). The SiGe (224) diffraction has the same in-plane reciprocal lattice parameter as the Si substrate. This confirms a fully pseudomorphical growth of the SiGe layer on the SOI wafer. Furthermore, the broad distribution in q_z is clear evidence of a chemical gradient across the SiGe layer since any strain relaxation would be visible in a q_x-shift towards the black strain relaxation line. The maintenance of the fully compressive strained condition in the SiGe reference after r-FLA in Fig. 5.1 - 6 b) suggests that r-FLA is not the driving force for strain relaxation. On the other hand, the implantation damage in combination with partial *in situ* recrystallization leads to the first relaxation events in the $Si_{1-x-y}Ge_ySn_x$ layer, as shown in Fig. 5.1 - 6 c). After r-FLA for 6 ms at E_d = 120 J cm^{-2} (see Fig. 5.1 - 6 d)), the q_x and q_z distribution is almost the same as in the as-implanted state, but the overall intensity is increased. Similar results could also be obtained for the other r-FLA annealing states, as shown in **appendix 8.15**. Unfortunately, the strain

distribution, in combination with the low intensity, does not allow a quantitative comparison between the different annealing conditions.

By combining the μ-Raman results in Fig. 5.1 - 5 a) with the strain relaxation trend from the (224) RSM in Fig. 5.1 - 6, it is possible to conclude that the Si-Si (≈ 510 cm^{-1}) mode seems to be more affected by Sn incorporation and strain relaxation than the Ge-Ge and Si-Ge modes. This is most likely related to the significantly higher Si concentration in the $Si_{1-x-y}Ge_ySn_x$ (x ≈ 1.1 and y ≈ 30.8 at.%) alloys.

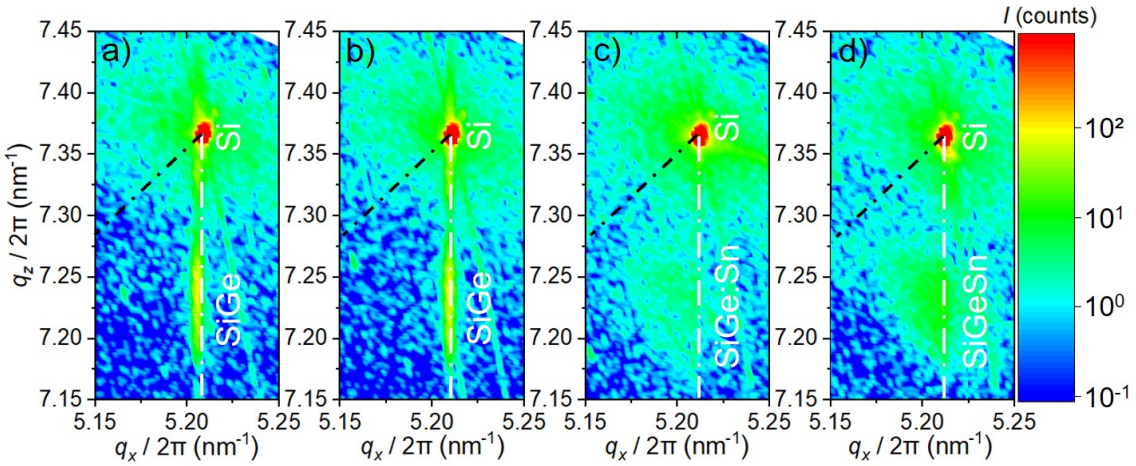


Fig. 5.1 - 6: (224) XRD-RSM of the SiGe reference in the as-grown state a), the SiGe reference after r-FLA for 6 ms at E_d = 120 J cm^{-2} b), $Si_{1-x-y}Ge_ySn_x$ as-implanted Sn c) and after r-FLA for 6 ms at E_d = 120 J cm^{-2} d). The white vertical dash-dot line corresponds to the fully pseudomorphically grown state, and the black dash-dot line is the strain relaxation line for a fully relaxed alloy on Si.

Strain relaxation is usually related to defect formation. Therefore, local defects within the microstructure of the annealed SiGeSn layers were searched for by cross-sectional TEM, as presented in Fig. 5.1 - 7.

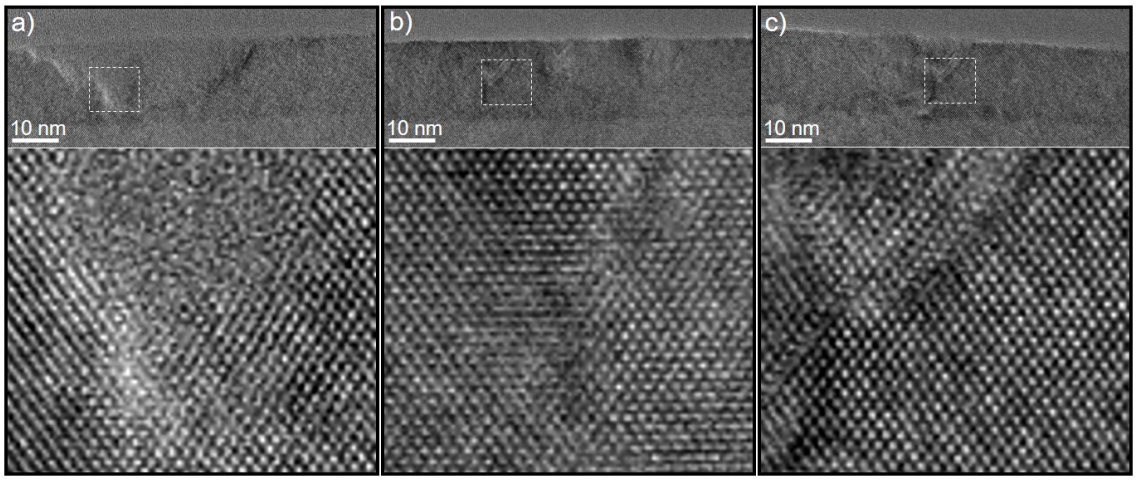


Fig. 5.1 - 7: HR-TEM images of the SiGeSn on SOI layer after r-FLA with 60 J cm^{-2} with 3.2 ms a), 120 J cm^{-2} with 6 ms b) and 150 J cm^{-2} with 20 ms c). Pre-heating was performed for all three samples at peak temperatures of 570 °C. The white square in a) – c) belongs to the enlarged detail image below.

After r-FLA for 3.2 ms with 60 J cm^{-2}, the largest defects are the amorphous contributions in a slightly defected crystal. The amorphous parts are less regularly distributed compared to the as-implanted states, which can be explained by an uncompleted recrystallization due to the small flash E_d. Moreover, this result confirms that the selected pre-heating at around 570 °C does not lead to a recrystallization of the layer. On the other hand, the fully recrystallized states in b) and c) contain few randomly distributed defects such as stacking faults or even forest dislocations in an almost perfect $Si_{1-x-y}Ge_ySn_x$ matrix. The low number of defects explains the small strain relaxation degree. The origin of the “V” shaped “forrest dislocations” is attributed to the pinning of at least two dislocation loops <011> [254]. This suggests a propagation of dislocations during the millisecond thermal treatment. On the other hand, some dislocation might annihilate during thermal treatments, which could explain the improved layer quality for the annealing with a 20 ms pulse length.

5.1.4 P and Ga doping of $Si_{1-x-y}Ge_ySn_xOI$ via implantation and FLA

For the fabrication of transistors like JLFETs (see **Chapter 6**), it is necessary to increase the layer conductivity by doping. However, alloying of SiGe with Sn and co-doping with Ga (for p-type) or P (for n-type) within one step increases the probability of amorphization of the entire Si seed layer. Therefore, the material was first implanted with Sn and recrystallized with r-FLA (E_d =120 J cm^{-2}, 6 ms), as presented in **sections 5.1.2** and **5.1.3**. Afterward, the SiGeSn material was implanted with P (E = 12 kV, 7°, D_I = 7.4 x 10^{13} cm^{-2}) or Ga (E = 20 kV, 7°, D_I = 1.4 x 10^{14} cm^{-2}) and annealed again with r-FLA (E_d =120 J cm^{-2}, 6 ms).

The doping and recrystallization were investigated by µ-Raman, Hall-effect, and TOF-SIMS measurements. Pre-experiments for Ga and P doping of $Si_{0.73}Ge_{0.27}$ on SOI material without an additional capping layer could show an active carrier concentration of 4 x 10^{19} cm^{-3} for Ga and 1 x 10^{19} cm^{-3} for P after r-FLA with 120 J cm^{-2} for 6 ms. Therefore, the implantation energies were adjusted according to the SiN_x layer thickness of 8.6 nm. The selected SRIM simulation results for Sn (E = 26 kV, R_p ≈ 16 nm including 8.6 nm SiN_x, as discussed in **section 5.1.2**), Ga (E = 20 kV, R_p ≈ 15 nm including 8.6 nm SiN_x cap) and P (E = 12 kV, R_p ≈ 15 nm including 8.6 nm SiN_x cap) are converted into a concentration by multiplying the SRIM ion depth profile with the fluence. The obtained depth profiles are added in Fig. 5.1 - 8 a). All three dopants have a high concentration within the fabricated $Si_{1-x-y}Ge_ySn_x$ layer, which should cause amorphization during the implantation. However, after implantation of Ga and P, no significant changes were observed in the µ-Raman spectra, compared to the r-FLA 120 J cm^{-2} with 6 ms state

before P and Ga implantation (see Fig. 5.1 - 5 a)). The Hall-effect measurements, performed after removal of SiN_x by etching in 40% HF:Di for one minute and dopant activation with FLA, revealed an active carrier concentration of only $n_{e^-} \approx 1.5 \times 10^{14}$ cm^{-3} for P and $n_{h^+} \approx 4 \times 10^{17}$ cm^{-3} for Ga. To clarify the obtained µ-Raman and Hall-effect results, ion depth profiles were measured by SIMS before and after annealing, as shown in Fig. 5.1 - 8 a) and b).

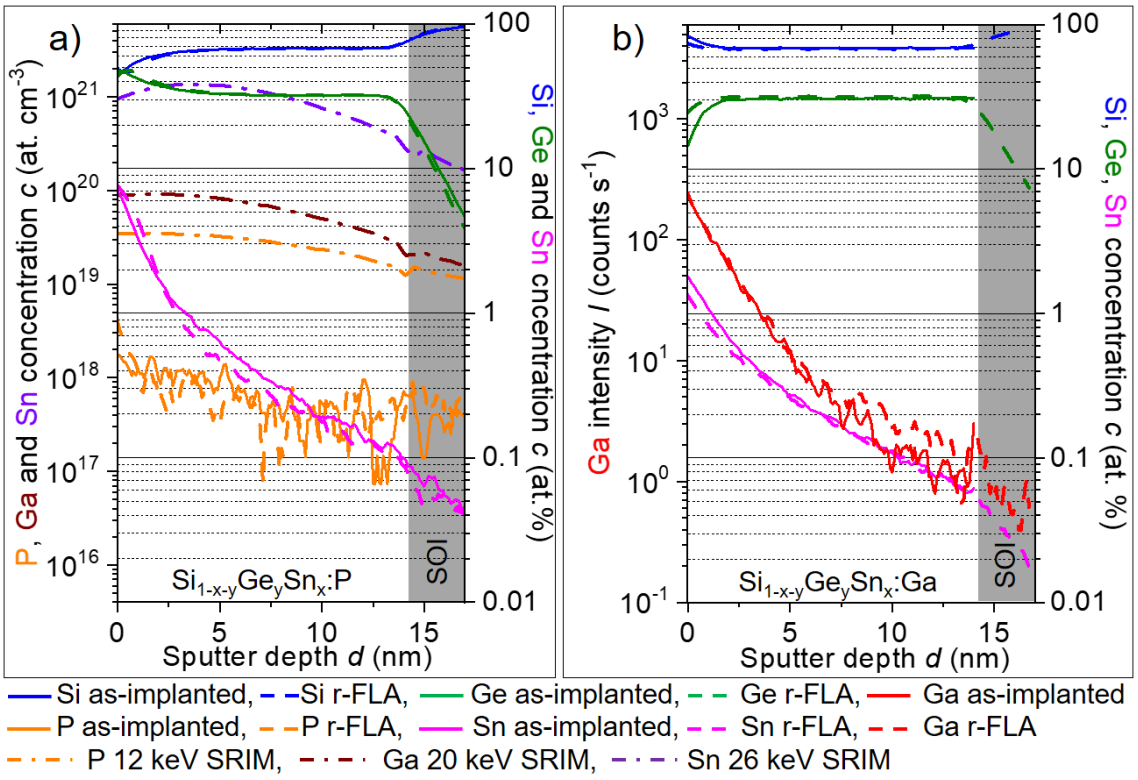


Fig. 5.1 - 8: Elemental depth distribution obtained from TOF-SIMS and SRIM simulations within the SiGeSn layer doped with P a) and Ga b). Compared are the as-implanted states with P or Ga with their r-FLA-treated counterpart with E_d = 120 J cm^{-2} for 6 ms and pre-heating peak temperatures of 570 °C. The targeted implantation depth profiles of Sn, P, and Ga are simulated by SRIM under an implantation angle of 7° and with an 8.6 nm thick SiN_x capping layer and inserted in a) as dash-dot lines.

According to the SIMS results, the depth distribution of all the implanted ion species is shallower than expected. The origin of this discrepancy is not clear yet since the SiN_x capping layer thickness is well determined by TEM (see Fig. 5.1 - 3 d)). However, it must be mentioned that SIMS measurements of these samples are challenging and come with some uncertainties, as explained in detail in **appendix 8.16**. On the other hand, the hypothesis of shallower implantations is supported by i) loss of Sn after SiN_x removal (see Fig. 5.1 - 4 d)), ii) the absence of a significant amorphization obtained by µ-Raman, and iii) the low active carrier concentration by Hall-effect measurements. The comparison obtained elemental depth distributions of the as-implanted and the r-FLA-treated states in Fig. 5.1 - 8 a) and b) proves again the successfully suppressed diffusion of P, Ga, and Sn during the millisecond annealing r-FLA.

5.1.5 Conclusion

The presented results show the general feasibility of fabricating $Si_{1-x-y}Ge_ySn_x$ alloys by ion beam implantation of Sn in $Si_{1-y}Ge_y$ films and recrystallization by FLA. In thick Ge-based films, 2.2% Sn could be fully incorporated into the crystal, but an implantation capping layer and reduced implantation temperatures are required to maintain a good surface quality. In the case of thin films on SOI, a good process control for the capping layer deposition and the implantation steps are necessary to avoid implantation profiles that are too deep or too shallow. In the presented work, about 1% Sn could be partially incorporated into a 15 nm thick $Si_{0.715}Ge_{0.283}$ layer by r-FLA. The amount of implanted Sn can be further increased by adjusting the implantation angle and achieving deeper implantation profiles. Unfortunately, the actual implantation profile in our experiments seems to differ from the SRIM simulation. Furthermore, the Sn implantation causes *in situ* strain relaxation during the implantation. Therefore, it is suggested to reduce the implantation flux and enhance the active cooling during the implantation. Especially the thin implanted layers on SOI suffer from charged surfaces and limited heat dissipation since the buried oxide prevents effective heat and charge dissipation through the substrate. It is shown that the $Si_{0.681}Ge_{0.308}Sn_{0.011}$ layers can be recrystallized by r-FLA with $E_d \approx 120 – 150$ J cm^{-2} and pulse lengths of 6 – 20 ms without any indication of Sn segregations. The shown strain relaxation by the formation of stacking faults and dislocations is mainly related to the ion beam implantation and does not proceed further due to r-FLA. The lower used r-FLA $E_d = 60$ J cm^{-2} could only partially recrystallize the $Si_{0.681}Ge_{0.308}Sn_{0.011}$ layer after Sn ion implantation, even with the help of a short pre-heating of up to 570 °C. The recrystallized structures after r-FLA at 150 J cm^{-2} were mainly free of defects, but the Sn incorporation decreased the overall layer quality compared to the fully pseudomorphically as-grown $Si_{0.73}Ge_{0.27}$ layer.

5.2 MBE and post-growth thermal treatments of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI

In this section, the fabrication approach of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ thin films via direct MBE growth on SOI and post-growth thermal treatments will be discussed. Until the date of this work, there are no publications about the direct growth of thin film $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ on SOI available. In general, the direct growth of such alloys on Si suffers from the large lattice mismatch to Si, the non-equilibrium conditions, and the reduced thermal conduction of the SiO_2 interlayer. Recently, a successful direct growth of 300 nm thick $Ge_{0.978}Sn_{0.022}$ on a virtual Si substrate by MBE was presented [114, 255]. Therefore,

the process seems to be feasible with relatively low defect densities of about ~10^7 cm^{-2} [112], which is in an acceptable range for device-grade applications. A fully pseudomorphic growth of $Ge_{0.978}Sn_{0.022}$ on Si would cause about 4.5% compressive strain, according to Eq. 2.1 - 1 and Eq. 4.1 - 1. In this thesis, the target alloys grown on SOI are $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$, which would cause 5.3% and 1.9% compressive strain, respectively. These strain values are high enough to cause dislocations and stacking faults at the interface between Si and $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ [90, 112] or threading dislocations when the layer exceeds the critical thickness [92]. Therefore, post-growth PLA and FLA are performed to evaluate the possibility of improving the layer quality of the highly mismatched thin films. The $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ layer properties are investigated before and after annealing with µ-Raman, XRD, and RBS, and some particular samples are selected for SIMS, Hall-effect, and TEM analysis.

5.2.1 MBE growth of $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI

For the experiment, a commercially available SOI wafer (see wafer A in **appendix 8.11**) was used. Pre-experiments have shown that conventional removal of native SiO_2 on the SOI surface via thermal desorption creates undesired bowing of the SOI wafer. Therefore, the wafer is diced in 35 x 35 mm^2 pieces, and the native SiO_2 is removed by a 2.5% HF:DI etching for 15 s. Afterward, the SOI material was inserted in the MBE chamber, and the substrate was heated up to 700 °C with a ramp of about 30 K min^{-1}. Then, the temperature was kept constant for 5 minutes to eliminate the H dangling bonds on the Si surface created by HF etching [256]. Thereafter, the substrate temperature was reduced to 160 °C ($Ge_{0.94}Sn_{0.06}$) or 180 °C ($Si_{0.14}Ge_{0.80}Sn_{0.06}$) with stabilization steps at 330 °C for 20 min, 130 °C for 15 min ($Ge_{0.94}Sn_{0.06}$) or 180 °C for 15 min ($Si_{0.14}Ge_{0.80}Sn_{0.06}$). Finally, the MBE growth was performed at around 180 °C ($Ge_{0.94}Sn_{0.06}$) or 200 °C* [6] ($Si_{0.14}Ge_{0.80}Sn_{0.06}$) with a growth rate of 6 nm min^{-1} ($Ge_{0.94}Sn_{0.06}$) or 10 nm min^{-1} ($Si_{0.14}Ge_{0.80}Sn_{0.06}$). Both layers are *in situ* doped with Sb in a targeted concentration of 5 x 10^{19} cm^{-3}. Details about the targeted process parameter can be found in **appendix 8.12**. Afterward, the material is sawed in 10 x 10 mm^2 pieces.

*[6] The temperature on the sample front surface is increased by about 20 °C during the deposition because of the heat influence of the Ge and Sn effusion cells [93]. Therefore, the assumed growth temperatures are higher than the controlled substrate temperature on the sample back side of 160 °C for $Ge_{0.94}Sn_{0.06}$ and 180 °C for $Si_{0.14}Ge_{0.80}Sn_{0.06}$.

5.2.2 Microstructure of as-grown $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$

A microstructural overview of the as-grown $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI is provided by the TEM-based study in Fig. 5.2 - 1. The EDXS mappings in Fig. 5.2 - 1 a) and b) confirm the targeted layer stack and relative homogeneous distribution of Sn within $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$. In the HR-TEM images in Fig. 5.2 - 1 c) and d) as well as their enlargements in e) and f), stacking faults close to the interface can be observed. The microstructure of the $Ge_{0.94}Sn_{0.06}$ is partially crystalline but contains either mis-orientated grains or amorphous inclusions above the interface. The presence of amorphous microstructure features would indicate an epitaxial breakdown during the growth, which appears when the critical thickness for epitaxial growth is exceeded [48].

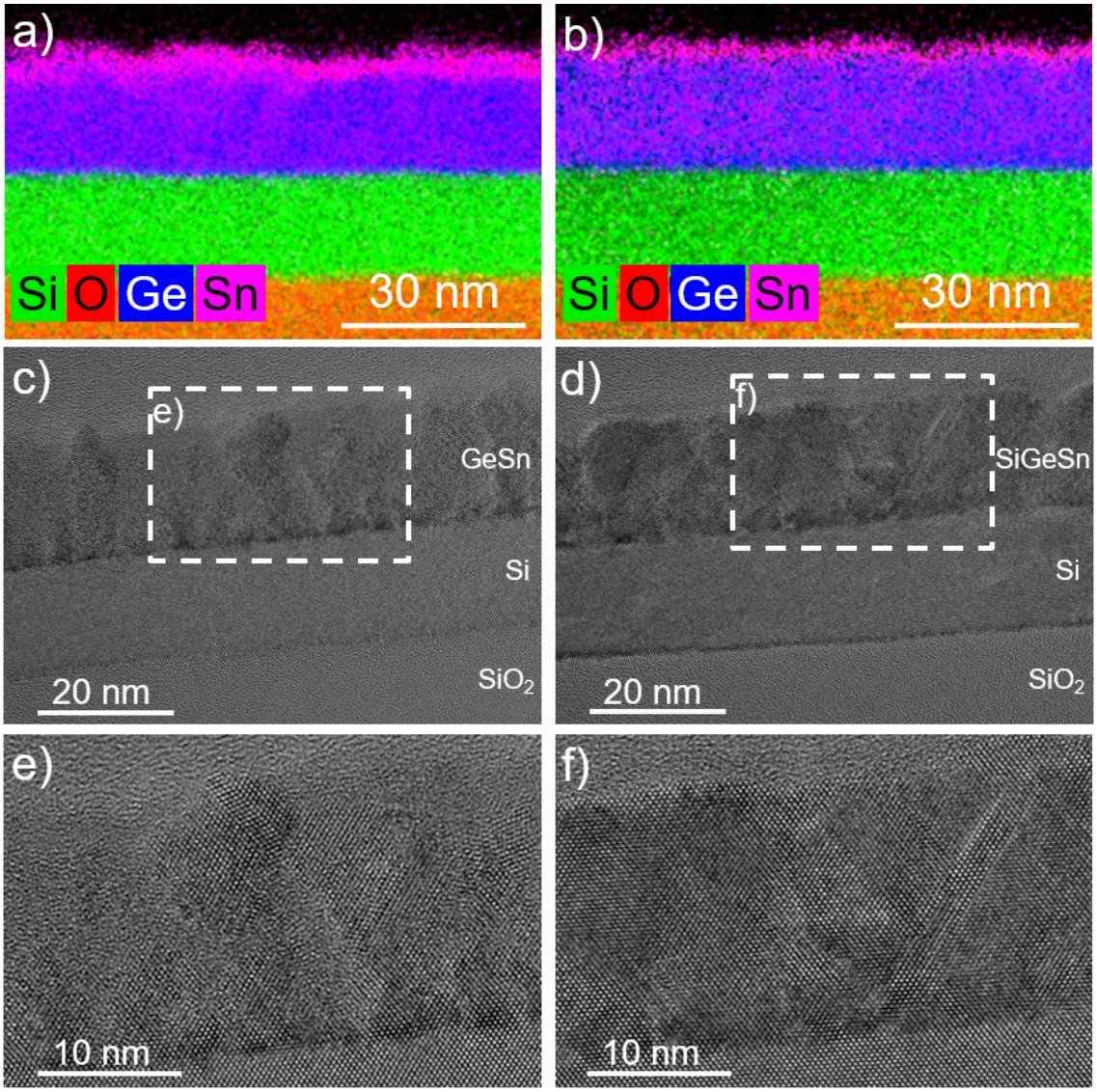


Fig. 5.2 - 1: TEM-based analysis of the as-grown $Ge_{0.94}Sn_{0.06}$ on SOI in a), c), and e) and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI in b), d), and f). The EDXS mappings are superimposed spectra with Si (green), O (red), Ge (blue), and Sn (magenta). The HR-TEM images in c) and d) show from bottom to the top: the BOX SiO_2, Si, and the grown $Ge_{0.94}Sn_{0.06}$ or $Si_{0.14}Ge_{0.80}Sn_{0.06}$ layer. The white dashed rectangles in c) and d) correspond to the enlarged images of the as-grown layer in e) and f).

The $Si_{0.14}Ge_{0.80}Sn_{0.06}$ layer in Fig. 5.2 - 1 d) and f) is single-crystalline but contains many stacking faults. The top surface of $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ has a native oxide $Si_{1-x-y-z}Ge_ySn_xO_z$ layer and appears to be slightly inhomogeneous compared to the $Si_{1-x-y}Ge_ySn_x$ / SOI interface. This suggests more a “layer by layer” plus “three-dimensional island”-based (Stranski-Krastanov) growth with a small island spacing than the targeted “layer by layer” (Frank–van der Merwe) growth mechanism [31]. The Stranski-Krastanov growth is known for heteroepitaxially grown films with a large lattice mismatch and low interface energies. Additionally, the Stranski-Krastanov growth was already observed for the growth of Ge on Si [111]. The observed tight island coverage and a layer thickness above the critical thickness lead to significant strain relaxation by defect formation, which can be seen later in Fig. 5.2 - 1 e) and d). Further details about the Stranski-Krastanov growth can be obtained from refs. [31] and [111]. In the following section, the microstructure will be further analyzed and compared with different annealing conditions.

5.2.3 Microstructure after post-growth thermal treatments

The $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI layers are annealed by PLA with energy densities between 0.12 and 0.25 J cm^{-2} and f-FLA at 48 J cm^{-2} and a pulse length of 3.2 ms. Each annealing step was characterized by RBS-R/C, µ-Raman, and XRD. A selection of annealed states will be discussed in this section.

The RBS-R/C results of the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI before and after annealing are shown in Fig. 5.2 - 2 and Fig. 5.2 - 3. The obtained spectra contain Sn superimposed with Sb (1460 - 1510 keV), Ge (1325 – 1390 keV), and Si (< 1000 keV). The Si contribution of the $Si_{0.14}Ge_{0.80}Sn_{0.06}$, located between 950 – 1000 keV, is partly merged with the pure Si signal of the SOI layer and the high energy tail of the BOX SiO_2.

The RBS-R spectra of the as-grown $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ states were fitted by SIMNRA and confirmed the expected layer composition and thickness. However, changes in thickness and composition influence the intensity significantly. After annealing with the highest selected E_d (0.2 J cm^{-2} for $Ge_{0.94}Sn_{0.06}$ and 0.25 J cm^{-2} for $Si_{0.14}Ge_{0.80}Sn_{0.06}$), which is slightly below the melting regime, the RBS-R spectra remain the same as the as-grown states (see b) and c) in Fig. 5.2 - 2 and Fig. 5.2 - 3). This suggests, at first glance, an absence of diffusion since the shape and energy remain the same. On the other hand, the 20 nm thick layers are close to the depth resolution limit, which can hinder the observation of small changes in the layer composition. Therefore, this first approximation is confirmed by RBS-R measurements under an incident angle of 80°, as shown in **appendix 8.17**.

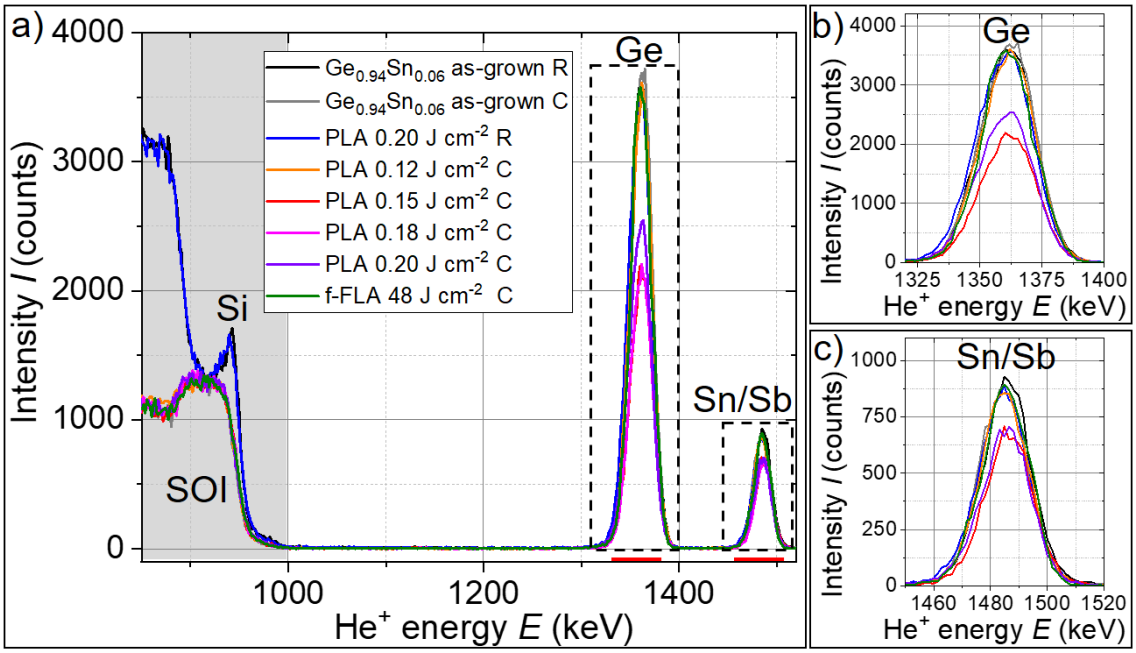


Fig. 5.2 - 2: RBS-R/C results of the $Ge_{1-x}Sn_x$ on SOI material in the as-grown state, after PLA with 0.12, 0.15, 0.18 and 0.2 J cm^{-2}, and f-FLA with 48 J cm^{-2} for 3.2 ms a). The marked windows in a) show the enlargements of the Ge b) and Sn/Sb c) contributions of $Ge_{1-x}Sn_x$. The spectra of Sn and Sb are superimposed.

The RBS-C spectrum of the $Ge_{0.94}Sn_{0.06}$ as-grown state in Fig. 5.2 - 2 is similar to its RBS-R counterpart since the layer contains amorphous inclusions or randomly oriented nanocrystals (see Fig. 5.2 - 1 e)). Analog channeling results were also obtained for the mildly treated PLA 0.12 J cm^{-2} and f-FLA 48 J cm^{-2} for 3.2 ms $Ge_{1-x}Sn_x$ samples. Pronounced channeling can be observed after PLA with 0.15, 0.18, and 0.2 J cm^{-2}.

Table 5.2 - 1: RBS analysis results of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI in the as-grown and PLA-treated states. The minimum channeling yield for Si χ_{Si}, Ge χ_{Ge}, and Sn/Sb $\chi_{Sn/Sb}$, as well as the substitutional fraction of Sn/Sb on Si sites $\xi_{Sn/Sb,Si}$ and on Ge lattice sites $\xi_{Sn/Sb,Ge}$ is calculated by Eq. 3.6 - 1 and Eq. 4.2 - 1. The integration intervals are marked with red horizontal section lines in Fig. 5.2 - 2 a) and Fig. 5.2 - 3 a) and are between 950 and 1000 keV for Si, 1340 and 1390 keV for Ge, and 1465 and 1515 keV for Sn/Sb.

Sample	χ_{Si} (%)	χ_{Ge} (%)	$\chi_{Sn/Sb}$ (%)	$\xi_{Sn/Sb,Si}$ (%)	$\xi_{Sn/Sb,Ge}$ (%)
$Ge_{0.94}Sn_{0.06}$ as-grown	-	100.0	97.8	-	0
$Ge_{1-x}Sn_x$ PLA 0.15 J cm^{-2}	-	60.6	76.5	-	59.6
$Ge_{1-x}Sn_x$ PLA 0.18 J cm^{-2}	-	58.9	72.7	-	66.4
$Ge_{1-x}Sn_x$ PLA 0.20 J cm^{-2}	-	71.2	79.6	-	70.7
$Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown	48.2	58.8	80.5	37.6	47.2
$Si_{1-x-y}Ge_ySn_x$ PLA 0.15 J cm^{-2}	52.2	63.1	84.3	32.9	42.7
$Si_{1-x-y}Ge_ySn_x$ PLA 0.20 J cm^{-2}	53.4	71.6	87.4	27.0	44.2
$Si_{1-x-y}Ge_ySn_x$ PLA 0.25 J cm^{-2}	52.4	79.0	93.7	13.3	30.0

In order to quantify the improvements of the $Ge_{1-x}Sn_x$ crystal structure, the channeling yield and substitutional fractions were calculated and summarized in Table 5.2 - 1. The

general appearance of channeling in the $Ge_{1-x}Sn_x$ microstructure, as well as the SOI beneath, suggests an epitaxial recrystallization or regrowth on the SOI layer. The lowest channeling yields in Table 5.2 - 1 were achieved after PLA with 0.15 and 0.18 J cm^{-2} with $\chi_{Ge} \approx 60\%$ and $\chi_{Sn/Sb} \approx 75\%$. Additionally, the occupation of Sn/Sb on Ge lattice sites with $\xi_{Sn/Sb,Ge} = 59.6\%$ and 66.4% also suggests a reasonable amount of incorporated/activated Sn/Sb atoms on substitutional lattice sites. However, further increasing of PLA to $E_d = 0.2$ J cm^{-2} causes de-channeling in Ge and Sn/Sb.

The occurrence of channeling in Si, Ge, and Sn/Sb in the $Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown state in Fig. 5.2 - 3 confirms the epitaxial single-crystalline growth of $Si_{1-x-y}Ge_ySn_x$ on the SOI wafer. This matches the TEM results in Fig. 5.2 - 1 e). However, the high $\chi_{Sn/Sb} = 80.5\%$ indicates a large portion of Sn or Sb atoms sit at interstitial lattice positions. After f-FLA, the RBS-R/C results of the as-grown state could almost be maintained. On the other hand, PLA with $E_d \geq 0.15$ J cm^{-2} causes a slight de-channeling compared to the $Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown state. In general, the obtained χ_{Si}, χ_{Ge}, and $\chi_{Sn/Sb}$ of the fabricated $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ in Table 5.2 - 1 are relatively high because of the superposition crystal channeling with de-channeling events from surface defects and the formation of a thicker $Ge_{1-x}Sn_x$- or $Si_{1-x-y}Ge_ySn_x$-oxide layer after PLA, which will be discussed later in Fig. 5.2 - 8. Furthermore, the observed misfit dislocations can displace the atomic lattice positions.

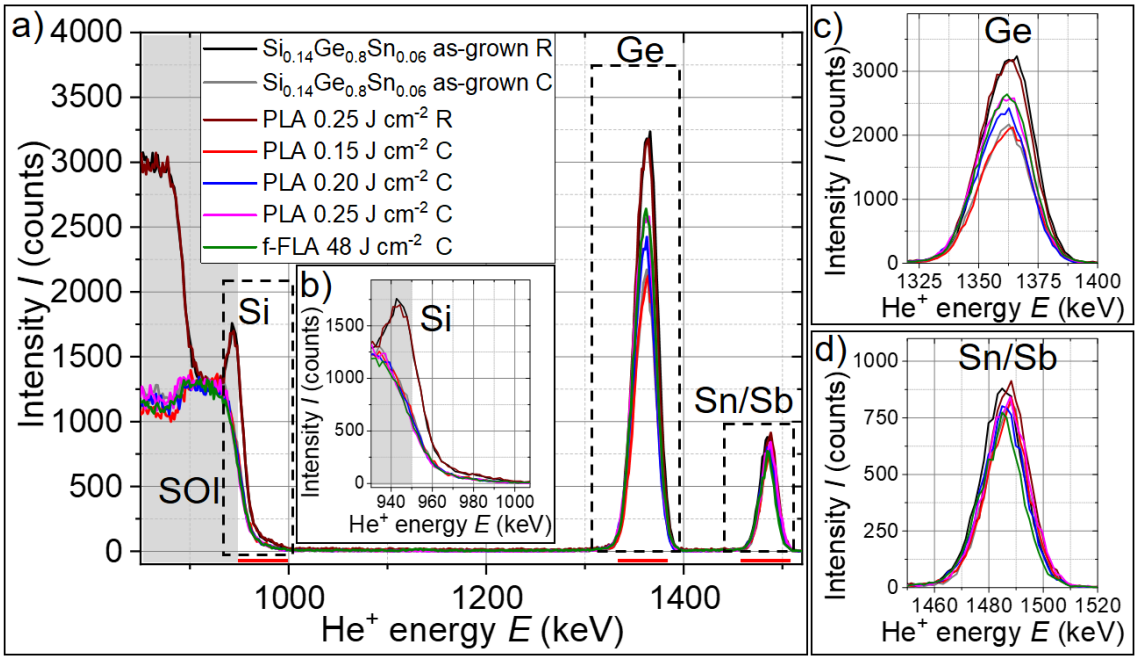


Fig. 5.2 - 3: RBS-R/C results of the $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI material in the as-grown state, after PLA with 0.15, 0.20 and 0.25 J cm^{-2},and f-FLA with 48 J cm^{-2} for 3.2 ms a). Additionally, the marked windows in a) show the enlargements of the Ge contribution in $Si_{0.14}Ge_{0.80}Sn_{0.06}$ b), the superimposed Sn/Sb contribution in c), and the Si contribution in d).

To confirm the RBS findings, HR-XRD *2θ-ω* scans of the (004) reflection were performed. The obtained diffractograms contain the $Ge_{1-x}Sn_x$ (004) in Fig. 5.2 - 4 a) or $Si_{1-x-y}Ge_ySn_x$ (004) in Fig. 5.2 - 4 b) reflections between 63° and 67° and the not shown Si (004) substrate reflection at 69.14°. The substrate lattice was used to align the measurement setup. However, it is not necessarily the case that the (004) plane orientation of the about 750 µm thick SOI carrier substrate coincides with that of the 20 nm SOI above the SiO_2 and the epitaxially grown layers. Therefore, RSM around the (004) Si substrate plane and the (004) plane of the epitaxially grown $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ alloy were performed to exclude the general tilt of the MBE-grown layer compared to the substrate. Details about this RSM (004) validation experiment are shown in **appendix 8.18**. According to the RSM (004) scans, the Si substrate and the $Si_{1-x-y}Ge_ySn_x$ have the same orientation within the measurement accuracy, which coincides with the RBS-C results in the SOI substrate in Fig. 5.2 - 2 a) and Fig. 5.2 - 3 a).

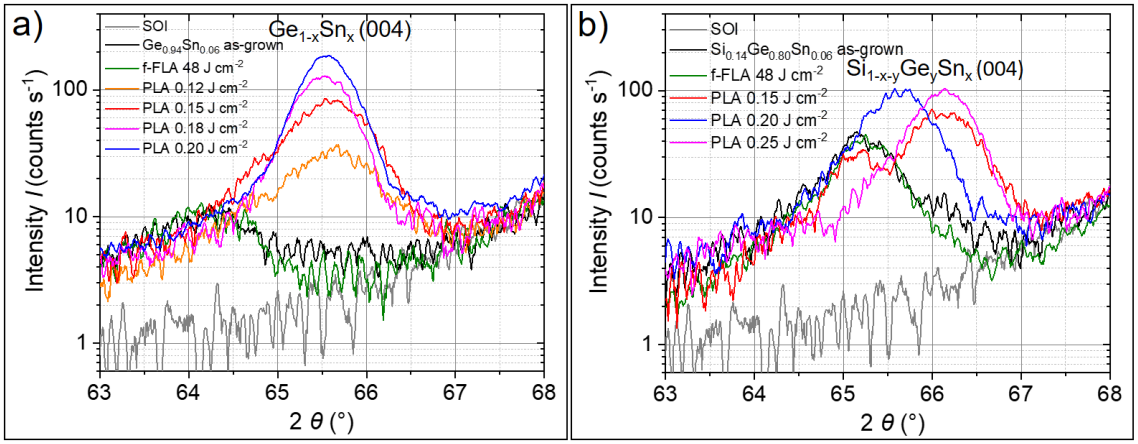


Fig. 5.2 - 4: HR-XRD *2θ – ω* scans around the (004) reflection of the $Ge_{1-x}Sn_x$ on SOI a) and $Si_{1-x-y}Ge_ySn_x$ on SOI b) in the as-grown state, after PLA with varying energy densities and f-FLA with 48 J cm^{-2} for 3.2 ms.

Both as-grown states of the investigated alloys have relatively low reflection intensities in Fig. 5.2 - 4, and f-FLA at 48 J cm^{-2} for 3.2 ms does not significantly change the observed peak shape and position. After PLA, a shift of the $Ge_{1-x}Sn_x$ (004) and $Si_{1-x-y}Ge_ySn_x$ (004) reflection towards larger angles and an increased reflection intensity can be observed. The higher intensities in Fig. 5.2 - 4 a) correlate partially with the RBS-R/C results in Fig. 5.2 - 2 and can be understood as the recrystallization of the lattice compared to the $Ge_{0.94}Sn_{0.06}$ as-grown state. Furthermore, an increased layer quality after PLA can be assumed from the reduced FWHM of the $Ge_{1-x}Sn_x$ (004) reflection. The intensity improvement due to PLA of $Si_{1-x-y}Ge_ySn_x$ (004) in Fig. 5.2 - 4 b) is smaller since the $Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown state is already crystalline. Therefore, the higher intensity is related to a general reduction in defect concentration. On top of the increased (004) reflection intensity, a significant shift towards higher diffraction angles is

observed after PLA in Fig. 5.2 - 4 a) and b). This indicates a reduced out-of-plane lattice parameter, which is caused either by strain relaxation or out-diffusion of larger atoms. Next to the main high-intensity (004) reflections, an additional small peak at around 65° can be observed for PLA with E_d = 0.15 J cm^{-2} in Fig. 5.2 - 4 a) and b). This can be related to a layer separation into a slightly annealed as-grown-like bottom layer and the highly PLA-affected top layer. In the case of $Si_{1-x-y}Ge_ySn_x$ PLA with 0.20 J cm^{-2}, the two reflections merge, and the reflection position shifts only slightly towards lower diffraction angles compared to the main reflection of $Si_{1-x-y}Ge_ySn_x$ PLA with 0.15 and 0.25 J cm^{-2}, which will be addressed further below.

The influence of post-growth thermal treatments on the strain conditions was investigated by (224) RSM and µ-Raman. Fig. 5.2 - 5 and Fig. 5.2 - 6 show (224) RSM in dependence on different annealing conditions. The $Ge_{0.94}Sn_{0.06}$ as-grown state in Fig. 5.2 - 5 a) has a barely noticeable GeSn (224) reflection located close to the strain relaxation line at $q_z/2\pi \approx 7.0$ nm^{-1}. This weak diffraction is related to the mainly amorphous nature of the $Ge_{0.94}Sn_{0.06}$ layer. Furthermore, the location of the reflection on the black dashed strain relaxation line confirms that the crystalline $Ge_{0.94}Sn_{0.06}$ portion is entirely strain-relaxed. After PLA, the peak intensity increases significantly. This correlates with the RBS-C and (004) XRD findings (see Fig. 5.2 - 2 and Fig. 5.2 - 4 a)). According to the $Ge_{1-x}Sn_x$ (224) reflection close to the black strain relaxation line in Fig. 5.2 - 5, the $Ge_{1-x}Sn_x$ samples are fully strain-relaxed after PLA as well. Based on their reflection positions, one can calculate the relaxed lattice parameters $a_0 \approx 0.569$ nm after PLA with Eq. 8.4 - 1 or Eq. 8.4 - 2 and approximate the $Ge_{1-x}Sn_x$ alloy composition to x ≈ 5.97 at.% by using Eq. 2.1 - 1. This composition coincides well with the earlier presented RBS results (see Fig. 5.2 - 2). However, the GeSn (224) reflections are relatively broad, which could be related to a gradient in strain and/or chemical composition. Combining the observed results for $Ge_{1-x}Sn_x$ PLA 0.12 state, like the higher XRD reflection intensities (see Fig. 5.2 - 4 a) and Fig. 5.2 - 5 b)), the absence of RBS channeling (see Fig. 5.2 - 2), the PLA E_d dependent penetration depth (see Fig. 4.1 - 2 b)) and the larger coherence length of the GeSn (224) reflection, suggest the presence of a nanocrystalline $Ge_{1-x}Sn_x$ top layer. On the other hand, the GeSn (224) reflections after PLA 0.15 J cm^{-2} in Fig. 5.2 - 5 c) and 0.18 J cm^{-2} in Fig. 5.2 - 5 d) are narrower in q_x and elongated along q_z compared to the 0.12 J cm^{-2} case. This matches well with the observed channeling in Fig. 5.2 - 2 because of the single-crystalline structure after PLA with E_d = 0.15 and 0.18 J cm^{-2}.

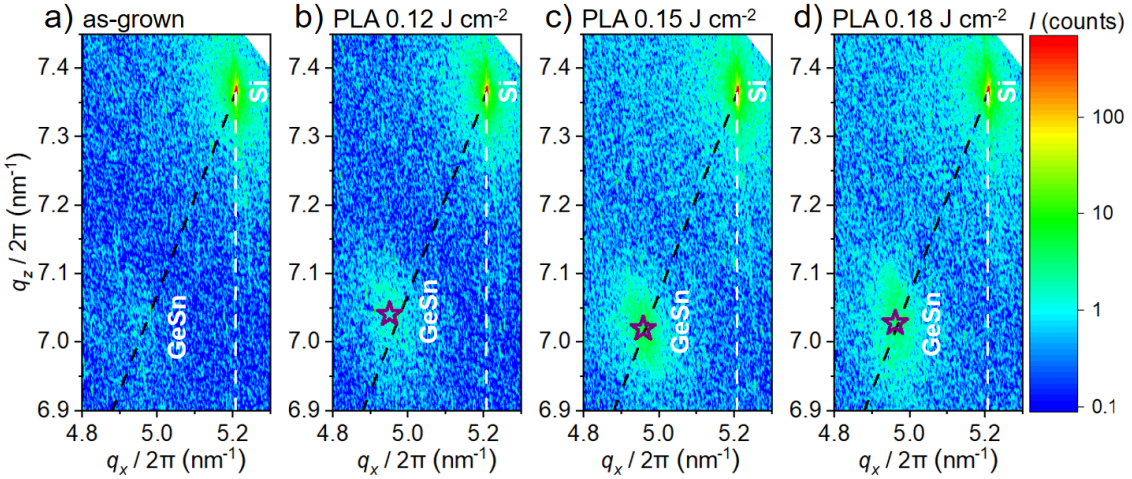


Fig. 5.2 - 5: (224) XRD-RSM of $Ge_{1-x}Sn_x$ on SOI in the as-grown a) and after PLA with E_d = 0.12 J cm^{-2} b), 0.15 J cm^{-2} c), and 0.18 J cm^{-2} d). The black dashed line is the strain relaxation line, and the vertical white dashed line corresponds to the fully pseudomorphically grown state. The fitted maxima of the GeSn (224) reflections are indicated by the purple stars.

The (224) reflection of the $Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown state is located between the pseudomorphic and the strain relaxation line (see Fig. 5.2 - 6 a)). This suggests a strain distribution across the layer thickness from partially compressive strained at the SiGeSn/SOI interface towards almost relaxed close to the surface. After PLA with 0.15 J cm^{-2}, the SiGeSn (224) reflection appears to be elongated in the q_z direction. While the portion with $q_z/2\pi \approx 7.0$ nm^{-1} reminds in location and intensity of the as-grown state, the contribution with the higher intensity at $q_z/2\pi \approx 7.1$ nm^{-1} appears to be slightly tensile strained. This supports the double layer hypothesis concluded from the (004) HR-XRD scan (see Fig. 5.2 - 4 b)). The tensile strain could emerge due to an out-diffusion of larger atoms from the lattice while maintaining the in-plane lattice parameter of the as-grown state or can be introduced by the thermal expansion coefficient difference between the $Si_{1-x-y}Ge_ySn_x$ and the SOI substrate as reported for Ge on Si after cooling from high temperatures (T > 660 °C) to room temperature [31]. In the case of $Si_{1-x-y}Ge_ySn_x$ annealed with E_d = 0.2 J cm^{-2} in Fig. 5.2 - 6, both reflections merged, and the SiGeSn (224) has similar q_x/q_z as in the as-grown state. This can be explained by the increasing penetration depth of the PLA laser with the increasing E_d and suggests a liquid phase epitaxy on the SOI substrate. Increasing the PLA E_d to 0.25 J cm^{-2}, as shown in Fig. 5.2 - 6 d), leads to a shift in the SiGeSn (224) reflection along the strain relaxation line towards the Si (224) substrate reflection. This is a clear evidence of the out-diffusion of a significant amount of larger atoms since the strain conditions remain almost the same. Unfortunately, the remaining strain and the additional third variable (ε_{II}, c_{Si}, and c_{Sn}) do not allow us to estimate the strain or the chemical composition quantitatively by measuring q_x and q_z RSM.

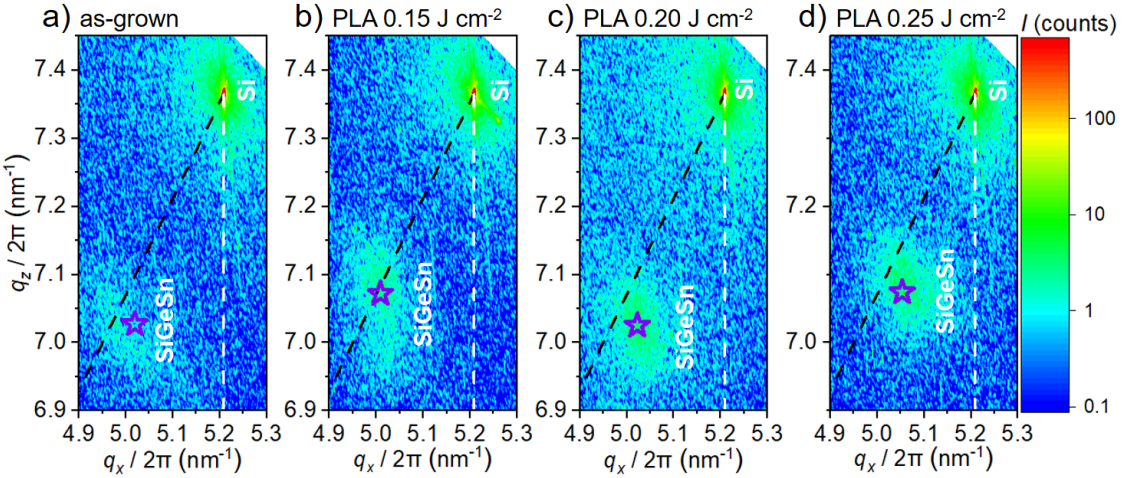


Fig. 5.2 - 6: (224) XRD-RSM of $Si_{1-x-y}Ge_ySn_x$ on SOI in the as-grown state a) and after PLA with E_d = 0.15 b), 0.20 c), and 0.25 J cm^{-2} d). The black dashed line is the strain relaxation line, and the vertical white dashed line corresponds to the fully pseudomorphically grown state. The fitted maximum of the SiGeSn (224) reflection is indicated by the center of the purple star.

The µ-Raman spectra in Fig. 5.2 - 7 a) and b) contain the Ge-Ge (≈300 cm^{-1}), Si-Ge (≈400 cm^{-1}), Si-Si (≈475 cm^{-1}) and Si-Si (520.5 cm^{-1}) phonon modes. The Si-Si mode at 520.5 cm^{-1} belongs mainly to the strain-relaxed Si carrier substrate but also contains contributions of the 20 nm SOI layer. The other modes can be attributed to the thin $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ layer and appear as slightly red-shifted due to the interaction between the Sn concentration and strain, as explained in **section 4.1.3** on $Ge_{1-x}Sn_x$.

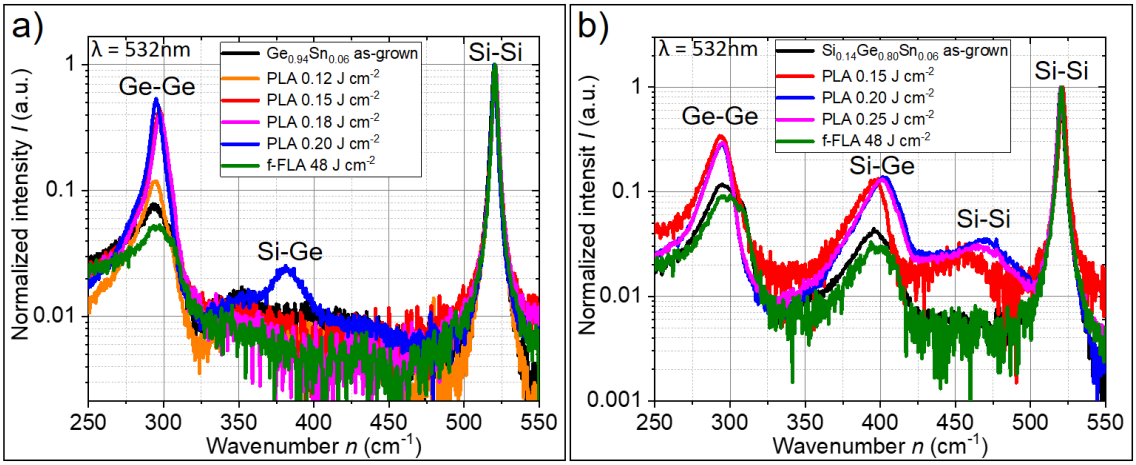


Fig. 5.2 - 7: µ-Raman spectra of the $Ge_{1-x}Sn_x$ on SOI a) and $Si_{1-x-y}Ge_ySn_x$ on SOI b) in the as-grown state, after PLA with energy densities between 0.12 and 0.25 J cm^{-2}, and after f-FLA with 48 J cm^{-2} for 3.2 ms.

After PLA, the observed double peaks of the as-grown states merge in Fig. 5.2 - 7, the FWHM is reduced, and the overall intensity increases. This is related to an improvement of the layer quality or homogeneity, as already concluded from the XRD results. Owing to qualitative similarities in the µ-Raman results to the earlier presented XRD results, a detailed interpretation of the µ-Raman results is given in **appendix 8.19**. Worth mentioning is the emerging Si-Ge mode, which emerged for $Ge_{1-x}Sn_x$ in Fig. 5.2 - 7 a)

after PLA with 0.2 J cm^{-2}. The presence of this peak indicates a local formation of $Si_{1-x-y}Ge_ySn_x$ or $Si_{1-y}Ge_y$ due to diffusion between the former $Ge_{0.94}Sn_{0.06}$ and the top SOI layer. Furthermore, the PLA 0.15 J cm^{-2} treated state of $Si_{1-x-y}Ge_ySn_x$ in Fig. 5.2 - 7 b) showed a significant shift to lower wavenumbers, which confirms in-plane tensile strain from the (224) RSM results in Fig. 5.2 - 6 b).

The PLA annealed $Ge_{1-x}Sn_x$ on SOI and $Si_{1-x-y}Ge_ySn_x$ on SOI samples with the highest PLA energy densities were selected for a cross-sectional TEM analysis, as shown in Fig. 5.2 - 8. Both materials show a highly improved layer quality compared to their as-grown states (see Fig. 5.2 - 1).

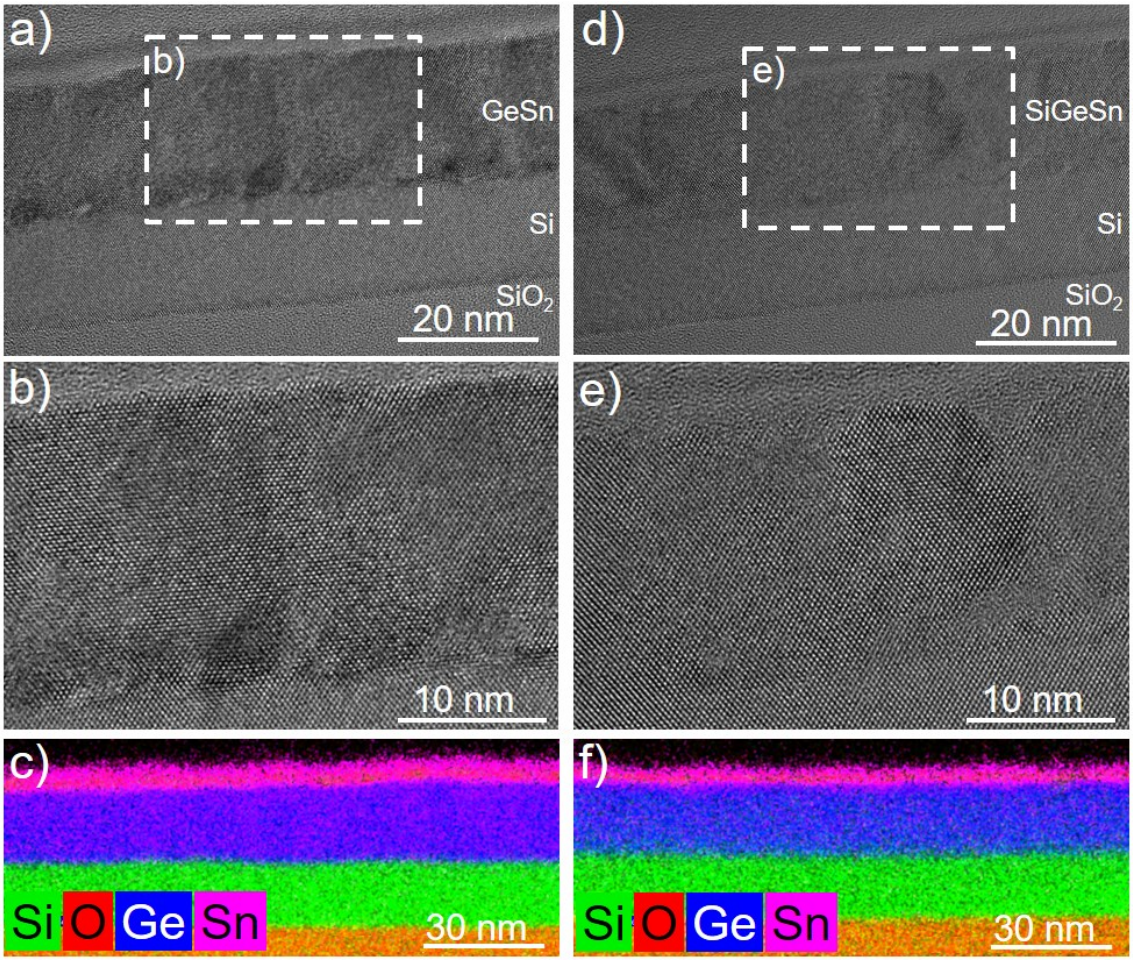


Fig. 5.2 - 8: TEM-based analysis of $Ge_{1-x}Sn_x$ on SOI after PLA at 0.20 J cm^{-2} a) - c) and $Si_{1-x-y}Ge_ySn_x$ on SOI after PLA at 0.25 J cm^{-2} d) - f). The white dashed rectangles in a) and d) correspond to the enlarged images in b) and e). The EDXS-based maps in c) and f) are the superimposed element distributions from Si (green), O (red), Ge (blue), and Sn (magenta).

The $Ge_{1-x}Sn_x$ sample is fully crystalline after PLA at 0.20 J cm^{-2} but has a rough interface to the SOI layer. Additionally, local inhomogeneities in the $Ge_{1-x}Sn_x$ layer thickness and elemental redistributions were observed, which indicate a locally molten/overheated $Ge_{1-x}Sn_x$ layer. The PLA 0.25 J cm^{-2} treated $Si_{1-x-y}Ge_ySn_x$ sample shows local changes in the crystal orientation (see Fig. 5.2 - 8 e)). The EDXS images in Fig. 5.2 - 8 c) and f)

suggest the formation of a thick Sn-rich oxide at the sample surface. Additionally, Fig. 5.2 - 8 f) indicates an out-diffusion of Sn (weaker Sn signal) in the $Si_{1-x-y}Ge_ySn_x$ layer after PLA with E_d = 0.25 J cm^{-2}, which was expected after a detailed analysis of the XRD results. Compared to the molten $Ge_{1-x}Sn_x$ samples discussed in **section 4.1.2**, no formation of Sn clusters and filaments was observed after PLA with low energy densities in the present section.

5.2.4 Dopant concentration and distribution

The dopant concentration and distribution are important parameters for the functionality of the transistors presented in **Chapter 6**. Therefore, the influence of post-growth PLA was investigated by SIMS and Hall-effect measurements.

The SIMS results in Fig. 5.2 - 9 show the elemental depth distribution before and after annealing. Both *in situ* doped as-grown $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI samples have a relatively homogeneous Sb profile despite the surface-related amplitude. Unfortunately, the Sn concentration is slightly reduced after PLA. The $Si_{1-x-y}Ge_ySn_x$ on SOI material in Fig. 5.2 - 9 b) shows, apart from Sn depletion, a redistribution of Ge and Si after PLA. The varying chemical composition across the layer thickness might be the origin of the Sb intensity fluctuations since it influences the sputter yield. After annealing with 0.15 and 0.25 J cm^{-2}, a redistribution of Si towards the SOI interface and a Ge diffusion towards the surface is visible. Furthermore, the PLA 0.15 J cm^{-2} state shows a small kink close to the SOI interface. This kink is related to the almost PLA unaffected $Si_{1-x-y}Ge_ySn_x$ layer, which correlates with the weak intensity signal below the main SiGeSn (224) reflection in Fig. 5.2 - 6 b). The sample annealed with 0.2 J cm^{-2} shows a relatively constant Ge concentration while Sn increases and Si decreases towards the surface.

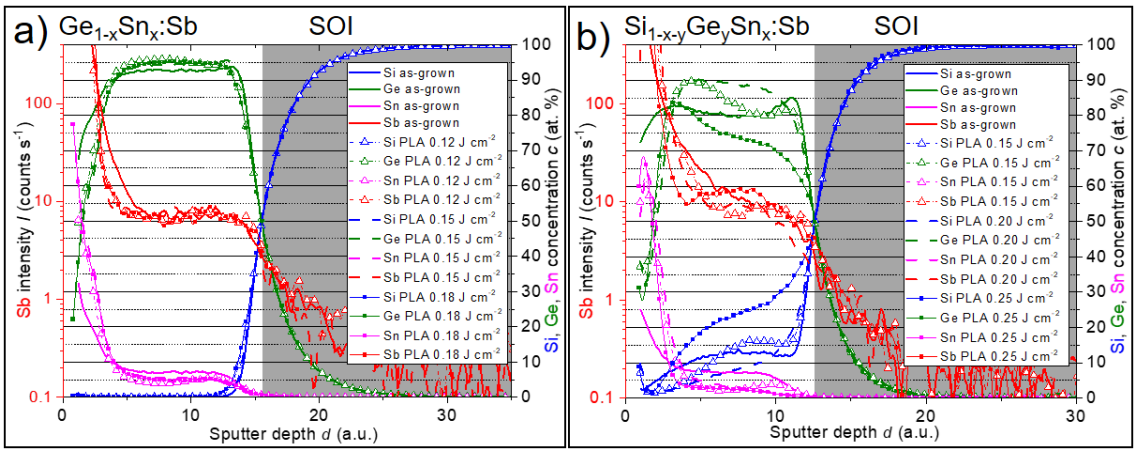


Fig. 5.2 - 9: TOF-SIMS results of the $Ge_{1-x}Sn_x$ on SOI a) and $Si_{1-x-y}Ge_ySn_x$ on SOI b) in the as-grown state and after PLA. The Si layer beneath the alloy is colored in grey.

For Hall-effect measurements in van-der-Pauw configuration, 50 nm thick Ni contacts with a diameter of 1 mm were fabricated on the as-grown and post-growth PLA-treated $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ layers by lithography, 1% HF:DI oxide etching, Ni evaporation, and lift-off. The Hall-effect results of the 20 nm thick *in situ* Sb doped (targeted concentration 5×10^{19} cm^{-3}) $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ layers are shown in Fig. 5.2 - 10 before and after contact formation f-FLA with 48 J cm^{-2} and a flash length of 3.2 ms. The fabricated contact behaves ohmic for small currents ($I_{DS} \approx \pm 1$ mA) before and after f-FLA. The carrier concentration in the Ni as-deposit state is 1.8×10^{19} cm^{-3} for the as-grown $Ge_{0.94}Sn_{0.06}$ and 5.1×10^{17} cm^{-3} for the as-grown $Si_{0.14}Ge_{0.80}Sn_{0.06}$ states. For the PLA-treated samples with $E_d < 0.15$ J cm^{-2}, a similar or slightly reduced carrier concentration compared to the as-grown states was determined as visible on the $Ge_{1-x}Sn_x$ sample treated with $E_d = 0.12$ J cm^{-2} in Fig. 5.2 - 10 a). This indicates the existence of a certain energy barrier, which needs to be overcome to activate additional Sb within the $Ge_{1-x}Sn_x$ lattice. After PLA with $E_d \geq 0.15$ J cm^{-2}, a significant amount of Sb could be activated in both alloys. In the case of $Ge_{1-x}Sn_x$, active carrier concentrations of 3.9×10^{19} cm^{-3} (0.15 J cm^{-2}) and 4.2×10^{19} (0.18 J cm^{-2}) were determined, which are close to the targeted absolute Sb concentration of 5×10^{19} cm^{-3}. In the $Si_{1-x-y}Ge_ySn_x$ case, the n_{e^-} could be significantly increased due to the post-growth PLA compared to the as-grown state to 2.34×10^{19} cm^{-3} for $E_d = 0.15$ J cm^{-2}, 2.28×10^{19} cm^{-3} for $E_d = 0.20$ J cm^{-2} and 1.07×10^{19} cm^{-3} for $E_d = 0.25$ J cm^{-2}, as shown in Fig. 5.2 - 10 b).

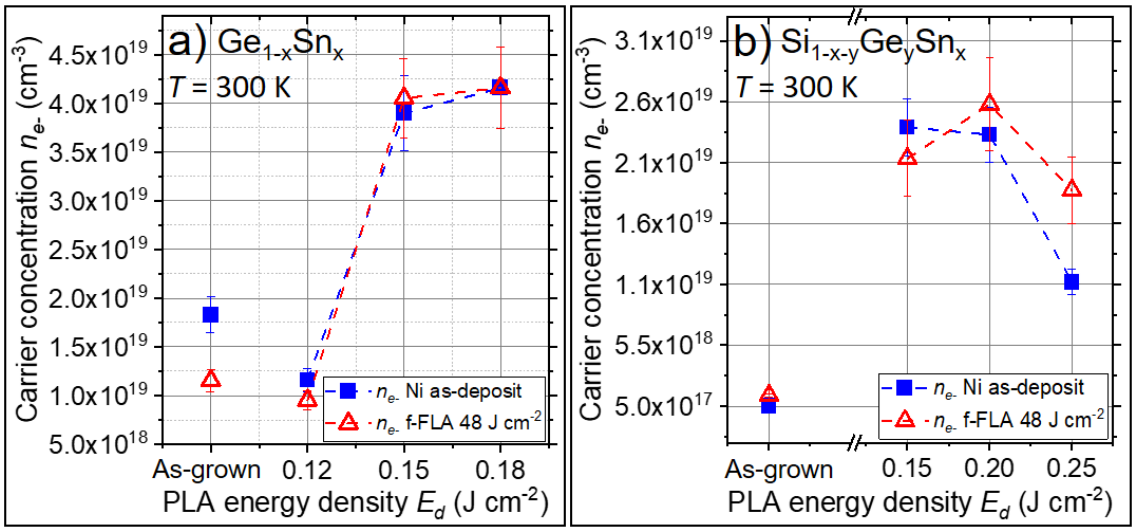


Fig. 5.2 - 10: Active electron concentration n_{e^-} of $Ge_{1-x}Sn_x$ a) and $Si_{1-x-y}Ge_ySn_x$ b) determined by Hall-effect measurements at 300 K of the as-grown state and after post-growth PLA with different energy densities E_d. The measurements were performed after Ni deposition and after contact formation f-FLA with 48 J cm^{-2} for 3.2 ms. Details about the extraction and calculation of the carrier concentration n_{e^-} can be found in **appendix 8.6**.

FLA with 48 J cm^{-2} for 3.2 ms of the Ni contacts enables the formation of a $Ni_{0.55}Ge_{0.42}Sn_{0.03}$ alloy beneath the Ni contact without harming the alloy quality next to

the contact, as confirmed in **section 5.2.3**. Cross-sectional TEM analysis of the contact, presented in Fig. 5.2 - 11, on the example of as-grown $Ge_{0.94}Sn_{0.06}$, confirms the formation of $Ni_{0.55}Ge_{0.42}Sn_{0.03}$ beneath the remaining pure Ni layer. Furthermore, the given chemical concentration determined by EDX in Fig. 5.2 - 11 b) and c) was verified by comparing FFT diffraction images of the fabricated $Ni_{0.55}Ge_{0.42}Sn_{0.03}$ with the Inorganic Crystal Structure Database (ICSD) of the Ni-Ge system. The chemical composition of the observed phase is in between the $Ni_1(GeSn)_1$ and $Ni_5(GeSn)_3$ phases reported by ref. [257] after 30 s RTA at 350 °C and 270 °C, respectively.

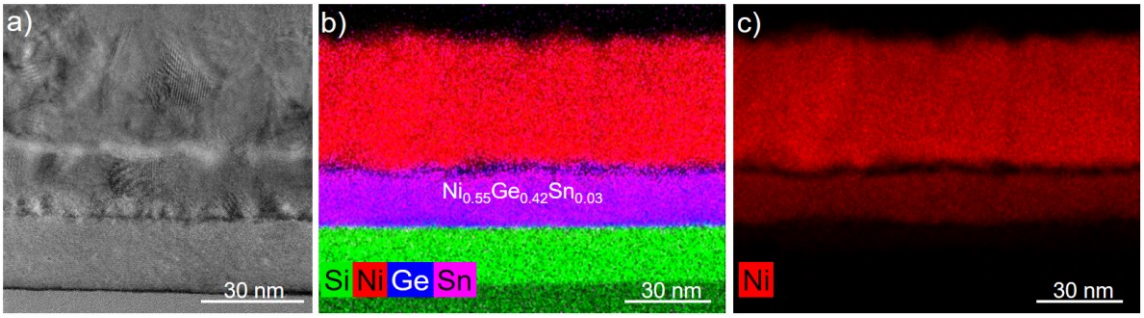


Fig. 5.2 - 11: Cross-sectional TEM-based analysis of the as-grown $Ge_{0.94}Sn_{0.06}$ microstructure after Ni deposition and contact formation f-FLA with 48 J cm^{-2} for 3.2 ms imaged with HR-TEM a) and STEM-EDXS mappings b) and c). The EDXS results show superimposed spectra of Si (green), Ni (red), Ge (blue), and Sn (magenta) in b) and only the Ni signal in c).

The active carrier concentrations before and after f-FLA are in a similar range for both alloys (see Fig. 5.2 - 10), which suggests the application of f-FLA as a suitable method to improve the contact quality by alloy formation in **Chapter 6**.

5.2.5 Conclusion

The fabricated $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ layers on SOI have the desired alloy composition and thickness of 20 nm but are grown in a Stranski-Krastanov growth mechanism. The layer thickness exceeded the critical layer thickness for plastic strain relaxation for both alloys because of the large lattice mismatch of the alloys to the SOI substrate. Therefore, both as-grown alloys are nearly strain-relaxed and contain many defects. Whereas the $Si_{0.14}Ge_{0.80}Sn_{0.06}$ layer is still mainly single-crystalline, the $Ge_{0.94}Sn_{0.06}$ layer contains amorphous inclusions or randomly oriented nanocrystals because of the epitaxial breakdown during the growth. Nevertheless, an active carrier concentration of $n_{e^-} \approx 1.8 \times 10^{19}$ cm^{-3} for $Ge_{0.94}Sn_{0.06}$ and $n_{e^-} \approx 5.1 \times 10^{17}$ cm^{-3} for $Si_{0.14}Ge_{0.80}Sn_{0.06}$ were determined in the as-grown material. After contact formation annealing by FLA with E_d = 48 J cm^{-2} for 3.2 ms, the n_{e^-} is only slightly changed to 1.2×10^{19} cm^{-3} for $Ge_{0.94}Sn_{0.06}$ and 1.4×10^{18} cm^{-3} for $Si_{0.14}Ge_{0.80}Sn_{0.06}$. Furthermore, the used f-FLA parameters with E_d = 48 J cm^{-2} for 3.2 ms do not change any of the investigated crystal properties compared to the as-grown states but enable the formation

of $Ni_{0.55}Ge_{0.42}Sn_{0.03}$ contacts. However, it must be concluded that the defect-rich $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI layers are an enormous challenge for the application as an active component in opto- or nanoelectronic devices. Hence, it is required to i) reduce the lattice parameter mismatch between the alloy and the substrate or ii) perform suitable post-growth thermal treatments.

Post-growth PLA of $Ge_{0.94}Sn_{0.06}$ improved the layer quality significantly. However, Sn diffuses towards the surface and forms a thicker Sn-rich oxide during the PLA process. PLA with 0.12 J cm^{-2} results in a nano-crystalline top layer and does not activate additional Sb dopants. After PLA with 0.15 and 0.18 J cm^{-2}, the $Ge_{1-x}Sn_x$ recrystallizes epitaxially as a single-crystal. In the recrystallized conditions, 60% (0.15 J cm^{-2}) and 66% (0.18 J cm^{-2}) of the Sn atoms were located on substitutional Ge lattice sites. The significantly improved crystal structure coincides with an increased active carrier concentration $n_{e^-} \approx 3.9 \times 10^{19}$ cm^{-3} (0.15 J cm^{-2}) and $n_{e^-} \approx 4.16 \times 10^{19}$ cm^{-3} (0.18 J cm^{-2}), which is about 80% of the targeted Sb concentration. SIMS measurements confirmed an almost unaffected Sb depth distribution in $Ge_{1-x}Sn_x$ after PLA with energy densities up to 0.18 J cm^{-2}. After PLA with 0.2 J cm^{-2}, a locally molten $Ge_{1-x}Sn_x$ layer was observed. Away from the melted regions, a $Ge_{1-x}Sn_x$ layer with a significantly lower defect concentration (similar to the PLA 0.15 and 0.18 J cm^{-2}) occurred.

The post-growth PLA of $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI has an E_d-dependent influence on the microstructure and leads to elemental redistributions. For E_d = 0.15 J cm^{-2}, the layer is divided into a tensile strained (PLA-affected) top layer and a slightly compressive strained as-grown-like bottom layer. For E_d = 0.2 J cm^{-2}, the entire $Si_{1-x-y}Ge_ySn_x$ layer is affected by PLA, which resulted in a slightly compressive strained layer with a homogeneous elemental distribution. After PLA with E_d = 0.25 J cm^{-2}, the $Si_{1-x-y}Ge_ySn_x$ layer is overheated, and significant amounts of Sn and Ge atoms diffuse towards the $Si_{1-x-y}Ge_ySn_x$ layer surface. The carrier concentration of the $Si_{1-x-y}Ge_ySn_x$ alloy could be significantly increased by PLA from $n_{e^-} \approx 5.1 \times 10^{17}$ cm^{-3} in the as-grown state to $n_{e^-} \approx 2.3 \times 10^{19}$ cm^{-3} after PLA with E_d = 0.15 and 0.20 J cm^{-2}. In general, the $Si_{1-x-y}Ge_ySn_x$ quality after PLA seems to be improved for the three discussed PLA annealing states, but this is not reflected in the RBS-R/C results since the thicker oxide caused de-channeling.

6 $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI junctionless transistors

$Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys are promising CMOS-compatible future materials to overcome the physical scaling limits in silicon-based transistor technology. However, $Si_{1-x-y}Ge_ySn_x$ transistors are only theoretically discussed, and not many lateral $Ge_{1-x}Sn_x$ n-type transistors have yet been reported to benchmark the material performance. A relatively new, simple, and promising device concept for this purpose is the junctionless field effect transistor (JLFET), which works as a gated resistor. JLFETs are based on a uniform doping concentration in the source, channel, and drain regions. The absence of junctions simplifies the fabrication process, avoids dopant diffusion-related issues, and allows excellent short-channel characteristics, like drain-induced barrier lowering (DIBL) [7, 58, 258]. Based on the channel geometry and gate configuration, many different depletion-based JLFET concepts were proposed, including thin-film, nanowire, single-gate, double-gate, gate-all-around, and fin-FETs [259]. The operation of a JLFET is based on the depletion and accumulation of conducting charge carriers within the highly doped (~10^{19} cm^{-3}) channel region, which is fundamentally different from the well-known inversion mode MOSFETs. Therefore, in **section 6.1**, the JLFET functionality will be elucidated. Afterward, a fully CMOS-compatible top-down fabrication approach for lateral n-type $Si_{1-x-y}Ge_ySn_x$ on SOI hetero nanowire junctionless transistors (JNT) is presented in **section 6.2**. Furthermore, this section is accompanied by a structural characterization with a top-view SEM and cross-sectional TEM and deals with alloy-specific advantages and challenges in transistor fabrication. In **section 6.3**, the electrical performance of the fabricated transistors is discussed. It highlights the influence of different i) manufacturing steps, ii) post-growth thermal treatment conditions, iii) gate configurations, and iv) post-fabrication FLA.

6.1 Operation principle of n-type JLFETs

The operating principle of n-type JLFET is based on the modulation of carriers by applying an electrical field through the gates. The source, channel, and drain regions are highly n-type doped, which increases the semiconductor conductivity and improves the source/drain contact properties [59, 260].

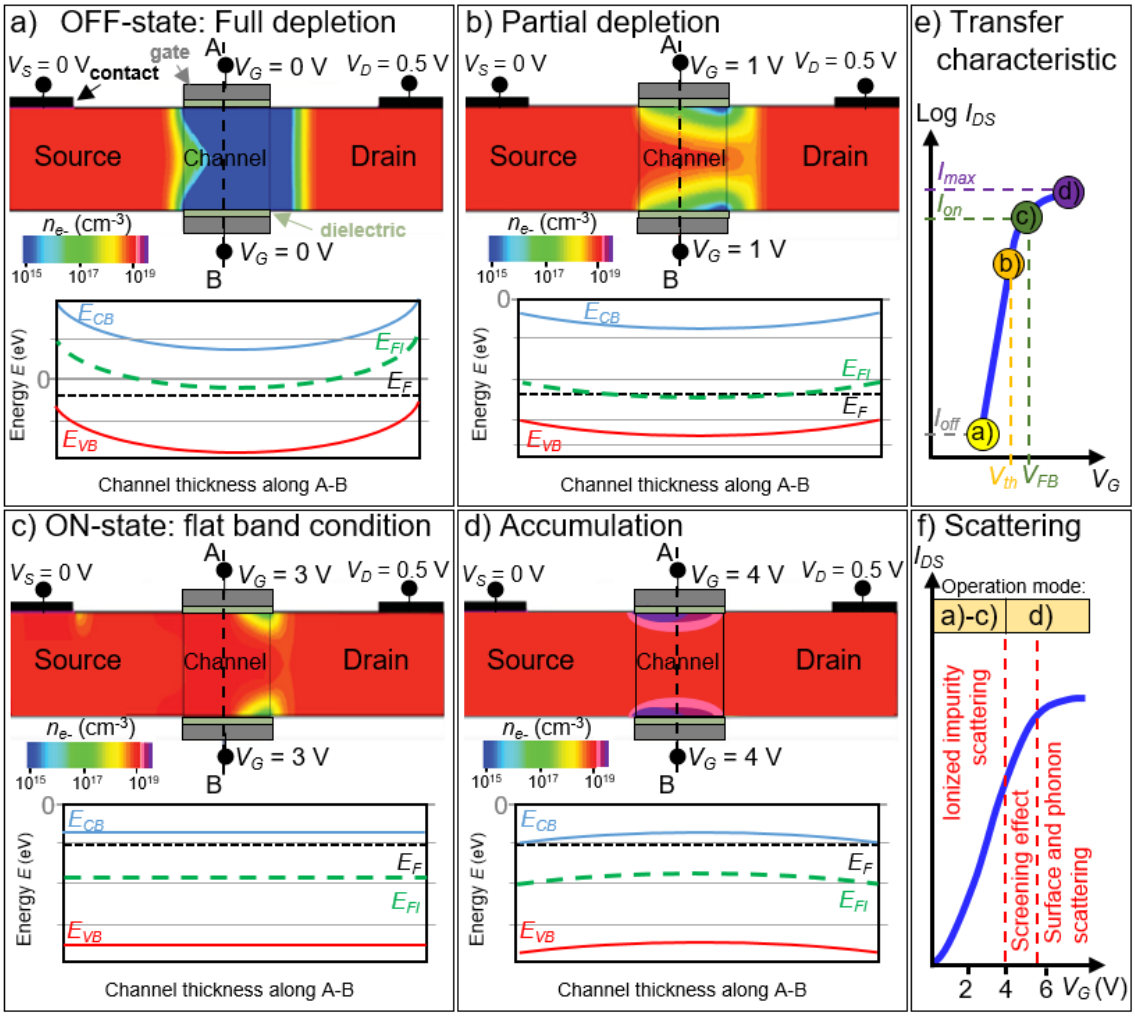


Fig. 6.1 - 1: Schematical electron concentration contour plots and energy band diagrams of selected n-type double-gate JLFET operation modes (a) - d)) in analogy to ref. [59]. The band diagrams are taken across the channel thickness (along the A-B line), and E_{CB} is the conduction band energy (blue solid line), E_F the Fermi energy (dashed black line), E_{FI} the intrinsic Fermi energy (green dashed line), E_{VB} the valence band energy (red solid line). The contour plot shows the electron concentration n_{e^-} for different applied gate voltages V_G in the full depletion a), partial depletion b), flat-band condition c), and accumulation d) mode. Schematical transfer characteristic of an n-type JNT with a logarithmic depiction of the drain-source current I_{DS} in dependence of the gate voltage V_G at a constant source V_S - drain V_D potential e). I_{off} is the off-current, V_{th} the threshold voltage related to the partial depletion mode of b), I_{on} is the on-current at V_{FB} (the flat-band voltage) related to the flat-band condition of c) and I_{max} is the enhanced on-current in the accumulation mode of d). Primary scattering mechanism dependent on the different operation modes for a linearly scaled transfer characteristic f). Due to different scattering mechanisms, the accumulation region is divided into weak (small V_G) and strong accumulation (large V_G).

Adding a thin dielectric and a gate material forms a metal-oxide-semiconductor (MOS) capacitor structure at the channel region [7]. If the work function of the gate is larger than the n-type semiconductor, then the channel beneath the gate can be depleted of e^-, as shown in Fig. 6.1 - 1 a) for the full volume depletion in the JLFET channel. To ensure a full volume depletion, it is required to adapt the channel shape, gate work function, dopant concentration, and dielectric thickness to each other, as explained in **section 6.2** on the example of a JNT in more detail. The functionality of a JNT and a double-gate

JLFET is qualitatively the same. However, the NW channel shape allows controlling the channel by the surrounding gate more effectively due to the additional electrical field from the NW side surfaces. The carrier depletion increases the resistance and turns the n-type normally-OFF JLFET off. Applying a certain positive gate voltage V_G pulls the intrinsic Fermi-energy E_{FI} below the Fermi-energy E_F in the band diagram of Fig. 6.1 - 1 b). This reduces the depletion layer width and uncovers an undepleted conducting cross-section with a high carrier concentration in the channel center, as shown in Fig. 6.1 - 1 b) [261]. The required gate potential to achieve a partial depletion condition is defined as the threshold voltage V_{th} of a JLFET [59]. At this stage, the e^- moves from source to drain within the channel center following a bulk conduction mechanism. Hence, the drain-source current I_{DS} increased significantly in Fig. 6.1 - 1 e). Further increase of V_G uncovers a larger conducting cross-section until the entire channel cross-section is conducting at the so-called flat-band voltage V_{FB}, which is associated with the JLFET on-current I_{on} (see Fig. 6.1 - 1 e) [261]. The related energy band diagram of the flat-band condition in Fig. 6.1 - 1 c) depicts the bands as straight lines, and the E_{FI} is entirely below E_F. Owing to the device architecture, the electrical fields inside the gate electrode are aligned perpendicular to the channel thickness for the double-gate structure or NW diameter for the gate-all-around case. Hence, the minimum field in the flat-band condition is located in the channel/NW center. The absence of the electric field and surface-related defects in the center increases the mobility and favors bulk conduction in the ON-state [7, 261-263]. However, experimental and simulation results revealed similar carrier mobilities of JLFETs in bulk conduction mode compared to MOSFETs in surface conduction mode since the high dopant concentration in the JLFET channel leads to enhanced Coulomb scattering [59, 263, 264]. In general, Coulomb scattering is the most dominant scattering mechanism of the JLFET operation modes discussed so far, as highlighted in Fig. 6.1 - 1 f). Further increasing V_G causes an accumulation of e^- at the dielectric-semiconductor interface, as shown in the contour plot in Fig. 6.1 - 1 d) and bends the energy bands downwards close to the semiconductor surface. In the case of a weak accumulation, a “screening effect” of the ionized dopants reduces impurity scattering, which increases I_{DS} in Fig. 6.1 - 1 f). The screening effect is based on the opposite polarities of the carriers and the ionized dopants [263]. The negative e^- are attracted by the positively ionized dopants and are assembled around the dopants. At the same time, the charge field of the attracted e^- shields the conducting e^- from being scattered by impurities, which increases the channel mobility in the accumulation layer. This effect can be expanded up to a volume accumulation of the channel region. However, for small NW dimensions, scattering at the NW surface and phonon scattering become present in the strong accumulation mode, which limits the I_{DS},

as shown in Fig. 6.1 - 1 f). In dependence on the JLFET design, sophisticated models based on solving Poisson´s equation were developed for different operation regimes and summarized in ref. [265]. The I_{DS} of an n-type JLFET in the ON-state and weak accumulation can be approximated by Eq. 6.1 - 1, where q is the elementary charge, μ_{e^-} the electron mobility, $\mu_{e^-,acc}$ the electron mobility in the accumulation channel, n_{e^-} the electron concentration, $L_{eff,acc}$ the effective length of the accumulation channel, $L_{eff,b}$ the effective length of the neutral bulk channel, S_{max} the cross-section of the channel when the surface is accumulated, W_{eff} the channel perimeter and C_{ox} the gate oxide capacitance normalized by the channel perimeter [265].

$$I_{DS} \approx \frac{q\,\mu_{e^-}\,n_{e^-}}{L_{eff,b}} S_{max} C_{ox} + \frac{\mu_{e^-,acc} C_{ox} W_{eff}}{L_{eff,acc}} \left(V_{DS}(V_G - V_{FB})\right) - \frac{1}{2} V_{DS}^2 \qquad \text{Eq. 6.1 - 1}$$

In order to get high on-currents, it is desired to have a highly doped channel with high mobilities, a large depletable channel cross-section, a thin oxide with a high capacitance, small effective accumulation length, large gate voltages before saturation, a small flat-band-voltage and large supply voltages. This can be achieved by modifying i) the channel material properties in terms of n_{e^-} , μ_{e^-} *and* $\mu_{e^-,acc}$ and ii) adjusting the device architecture, like the vertical NW thickness d_{NW}, the NW width W_{NW}, the width of the top-gate W_{TG} on the NW channel, the gate work function and gate shape, and the dielectric thickness and its dielectric constant. Furthermore, low sub-threshold swings *SS* are desired, which highly depends on the JLFET architecture [259]. Normally, omega-gated, trigated, or gate-all-around JLFETs have *SS* in the range of 60 – 100 mV dec.$^{-1}$ [259, 265].

The explained operation of JNTs is different from that of conventional MOSFETs, which results in slightly different transistor parameter extraction procedures [266-268]. Therefore, the JNT device parameter extraction and its definitions are explained in detail in **appendix 8.21** - **8.24**.

6.2 Fabrication of n-type JNTs

The general process flow for the fabrication of lateral n-type $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI JNTs using a top-down gate-last approach is depicted in Fig. 6.2 - 1. A 20 nm thick $Ge_{0.94}Sn_{0.06}$ or $Si_{0.14}Ge_{0.80}Sn_{0.06}$ layer *in situ* doped with Sb was epitaxially grown by MBE on SOI substrates with a 20 nm top Si layer in fabrication step (1), as explained in detail in **section 5.2.1**. SOI wafers are beneficial in reducing the leakage current, which decreases the I_{off} of electrical devices [3]. Additionally, the reduced parasitic drain capacitance increases the switching speed and reduces the power consumption of the fabricated devices [3]. Furthermore, the BOX beneath the top Si layer enables the control of the JNTs by using the SOI substrate as a back-gate [269].

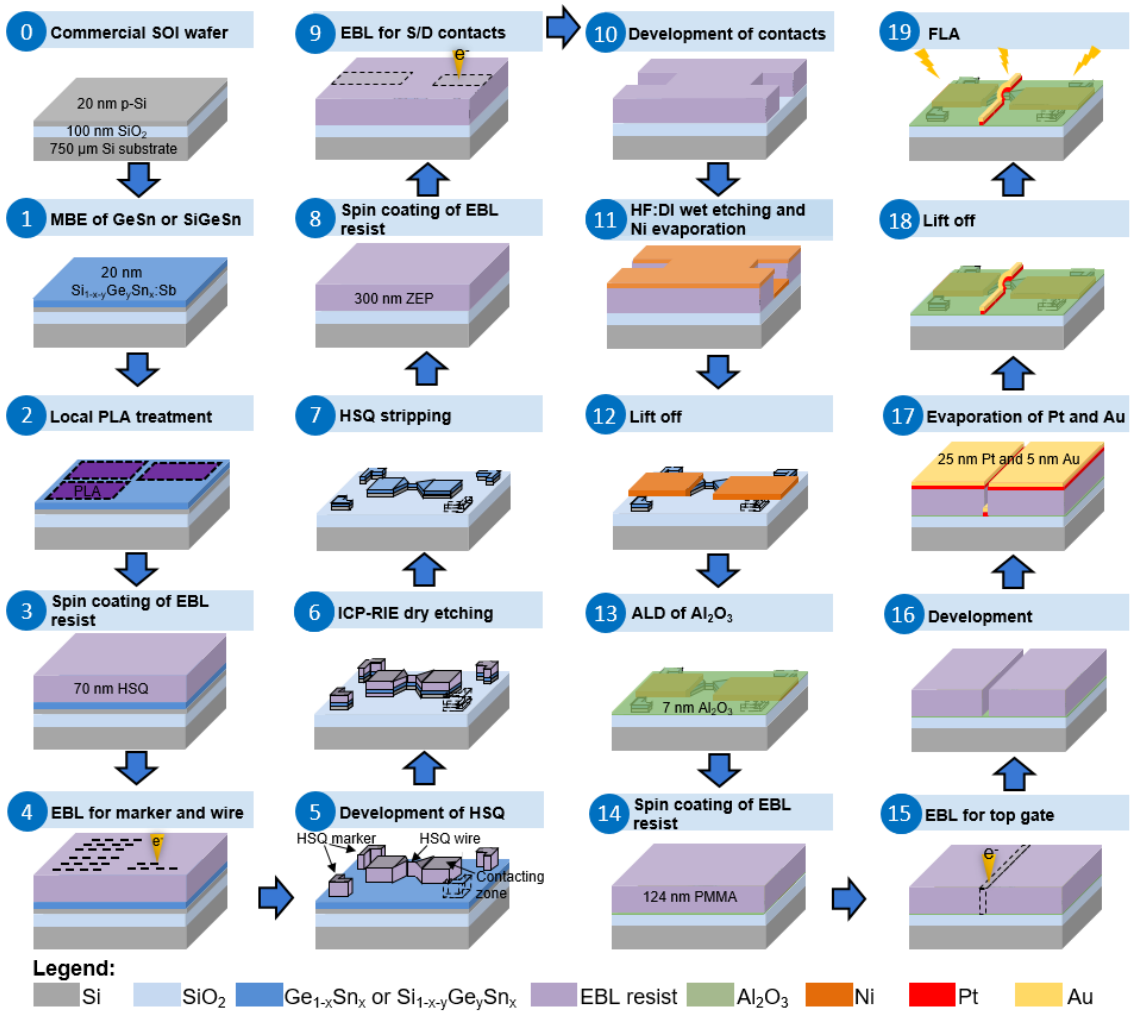


Fig. 6.2 - 1: Schematic presentation of the implemented top-down fabrication approach of lateral n-type $Ge_{1-x}Sn_x$ or $Si_{1-y-x}Ge_ySn_x$ on SOI JNTs. Detailed process parameters are summarized in **appendix 8.20.**

The quality of the $Ge_{0.94}Sn_{0.06}$ or $Si_{0.14}Ge_{0.80}Sn_{0.06}$ layers grown directly on Si suffers from lattice mismatch introduced defects, as explained in **section 5.2.2**. Therefore, the 10 x 10 mm² samples were locally PLA-treated in step (2) to improve the overall layer quality and further activate Sb. The high doping level provides high I_{on} (see Eq. 6.1 - 1), helps to reduce the source/drain contact resistance [268], and reduces the statistical fluctuation for dopants, which becomes important for tiny device dimensions [7]. On the other hand, the high doping level provides undesired Coulomb scattering, degrading the carrier mobility. Therefore, an Sb concentration of 5×10^{19} cm^{-3} was selected for the JNTs as a compromise. This dopant concentration is close to the commonly used literature values of 1×10^{19} cm^{-3} to 5×10^{19} cm^{-3} [59, 259]. The application of different PLA E_d on the same sample, as described in **section 5.2.3**, allows us to judge the influence of the post-growth thermal treatment on the JNT performance. In particular, JNTs were made of the as-grown $Ge_{0.94}Sn_{0.06}$ layer and the $Ge_{1-x}Sn_x$ layers after PLA at 0.12 and 0.15 J cm^{-2}, while $Si_{1-x-y}Ge_ySn_x$ JNTs were fabricated in the $Si_{0.14}Ge_{0.80}Sn_{0.06}$ in as-grown

state and after PLA with 0.15, 0.20 and 0.25 J cm^{-2}. A structural comparison of the different annealing states is presented in **section 5.2**. Afterward, the alignment markers, as well as [110] oriented single NWs with a length L_{NW} of 3 µm, 1 µm and 0.5 µm and a width W_{NW} of 90 nm and 78 nm for $Ge_{1-x}Sn_x$ and about 200 nm for $Si_{1-x-y}Ge_ySn_x$, were fabricated by a GeO_x etching, spin coating of the negative resist hydrogen silsesquioxane (HSQ) in step (3), electron beam lithography (EBL) in step (4), 25% tetramethyl-ammonium hydroxide (TMAH) and MF-319 based development in step (5), and inductively-coupled plasma reactive ion etching (ICP-RIE) in step (6) with chlorine-based chemistry. Four 4 x 4 µm "L"-shaped alignment markers are located around the NW within a 100 x 100 µm² write field. These markers are used for the EBL alignment of the source/drain contacts in step (9) and for the top-gate pattering in step (15). In general, L_{NW} should be short to reduce the overall source/drain resistance. On the other hand, a reduced L_{NW} requires good alignment in step (15). Small W_{NW} are required for a full depletion of the channel by the top-gate (TG) and overall better controllability of the current flow through the channel. In general, decreasing NW dimensions increases the demand for robust fabrication parameters, which is always challenging for novel materials. The NW ends are connected with proximity-corrected 10 x 10 µm² large contacting zones, as shown in Fig. 6.2 - 2 a). These zones are designed to lower the contact resistance between the group IV alloy and the source/drain Ni contacts in step (12). GeO_x etching in an acetic acid:DI solution shortly before the HSQ spin coating improves the HSQ adhesion and removes germanium oxides (GeO_x). Especially, the presence of the water-soluble GeO_2 beneath the exposed HSQ structures is a known origin for delaminations during water-based HSQ development [270]. EBL and the TMAH-based development are standard processes well described in ref. [271, 272]. Chlorine-based ICP-RIE was used to transfer the HSQ patterned structures into the material since fluorine-based ICP-RIE is known to form non-volatile $F_{1-x-y}Sn_xO_y$ [273], which effectively passivates $Ge_{1-x}Sn_x$ (x > 6at.%) on Ge. For the fluorine-based etching with sulfur hexafluoride (SF_6) and octaflurocyclobutane (C_4F_8), an etch selectivity above 433 [274] was reported for $Ge_{1-x}Sn_x$ (x > 8-15 at.%). The much lower etch rate of $Ge_{1-x}Sn_x$ compared to Ge can be used for etch-stop layers [132], underetching of horizontal layer/structures such as NW [273], or optical active µ-disks [273]. This interesting behavior could pave the way for implementing gate-all-around devices or even vertically stacked gate-all-around NW arrays for future high-performance device concepts [8].

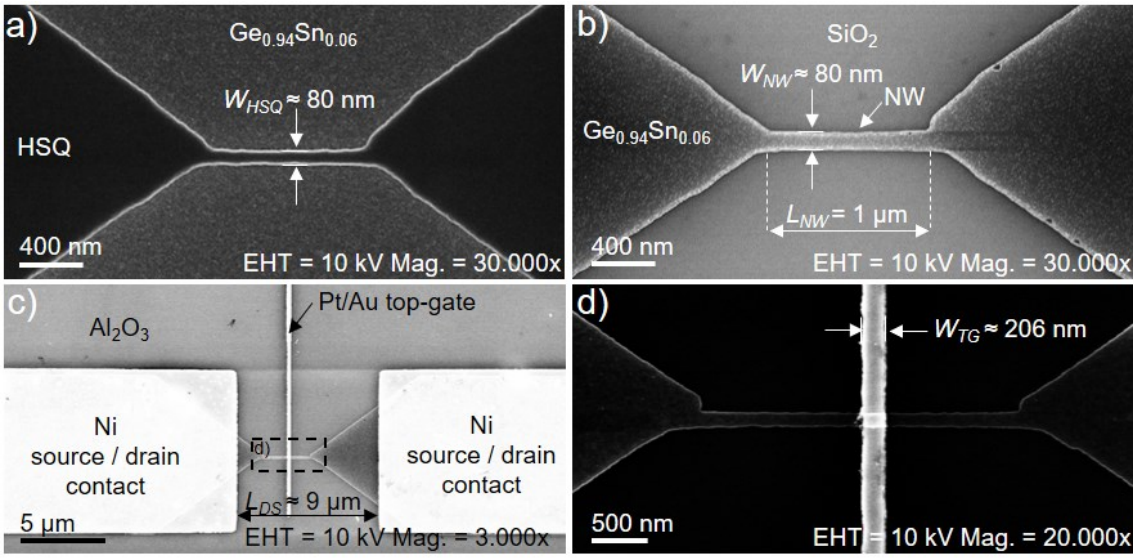


Fig. 6.2 - 2: Top-view InLense SEM images after HSQ development in step (5) a), after HSQ removal in step (7) b), and top-gate fabrication in step (18) c) and d). Representative fabricated NW between contacting zones with a $L_{NW} \approx 1$ µm long and $W_{NW} \approx 80$ nm broad NW in a) and b). Overview of a fabricated JNT with an Al_2O_3 passivated $L_{NW} \approx 3$ µm long, and $W_{NW} \approx 90$ nm wide NW in-between source/drain Ni contacts, and a $W_{TG} \approx 206$ nm wide Pt/Au top-gate c). Enlarged window in c) of the NW d).

After RIE, the HSQ resist was removed by wet etching with 1% HF:DI in step (7), and the NW dimensions were measured by top-view SEM, as shown in Fig. 6.2 - 2 b). The etched contours of the $Ge_{1-x}Sn_x$/Si or $Si_{1-x-y}Ge_ySn_x$/Si hetero-NW in the center of Fig. 6.2 - 2 b) could be successfully transferred from the patterned HSQ mask in Fig. 6.2 - 2 a). The source/drain contacts were fabricated by spin coating of the highly sensitive positive EBL resist ZEP520A [275, 276] in step (8), EBL exposure in step (9), opening of the exposed windows by development of the resist in step (10), 1% HF:DI native oxide etching, thermal evaporation of 50 nm thick Ni contacts in step (11), and lift-off in step (12). Ni that forms Ni-$Ge_{1-x}Sn_x$ alloys after annealing is considered to be the most suitable material to achieve an ohmic contact with low contact resistance for $Ge_{1-x}Sn_x$ alloys [257, 277-279]. Since the Si concentration in $Si_{1-x-y}Ge_ySn_x$ is only about 14 at.%, Ni is also used for the contact formation of the ternary alloy [257]. Furthermore, the source/drain Ni contacts have a distance of $L_{DS} \approx 9$ µm and cover the $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ NW contact zones, as visible in Fig. 6.2 - 2 c). The high doping level of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ helps to achieve an ohmic contact, and the contact zones lower the contact resistance compared to tiny contact areas of vertical device concepts [49, 59]. On the other hand, fabricating ohmic contacts to n-type Ge-based semiconductors is much more challenging than p-type ones because of a strong Fermi level pinning in the n-type case [280]. In the ideal case, the annealing of the electrical contact should be performed subsequently to the Ni deposition. However, this additional annealing would interfere with the influence of the post-growth PLA and is therefore

shifted towards the end of the JNT process flow in step (19). Hence, the JNT fabrication is continued with the fabrication of the dielectric by etching of the low-quality native $GeSnO_x$ or $SiGeSnO_x$ on the NW structures with the acetic acid:DI etching approach [224] and deposition of 7 nm Al_2O_3 (equivalent oxide thickness EOT ≈ 3 nm) by atomic layer deposition (ALD) to passivate the NW surface in step (13). Furthermore, the currently most promising high-k deposition approach [49, 71, 145] by wet chemically removing the native $SiGeSnO_x$ or $GeSnO_x$ oxide, deposition of about 1 nm Al_2O_3, oxygen plasma treatment, and deposition of hafnium dioxide (HfO_2) was not yet available for application at our laboratory. The involved oxygen plasma treatment step forms in the case of GeSn, a thin high-quality $GeSnO_x$ interfacial passivation layer at the high-k/GeSn interface. The $GeSnO_x$ interlayer formation enables interface defect state densities as low as 1×10^{11} cm^{-2} [145]. Fortunately, the interface quality is of minor importance for JNT functionality since the main conduction path is close to the NW center, as explained in **section 6.1**. On the other hand, it is better to have a low surface defect density for the JNT in accumulation mode. The gate dielectric thickness for the JNT design is more important since it should be thick enough to avoid gate leakage and electrical breakdown while sweeping the TG potential in the JNT operation. On the other hand, the oxide should be thin enough to enable the depletion of the NW channel [267]. Therefore, 7 nm thick Al_2O_3 was selected as a compromise. Afterward, the TG is fabricated by PMMA spin coating in step (14), opening TG windows with EBL exposure in step (15), and structure development in DI:IPA solution in step (16), followed by a deposition of 25 nm Pt and 5 nm Au in step (17). In order to investigate the influence of the TG width on the JNT performance, three different single-pixel line doses were selected for the PMMA EBL exposure. Pt is selected as the TG metal because of the inherent low resistivity and high work function of 5.6 – 6.4 eV [281], which allow an effective depletion of e^- in the n-type NW channel. Au is used as a ductile metal to ensure an entire electrical contact around the NW. Afterward, the PMMA-protected areas were uncovered by a lift-off process in step (18), and the W_{TG} was measured by top-view SEM, as exemplarily shown in Fig. 6.2 - 2 d).

Cross-sectional TEM-based analysis of fabricated JNTs was performed after TG fabrication in step (18). The lamella sampling was performed with a focused ion beam lift-out approach along the Pt TG, as shown in Fig. 6.2 - 3 a) and b), and at the Ni source/drain contact in Fig. 6.2 - 3 c). Generally, the image in Fig. 6.2 - 3 a) confirms the layer stack. However, the $Ge_{1-x}Sn_x$ layer of the GeSn/Si hetero NW structure is only about 3 nm thick. This $Ge_{1-x}Sn_x$ thickness is much thinner than the expected 20 nm from the TEM investigations in Fig. 5.2 - 8 and reduces the conducting cross-section significantly.

Within the fabrication process, three potential processes could reduce the $Ge_{1-x}Sn_x$ layer thickness: i) water-soluble Ge-based oxides could be dissolved during cleaning steps in acetone and IPA, ii) the GeO_x etching performed before the steps (3) and (13) could etch the Sn containing alloy, and iii) the removal of HSQ and partial $Ge_{1-x}Sn_x$ etching during RIE in step (6). However, variable angle ellipsometry or SEM on reference samples could exclude these potential explanations. On the other hand, the removal of the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ top surface layer prevents the potential negative influence of the Sn-rich oxide observed after PLA (see Fig. 5.2 - 8 c) and Fig. 5.2 - 8 f)). Additionally, the thinner vertical NW thickness can help to deplete the n-type $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ more efficiently.

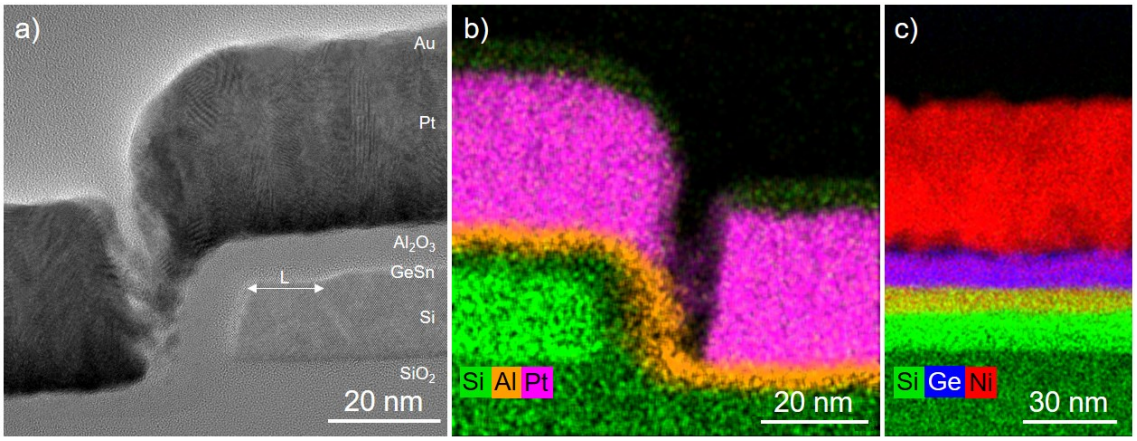


Fig. 6.2 - 3: Cross-sectional TEM-based analysis after TG fabrication in step (18) of the $Ge_{1-x}Sn_x$ JNT along the Pt TG a) and b) and at the Ni source/drain contact c). a) and b) are taken close to the NW edge and c) at the GeSn-Ni contact zone. The EDXS mappings in b) and c) show superimposed spectra with Si (green), Ge (blue), Pt (magenta), Al (orange), and Ni (red). The weak detection of Si on top of the Pt layer in b) is related to an inconvenient EDXS spectra overlap of the Au M_{4N3}-Line at 1746 eV and Si $K_{\alpha1}$–line at 1740 eV.

Furthermore, Fig. 6.2 - 3 a) shows a lateral etching *L* of about 18 nm for $Ge_{1-x}Sn_x$. For the $Si_{1-x-y}Ge_ySn_x$ NW, a lateral etching of 21 nm was observed. This etching is related to an isotropic underetching of the HSQ mask by chlorine-based RIE in step (6). The 7 nm thick Al_2O_3 layer covers the whole NW surface is homogeneously (see Fig. 6.2 - 3 a) and b)). The Pt/Au TG appears homogeneous on top of the NW but shows irregularities at the NW edge. Increasing the Pt/Au layer thickness can improve this TG contact connection. Nevertheless, the presence of a connection between the Pt/Au main contact pad to the Pt/Au TG across the $W_{TG} \approx 200$ nm wide structure is confirmed by electrical measurements (see **section 6.3**). Furthermore, the distance *L* between the TG edge irregularity and the underetched active NW is large enough to neglect this influence in the electrical field. The Ni/GeSn contact in Fig. 6.2 - 3 c) appears relatively smooth and shows an about 10 nm thick $Ge_{1-x-y}Sn_xNi_y$ layer. However, Ni is already diffused locally into the $Ge_{1-x}Sn_x$ layer and can be detected at the top of the SOI layer, which was not

expected before the post-fabrication FLA. Qualitatively similar TEM results are also observed for the $Si_{1-x-y}Ge_ySn_x$ JNTs. Finally, f-FLA with E_d = 48 J cm^{-2} for 3.2 ms was performed in step (19) in order to i) enhance the Ni-$Ge_{1-x}Sn_x$ or Ni-$Si_{1-x-y}Ge_ySn_x$ alloy formation at the source/drain contacts and ii) improve the interfaces between $Si_{1-x-y}Ge_ySn_x$/Si, the Al_2O_3/NW and Al_2O_3/Pt TG. Thermal treatments of the Sn-containing alloys are always critical because of the thermodynamic instability of these alloys. Currently, the main fabrication approach used for ohmic contacts to $Ge_{1-x}Sn_x$ layers is the deposition of Ni and performing relatively long RTA thermal treatments at temperatures below the growth temperature [27, 257]. However, the diffusion at such conditions is slow, and the NiGeSn/GeSn interface appears rough [257]. Furthermore, experiments with PLA ($T>T_m$) generated undesired and deep Ni and Sn-rich filaments by a pipe diffusion mechanism and a rough NiGeSn-GeSn interface [126, 179]. Therefore, solid phase f-FLA was selected as the method of choice.

6.3 Electrical characterization

The fabricated $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI JNTs were electrically investigated to evaluate the performance of the novel alloys. All electrical measurements of the transistors were performed on a probe system PA200 from Süss Microtec equipped with a semiconductor characterization system SCS-4200 and a switching matrix with Model 7174A 8 x 12 low current matrix card from Keithley Instruments. The measurements were carried out in a grey room environment. The temperature was kept at 25 °C with a temperature control ATT low temp system C200-60 from Advanced Temperature Test Systems GmbH (ATT). The presented transfer characteristics are performed with a double hysteresis sweep of the gate, and the presented curves belong to the second sweep. The supply voltage V_{DS} was limited to 0.5 V since the alloys are metastable, and the SOI substrate can suffer from localized self-heating effects during device operation because of the limited heat dissipation through the underlying insulator [3, 282].

6.3.1 JNT performance evolution during processing

The performance of the as-grown $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ JNTs are investigated by back-gated transfer characteristic measurements in dependence of manufacturing steps discussed in **section 6.2**. The I_{DS}-V_{BG} results are presented in Fig. 6.3 - 1 after deposition of the source/drain Ni contacts in step (12), NW passivation with Al_2O_3 in step (13), top-gate fabrication in step (18), and post-fabrication FLA in step (19). The back-gated transfer characteristic of the fabricated JNTs consists of an n-branch towards positive V_{BG} and a p-branch towards negative V_{BG}. Between both branches, the devices turn off at the I_{DS} minimum (I_{off}). The n-branch originates from the

highly n-type doped $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ thin films. The p-branch might be related to the contribution of the wider and thicker p-Si layer. This goes in line with the presence of both branches in transfer characteristics of p/n-stacked poly-Si JLFETs reported in ref. [283]. Even though both branches can be assigned to a layer of the n-type $Ge_{0.94}Sn_{0.06}$ or $Si_{0.14}Ge_{0.80}Sn_{0.06}$ / Si hetero NW material, the presence of a vertical p-n junction is not entirely covered by the conventional JNT device concept. Hence, the fabricated devices are a new type of transistor manufactured with a JNT approach. On the other hand, the absence of lateral junctions within the n- and p-type layers fulfills the JNT requirements. Therefore, the term JNT will be retained for our device, but it should be kept in mind that the presence of the p-Si layer beneath the n-type layer can deplete the n-type layer slightly and influence the back-gated characteristics.

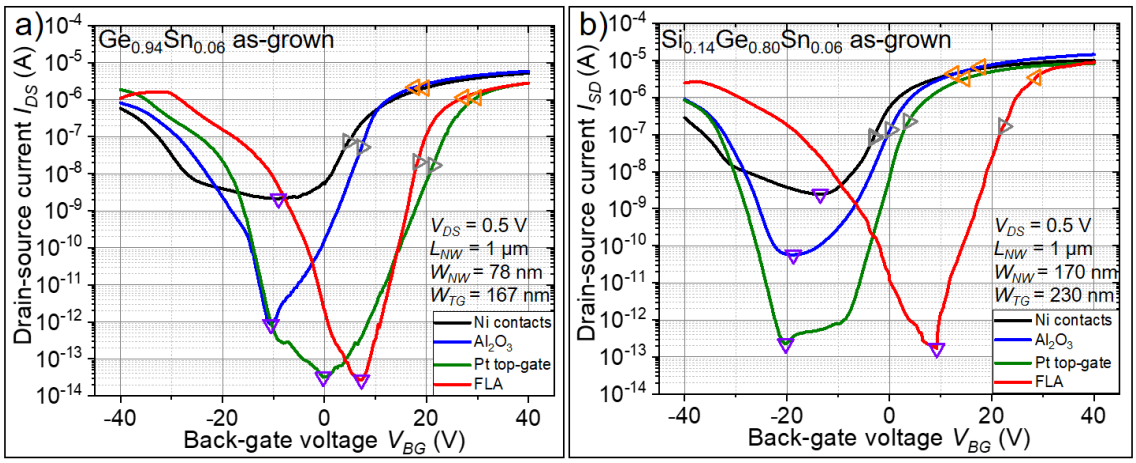


Fig. 6.3 - 1: Forward sweeps obtained from back-gated transfer characteristics of the as-grown $Ge_{0.94}Sn_{0.06}$ a) and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ b) after deposition of source/drain Ni contacts in step (12), Al_2O_3 deposition in step (13), top-gate fabrication in step (18) and post-fabrication FLA in step (19). Within the graphs, the I_{off} is highlighted by downwards-pointing violet triangles, V_{th} is highlighted by rightwards-pointing grey triangles, and I_{on} is highlighted by leftwards-pointing orange triangles.

The n-branches of the characteristics in Fig. 6.3 - 1 are quantitatively analyzed in Table 6.3 - 1 by extracting the subthreshold swing *SS*, V_{th}, V_{FB}, I_{on}, I_{off}, I_{on}/I_{off}-ratio, and the maximum I_{DS} current (I_{max}) at V_{BG} = 40 V. After deposition of the Ni source/drain contacts, the alloy-related characteristics have high I_{on} = 2.1 µA (V_{FB} = 19.5 V) for $Ge_{0.94}Sn_{0.06}$ and 4.4 µA (V_{FB} = 12.6 V) for $Si_{0.14}Ge_{0.80}Sn_{0.06}$, but small I_{on}/I_{off}-ratios of 1×10^3 and 2×10^3, since the unpasivated surface limits the ability to turn off the device. This is reflected in the large I_{DS} leakage currents of I_{off} = 2130 pA ($Ge_{0.94}Sn_{0.06}$) and 2470 pA ($Si_{0.14}Ge_{0.80}Sn_{0.06}$). The high I_{on} is related to the high conductivity of the highly n-type doped NW. The I_{on} of the $Si_{0.14}Ge_{0.80}Sn_{0.06}$ JNTs is generally higher than that of the $Ge_{0.94}Sn_{0.06}$ JNTs because of the higher material quality (see **section 5.2.1**) and the larger conducting NW cross-section. After deposition of Al_2O_3, the I_{on} increase to I_{on} = 4.3 µA (V_{FB} = 17.6 V) for $Ge_{0.94}Sn_{0.06}$ and 6.6 µA (V_{FB} = 17.8 V) for $Si_{0.14}Ge_{0.80}Sn_{0.06}$

and simultaneously the I_{off} reduces to 0.86 pA for $Ge_{0.94}Sn_{0.06}$ and 57 pA for $Si_{0.14}Ge_{0.80}Sn_{0.06}$ owing to the passivation of the NW surface. This measure eliminates undesired charge traps and dangling bonds at the NW surface and helps to increase the I_{on}/I_{off}-ratio to 5 x 10^6 for $Ge_{0.94}Sn_{0.06}$ and 1 x 10^5 for $Si_{0.14}Ge_{0.80}Sn_{0.06}$.

Table 6.3 - 1: Subthreshold swing *SS*, drain-source off-current I_{off}, threshold voltage V_{th}, flat-band voltage V_{FB}, drain-source on-current I_{on} at V_{FB}, maximum drain-source on-current in accumulation mode I_{max} and the I_{on}/I_{off}-ratio of the $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI back-gated transistors, presented in Fig. 6.3 - 1. Details about the extraction of the device parameters can be obtained in **appendix 8.21-8.24**.

Fabrication step		*SS* (mV dec.$^{-1}$)	I_{off} (pA)	V_{th} (V)	V_{FB} (V)	I_{on} (µA)	I_{max} (µA)	I_{on}/I_{off}
$Ge_{0.94}Sn_{0.06}$	Ni contacts (12)	3966	2130	4.61	19.51	2.07	5.24	1.1 x 10^3
	Al_2O_3 (13)	2639	0.858	7.29	17.64	2.16	5.87	5.1 x 10^6
	Pt TG (18)	2677	0.032	21.25	29.79	1.14	2.82	3.6 x 10^7
	FLA (19)	1470	0.027	18.30	27.30	1.16	2.84	3.7 x 10^7
$Si_{0.14}Ge_{0.80}Sn_{0.06}$	Ni contacts (12)	3448	2470	-3.00	12.59	4.36	10.10	1.8 x 10^3
	Al_2O_3 (13)	3088	57.4	0.12	17.80	6.63	14.50	1.2 x 10^5
	Pt TG (18)	2096	0.225	3.70	14.76	3.23	8.08	1.4 x 10^7
	FLA (19)	1370	0.171	22.30	28.60	3.46	8.84	2.0 x 10^7

After the deposition of the TG, the I_{on} is slightly reduced to 1.1 µA (V_{FB} = 29.8 V) for $Ge_{0.94}Sn_{0.06}$ and 3.2 µA (V_{FB} = 14.8 V) for $Si_{0.14}Ge_{0.80}Sn_{0.06}$ since the electric field of the grounded Pt TG reduces the conducting NW cross-section by a remaining depletion zone close to the NW surface. On the other hand, the inherent electric field emerging from the work function of the Pt top-gate allows the JNT to be turned off more efficiently. Therefore, I_{off} is further reduced to 0.03 pA for $Ge_{0.94}Sn_{0.06}$ and 0.23 pA for $Si_{0.14}Ge_{0.80}Sn_{0.06}$, and the I_{on}/I_{off}-ratio reaches about 4 x 10^7 for $Ge_{0.94}Sn_{0.06}$ and 1 x 10^7 for $Si_{0.14}Ge_{0.80}Sn_{0.06}$ after the top-gate fabrication. At this stage, it is important to note that the I_{off} in JNTs is mainly determined by the electrostatic control of the gate on the current in the channel and not by the leakage current of a reverse-biased diode, as in the MOSFET case [260]. This makes the JNT performance less sensitive to temperature variations and helps to minimize the leakage current in low band-gap materials, such as Ge, $Ge_{1-x}Sn_x$, and $Si_{1-x-y}Ge_ySn_x$ due to band-to-band-tunneling. Hence, the lower I_{off} of $Ge_{0.94}Sn_{0.06}$ compared to $Si_{0.14}Ge_{0.80}Sn_{0.06}$ can be attributed to the much smaller NW dimension, which improves the gate control. The large I_{on} and small I_{off} values of both types of JNTs could be maintained after post-fabrication FLA. However, the I_{off} position in Fig. 6.3 - 1 is shifted towards positive V_{BG} for both alloys after FLA. This might be related to the formation of negative interface charges, which need to be compensated by a more positive V_{BG}. The influence of the post-growth FLA will be discussed in detail in **section 6.3.4**. Comparing I_{on} at V_{BG} = V_{FB} with I_{max} at V_{BG} = 40 V in Table 6.3 - 1 shows

a further increase of I_{DS} for $V_{BG} > V_{FB}$ for all fabrication states due to the screening effect in the accumulation mode, as explained in **section 6.1**. The extracted *SS* of JNTs at different fabrication states, summarized in Table 6.3 - 1, is relatively large due to the large dimensions of the back-gate structure consisting of a 100 nm thick SiO_2 on a 750 µm thick Si carrier wafer, which reduces the gate coupling to the active layer in the NW. Nevertheless, a significant performance improvement can be observed in the progress of the JNT fabrication. The *SS* drops down from 3966 mV dec.$^{-1}$ for $Ge_{0.94}Sn_{0.06}$ and 3448 mV dec.$^{-1}$ for $Si_{0.14}Ge_{0.80}Sn_{0.06}$ after the Ni contact fabrication to 1407 mV dec.$^{-1}$ for $Ge_{0.94}Sn_{0.06}$ and 1370 mV dec.$^{-1}$ for $Si_{0.14}Ge_{0.80}Sn_{0.06}$ after FLA. The V_{th} of the device shows a trend towards positive V_{BG} after each processing step. Only the $Ge_{0.94}Sn_{0.06}$ FLA state is an outlier of this behavior due to the significantly improved *SS* compared to the Pt TG state. The general trend can be attributed to i) the generation of fixed charges at the NW interface with the gate dielectric, which is most likely the case for deposition of Al_2O_3 [284] and FLA or ii) confinement of the carriers in the NW in the case for the Pt top-gate deposition. Both effects require a larger back-gate potential to generate a first conduction path within the NW.

6.3.2 JNT performance in dependence on post-growth PLA

The influence of the post-growth PLA (step (2) in Fig. 6.2 - 1) is investigated by back-gated and top-gated transfer characteristics after top-gate fabrication in step (18). For this experiment, JNTs with a NW length of L_{NW} = 3 µm and a NW width of W_{NW} = 90 nm ($Ge_{1-x}Sn_x$) and 200 nm ($Si_{1-x-y}Ge_ySn_x$) were selected. The measurement results of $Ge_{1-x}Sn_x$ in the as-grown state and after PLA with E_d = 0.12 and 0.15 J cm^{-2} as well $Si_{1-x-y}Ge_ySn_x$ in the as-grown state and after PLA with E_d = 0.15, 0.20 and 0.25 J cm^{-2} are presented in Fig. 6.3 - 2. The top-gated $Ge_{1-x}Sn_x$ JNTs in Fig. 6.3 - 2 a) turn off at $V_{TG} \approx 0$ V and show a clear saturation below and above the subthreshold region. On the other hand, the $Si_{1-x-y}Ge_ySn_x$ JNTs Fig. 6.3 - 2 b) turn off at around $V_{TG} \approx -2$ V but show a proceeding reduction in I_{DS} for $V_{TG} < -2$ V. Hence, the $Ge_{1-x}Sn_x$ JNTs are normally-OFF transistors, and the $Si_{1-x-y}Ge_ySn_x$ JNTs are in an intermediate state between a normally-ON and a normally-OFF JNT. In general, a normally-ON n-type JNT can be fabricated by increasing the W_{NW}, d_{NW}, d_{ox}, or active carrier concentration or lowering the top-gate work function or W_{TG}. Since the d_{NW} and d_{ox} are almost the same for both materials, the active carrier concentration in $Si_{1-x-y}Ge_ySn_x$ is lower than for $Ge_{1-x}Sn_x$ and W_{TG} is larger for $Si_{1-x-y}Ge_ySn_x$, it is possible to conclude that the W_{NW} of $Si_{1-x-y}Ge_ySn_x$ JNTs is too large to deplete the NW channel entirely with the TG. Additionally, the corresponding back-gated JNT characteristics confirm this JNT classification (normally-ON/OFF) by the position of I_{off}. Whereas I_{off} is located at $V_{BG} \approx 4$ V for the

$Ge_{1-x}Sn_x$ JNTs, the I_{off} of the $Si_{1-x-y}Ge_ySn_x$ JNTs is around $V_{BG} \approx -18$ V, which is far away from $V_{BG} = 0$ V zero and makes it difficult to close the channel for the $Si_{1-x-y}Ge_ySn_x$ JNTs by the TG.

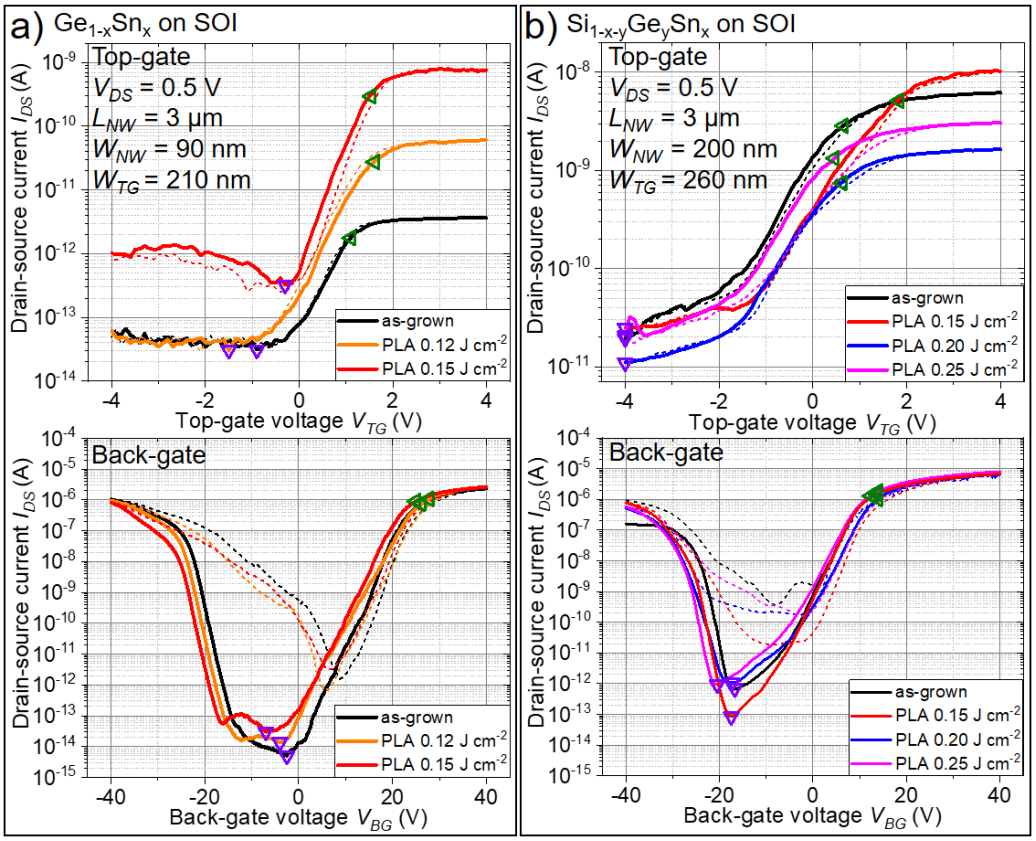


Fig. 6.3 - 2: Top-gated (top) and back-gated (bottom) transfer characteristic of $Ge_{1-x}Sn_x$ a) and $Si_{1-x-y}Ge_ySn_x$ b) JNTs after top-gate fabrication in step (18) in dependence on different post-growth PLA treatments in step (2). The $Ge_{1-x}Sn_x$ JNTs device dimensions are L_{NW} =3 µm long and W_{NW} = 90 nm wide NW with a W_{TG} = 210 nm wide TG. The $Si_{1-x-y}Ge_ySn_x$ JNTs device dimensions are L_{NW} =3 µm long and W_{NW} = 200 nm wide NW with a W_{TG} = 260 nm wide TG. The solid line corresponds to the forward sweep, and the dashed line corresponds to the backward sweep. The I_{on} at V_{FB} is highlighted with green left-pointing triangles, and I_{off} is highlighted with violet downwards-pointing triangles.

The transfer characteristics of Fig. 6.3 - 2 were analyzed in terms of *SS*, I_{on}/I_{off}-ratio, and I_{max}/I_{Off}-ratio. The summarized results of the $Ge_{1-x}Sn_x$ JNTs in Fig. 6.3 - 3 a) show an increasing *SS* and decreasing I_{DS}-ratios for increasing PLA E_d in the back-gated case. On the other hand, the top-gated results depict an opposite trend in *SS* and I_{DS}-ratios. This could be understood by the access of the top-/back-gate with respect to the depth-dependent layer quality and active doping level under the assumption of a thicker $Ge_{1-x}Sn_x$ layer. For the $Ge_{0.94}Sn_{0.06}$ as-grown state, close to the $Ge_{0.94}Sn_{0.06}$/Si interface, is a very thin $Ge_{0.94}Sn_{0.06}$ layer - grown layer by layer in the Frank-van der Merwe mechanism. This pseudomorphically grown layer can be easily accessed from the back-gate, and simultaneously, the top-gate work function depletes a part of the defect-rich not annealed upper section of the $Ge_{0.94}Sn_{0.06}$ layer (see TEM results in

Fig. 5.2 - 1 c) and e)). This would explain the slightly lower *SS* ≈ 2600 mV dec.$^{-1}$ and high I_{DS}-ratios (I_{on}/I_{off}-ratio ≈ 1.5 x 10^8 and I_{max}/I_{off}-ratio ≈ 5 x 10^8) of the back-gated as-grown $Ge_{0.94}Sn_{0.06}$ JNT. However, after PLA, the $Ge_{1-x}Sn_x$ layer quality became better, and the carrier concentration increased, as shown in **sections 5.2.3** and **5.2.4**. If one assumes the presence of a better $Ge_{1-x}Sn_x$ quality towards the surface, then the TG can access this material better, which explains the improving TG performance after PLA. In fact, the *SS* improved from about 750 mV dec.$^{-1}$ of the as-grown state to about 450 mV dec.$^{-1}$ after PLA with 0.15 J cm^{-2}. Furthermore, the top-gated I_{DS}-ratio increased from I_{on}/I_{off}-ratio = 5 x 10^1 and I_{max}/I_{off}-ratio = 1 x 10^2 in the as-grown state to I_{on}/I_{off}-ratio ≈ 9 x 10^2 and I_{max}/I_{off}-ratio ≈ 2 x 10^3 after PLA. On the other hand, taking the about 3 nm thin $Ge_{1-x}Sn_x$ layer thickness, observed in cross-sectional TEM in Fig. 6.2 - 3 a), into account, one has to consider the complex influence from the p-type Si beneath the n-type $Ge_{1-x}Sn_x$ layer as one potential candidate for the different top- and back-gated JNT performances. However, the investigation of the influence of the vertical p-n-junction on the electrical measurements is beyond the scope of this thesis. For simulations, one would require the knowledge of the Si p-type JNT fabricated with an n-type JNT approach, as presented in Fig. 6.2 - 1, as well as annealing-dependent $Ge_{1-x}Sn_x$ material properties of the about 3 nm thin $Ge_{1-x}Sn_x$ layers.

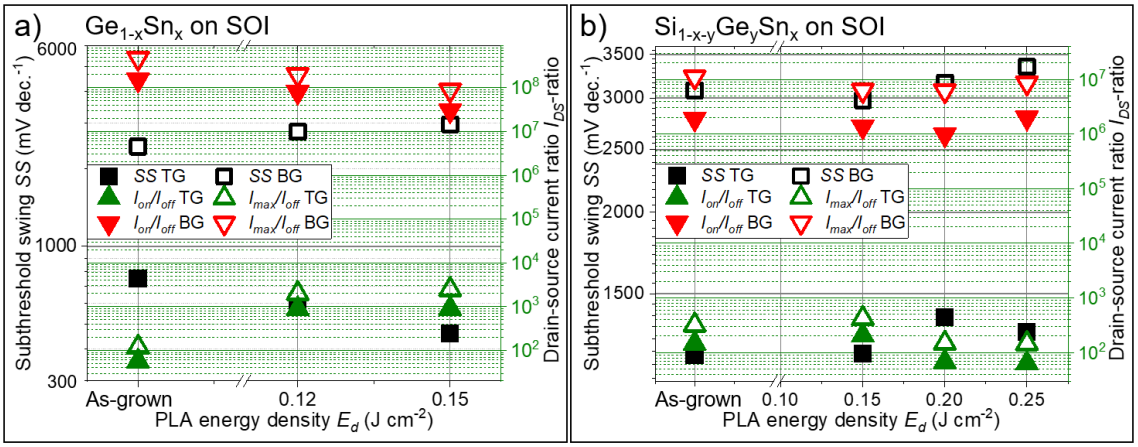


Fig. 6.3 - 3: Subthreshold swing *SS* and drain-source current I_{DS}-ratios of the top-gated TG and back-gated BG $Ge_{1-x}Sn_x$ a) and $Si_{1-x-y}Ge_ySn_x$ b) JNTs in dependence on the used post-growth PLA energy density E_d. The parameters are extracted from the transfer characteristics in Fig. 6.3 - 2. Details about the parameter extraction can be obtained in **appendix 8.22** and **8.23**.

The analysis of the $Si_{1-x-y}Ge_ySn_x$ JNTs in Fig. 6.3 - 3 b) shows an improved electrical performance for the top- and back-gated cases after PLA 0.15 J cm^{-2} compared to the as-grown state. This might be related to the higher active carrier concentration, the partly remaining $Si_{1-x-y}Ge_ySn_x$ bottom layer, and increased material quality after PLA with E_d = 0.15 J cm^{-2}. On the other hand, the reduced performance of the PLA 0.20 and 0.25 J cm^{-2} treated $Si_{1-x-y}Ge_ySn_x$ layers highlights the electrically improving influence of

Sn within the $Si_{1-x-y}Ge_ySn_x$ alloy since these layers showed an Sn out-diffusion due to PLA. However, this Sn- and oxygen-rich top layer is removed during the device fabrication, as explained in **section 6.2**.

Both types of top-gated JNTs in Fig. 6.3 - 2 have a relatively small hysteresis if we compare the forward- (solid line) with the backward-sweep (dashed line). This confirms the bulk conduction mechanism and suitable NW/Al_2O_3 interface properties in the accumulation mode. This is also reflected in the about 200% to 300% higher I_{max}/I_{off}-ratios compared to the I_{on}/I_{off}-ratios in Fig. 6.3 - 3.

An overall comparison between the $Ge_{1-x}Sn_x$ and the $Si_{1-x-y}Ge_ySn_x$ JNTs in Fig. 6.3 - 3 revealed a much better device performance of the $Ge_{1-x}Sn_x$ JNTs. Therefore, the following sections will focus on the $Ge_{1-x}Sn_x$ JNTs. Potential reasons for the lower $Si_{1-x-y}Ge_ySn_x$ JNT performances are the larger W_{NW} and the Si concentration in the alloy, which reduces the charge carrier mobility but improves the layer quality. However, further experiments with the same W_{NW} dimensions are necessary to compare both materials clearly.

6.3.3 Gate configuration of $Ge_{1-x}Sn_x$ JNTs

Significant differences in the device performance using TG and BG were observed in Fig. 6.3 - 3. While the JNTs have the desired large I_{on}/I_{off}- and I_{max}/I_{off}-ratios of about 1×10^7 to 4×10^8 under BG control, the device switching behaviors are much better under TG control with $SS \approx$ 450-500 mV dec.$^{-1}$. In order to benefit from high I_{DS}-ratios and small SS, it appears to be beneficial to apply a constant BG potential and sweep TG potential of the JNT, as shown in Fig. 6.3 - 4 a) on the example of $Ge_{1-x}Sn_x$ PLA 0.12 J cm^{-2} JNT with the device dimensions of L_{NW} = 500 nm, W_{NW} = 90 nm and W_{TG} = 140 nm.

The I_{DS}-V_{TG} characteristics in Fig. 6.3 - 4 a) show a relatively constant I_{off} of around 10 fA nearly independent of V_{BG}. On the other hand, the I_{on} increases significantly with increasing V_{BG} from 11 pA at V_{BG} = 0 V up to 0.48 µA at V_{BG} = 17 V. Hence, the analysis of the I_{on}/I_{off}-ratios in Fig. 6.3 - 4 b) shows a significant increase from 5×10^2 at V_{BG}= 0 V to a remarkable 7.2×10^7 at V_{BG} = 17 V. Furthermore, the I_{max}/I_{off}-ratio of the JNT in the accumulation mode follows the same trend and increases from 1.2×10^3 at V_{BG}= 0 V to 1.5×10^8 at V_{BG}= 17 V. These I_{DS}-ratios at V_{BG} = 17 V are already in the same range as those for the pure back-gated configuration of devices: $I_{on}/I_{off} = 7.7 \times 10^7$ and $I_{max}/I_{off} = 2.3 \times 10^8$. The general difference between the TG and BG cases can be understood by the different active device architectures. In the back-gated case, the BG potential affects the whole $Ge_{1-x}Sn_x$ structure, including the source/drain contacts shown in Fig. 6.2 - 2 c). This lowers the total $Ge_{1-x}Sn_x$ resistance and improves the Schottky-like

contacts due to enhanced band bending [55], which increases I_{on}, as later observed in **section 6.3.4**. In the case of the top-gated JNT, the gate width covers only a fraction of the NW, which allows the control of the JNT but does not allow carrier injection away from the TG.

Furthermore, the analysis of the *SS* in Fig. 6.3 - 4 b) shows an interplay between both gates. When the JNT is controlled only by the TG at V_{BG} = 0 V, the *SS* is about 600 mV dec.$^{-1}$. Afterward, the *SS* value drops down for small V_{BG} and reaches a minimum of 490 mV dec.$^{-1}$ at V_{BG} = 4 V since the combination of TG and BG simulates a kind of gate-all-around structure. Then, the *SS* increased towards higher V_{BG} up to 555 mV dec.$^{-1}$ at V_{BG} = 17 V because of an interaction of both gates, as visible in the variation of the subthreshold slopes.

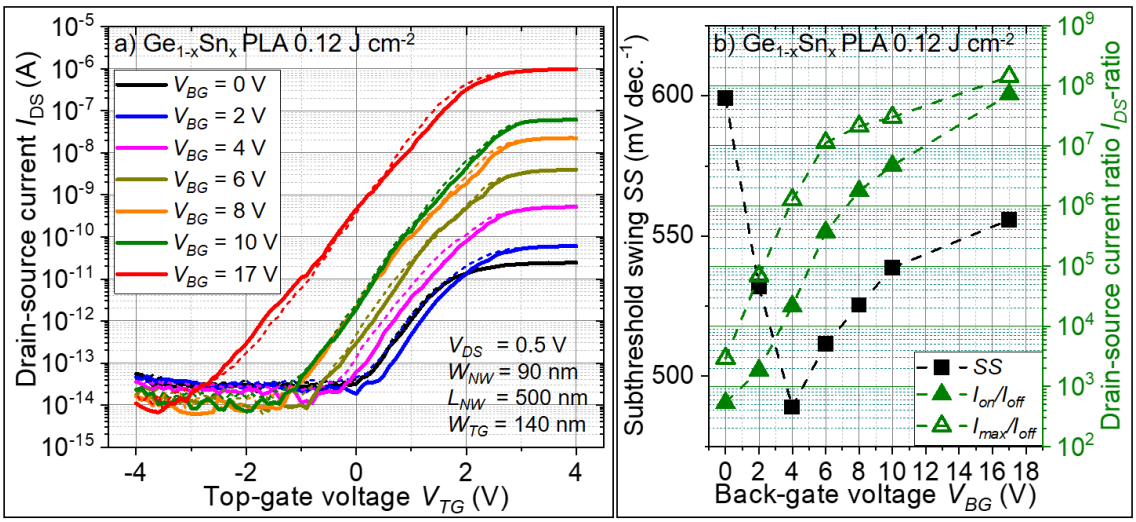


Fig. 6.3 - 4: Top-gated transfer characteristics of a $Ge_{1-x}Sn_x$ PLA 0.12 J cm^{-2} JNT with a NW length of L_{NW} = 500 nm, width of W_{NW} = 90 nm, and a top-gate width W_{TG} = 140 nm in dependence on a constant back-gate potential V_{BG} between 0 and 17 V a). Extracted minimum subthreshold swing *SS* and drain-source current I_{DS}-ratios of the JNTs shown in a) in dependence on V_{BG} b). Details about the parameter extraction can be obtained in **appendix 8.22** and **8.23**.

Similar measurements were also performed for the $Si_{1-x-y}Ge_ySn_x$ JNTs to observe the influence of the gate configuration for devices with a larger NW width, as shown in **appendix 8.25**. For these structures, the ability to boost the I_{DS}-ratio by applying an additional constant V_{BG} is more limited since the JNTs cannot be fully turned off, as discussed in **section 6.3.2**. Hence, the I_{on}/I_{max} increases with V_{BG}, but I_{off} increases simultaneously. On the other hand, the I_{max}/I_{off}-ratio is 1.1 x 10^5 without applying any V_{BG}.

Based on the presented results, it is possible to conclude that the combined application of the V_{BG} and V_{TG} potentials simulates a kind of gate-all-around JNT architecture, which allows to drive the JNT to an operating point by using a constant V_{BG} and then modulating the current by the V_{TG} sweep. In order to achieve better JNT performances, it is required

to reduce the NW dimensions (L_{NW}, W_{NW}) and W_{TG}, as discussed in **Chapter 7** in more detail.

6.3.4 Influence of post-fabrication FLA on $Ge_{1-x}Sn_x$ JNTs

In this section, the influence of the post-fabrication FLA in step (19) of Fig. 6.2 - 1 is discussed based on the $Ge_{1-x}Sn_x$ PLA 0.12 J cm^{-2} JNT with the device dimensions of L_{NW} = 1 µm, W_{NW} =78 nm and W_{TG} = 167 nm. Fig. 6.3 - 5 a) shows the back-gated transfer characteristics of the selected JNT before and after FLA. After FLA, the *SS* is reduced from 3050 to 2020 mV dec.$^{-1}$, and the back-gated characteristic is shifted towards positive V_{BG} since negative charges are formed at the Al_2O_3/NW surface. This shift correlates qualitatively with the presented back-gated $Ge_{0.94}Sn_{0.06}$ as-grown JNT after FLA treatment in **section 6.3.1**. Furthermore, for both FLA-treated JNTs, the I_{off} is slightly decreased, and the I_{max} slightly increased due to improved interface properties of the involved layers and a generally lower contact resistance (see Fig. 6.3 - 5 a) and Fig. 6.3 - 1 a)). For instance, in Fig. 6.3 - 5 a) I_{off} decreases from 10 fA at V_{BG} = -4.25V to 6 fA at V_{BG} = 3.75 V, and I_{max} increased from 3.8 µA to 9.4 µA at V_{BG} = 40V. The observed shift of the back-gated transfer characteristics Fig. 6.3 - 5 a) is about 8 V according to the minimum in I_{DS}, making it difficult to directly compare the JNT performance before and after FLA.

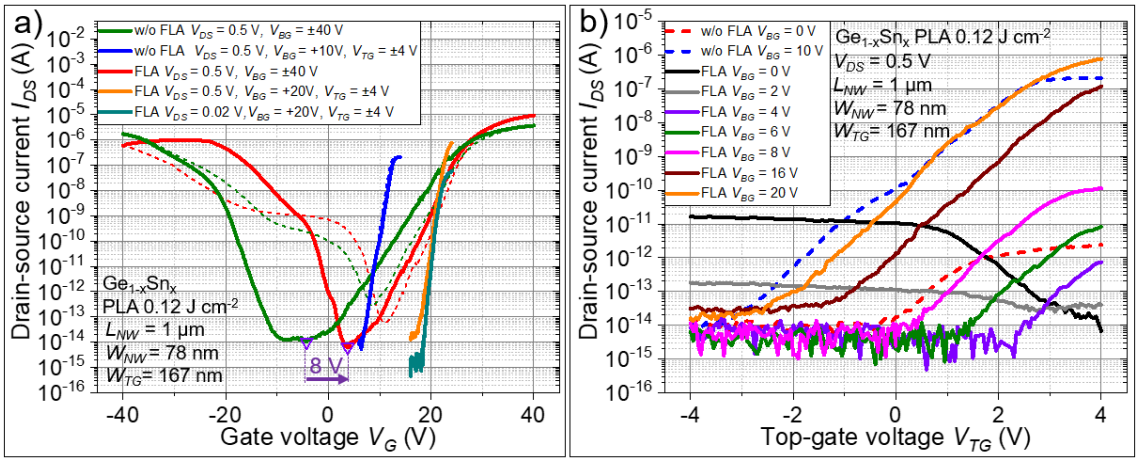


Fig. 6.3 - 5: Transfer characteristics of a $Ge_{1-x}Sn_x$ PLA 0.12 J cm^{-2} JNT with a L_{NW} = 1 µm long and W_{NW} = 78 nm wide NW and a W_{TG} = 163 nm wide TG with and without post-fabrication FLA with 48 J cm^{-2} for 3.2 ms. The characteristics are measured with and without (w/o) FLA by sweeping the back-gate potential V_{BG} or by applying a constant V_{BG} = 10 V or 20 V and sweeping the top-gate potential V_{TG} a). Evolution of the top-gated transfer characteristics with and without FLA in dependence on a constant V_{BG} b). The gate voltage V_G in a) is a summation of V_{TG} and V_{BG}.

A qualitative similar shift can be observed by comparing the top-gated characteristics with and without FLA for V_{BG} = 0 V in Fig. 6.3 - 5 b). After FLA, the top-gated characteristics with a constant V_{BG} = 0 V and 2 V have a decreasing I_{DS} towards positive

V_{TG} (see Fig. 6.3 - 5 b)). This p-type JNT characteristic is qualitatively similar to the shape of the back-gate characteristic at V_{BG} = ±4 V after FLA in Fig. 6.3 - 5 a) and is related to the contribution of the p-type Si or the negatively charged traps at the Al_2O_3/NW interface. For V_{BG} > 2 V, a clear n-type JNT behavior, qualitatively similar to the earlier discussed result in **section 6.3.3**, is visible in Fig. 6.3 - 5 b). Furthermore, an increased top-gate leakage current was noticed, from 0.1 pA before FLA to about 120 pA after FLA. The higher leakage current might be related to a slight diffusion of Sn into Al_2O_3, which was reported after RTA in ref. [71]. This could also be the reason for the more negative charge states on the Al_2O_3/NW interface. If we take the shift of about 8 V into account and compare the characteristic w/o FLA at V_{BG} = 10 V with the FLA-treated result at V_{BG} = 16 V in Fig. 6.3 - 5 b), then qualitative similar I_{max} and I_{off} values can be observed, and a straighter subthreshold slope occurs after FLA. However, the shift of about 8 V is just an approximation and is invalid for all characteristics since the back-gated subthreshold slopes in Fig. 6.3 - 5 a) are not identical. Therefore, a more detailed comparison of the *SS*, I_{on}/I_{off}-ratio, and I_{max}/I_{off}-ratio with and w/o post-fabrication FLA is presented in Fig. 6.3 - 6.

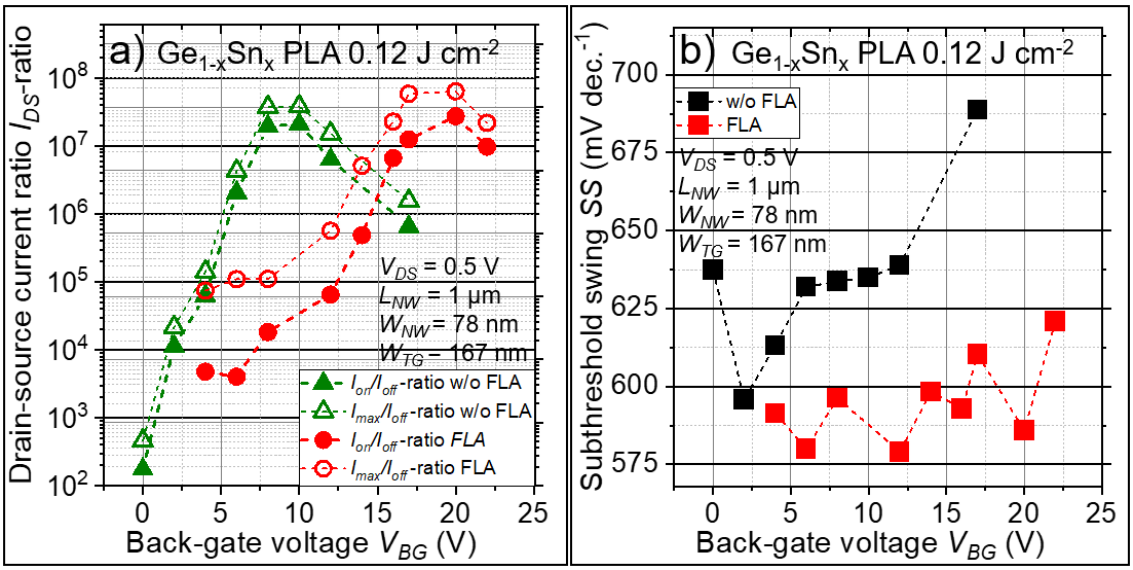


Fig. 6.3 - 6: Drain-source current I_{DS}-ratios a) and subthreshold swing *SS* b) of the $Ge_{1-x}Sn_x$ PLA 0.12 J cm^{-2} JNT with and without (w/o) post-fabrication FLA in dependence on an applied constant back-gate potential. The dimensions of the JNT are L_{NW} = 1 µm long and W_{NW} = 78 nm wide NW with a W_{TG} = 167 nm wide TG.

The JNTs w/o post-fabrication FLA show increasing I_{on}/I_{off}- and I_{max}/I_{off}-ratios with increasing V_{BG} until they reach a maximum at V_{BG} ≈ 8-10 V and decrease afterward. A similar trend is also observed after FLA but shifted for about +8 to +10 V in V_{BG}. This shift coincides with the mentioned I_{off}-shift earlier observed in the back-gated characteristics in Fig. 6.3 - 5 a). Furthermore, the global I_{DS}-ratios maxima in Fig. 6.3 - 6 a) are higher after FLA, which coincides with the pure back-gated results. Inserting the top-gated

transfer characteristics with the highest I_{DS}-ratios from Fig. 6.3 - 6 a) with and w/o FLA in Fig. 6.3 - 5 a) leads to the conclusion that the large I_{DS}-ratios of the back-gated results can be achieved before and after post-fabrication FLA. However, FLA allows for more homogeneous *SS* as well as higher I_{DS}-ratios. Furthermore, lowering the V_{DS} supply voltage from 0.5 V to 0.02 V allows for shifting the entire transfer characteristics to lower I_{DS} while maintaining the superb I_{DS}-ratios, as shown in Fig. 6.3 - 5 a) on the example of the top-gated characteristic with a constant V_{BG} = 20 V. Such characteristics are interesting for high-performance devices with low power consumption in the standby mode.

The influence of FLA on the contact quality is analyzed by output characteristics presented in Fig. 6.3 - 7. In Fig. 6.3 - 7 a), significantly larger absolute currents can be observed for negative V_{DS}. Therefore, the characteristics appear to be Schottky-like despite the high doping level. This can be related to a Fermi level pinning earlier observed for Ge [280]. After FLA, the characteristics in Fig. 6.3 - 7 c), especially for V_{TG} = 4 V, show a shottky-like but more linear and symmetric behavior, indicating improved contact qualities. However, the results were obtained with a simultaneously applied constant V_{BG} = 8 V to compensate for the shift in V_{BG}. This V_{BG} can also influence the Schottky barrier height [55]. Therefore, the output characteristics of the JNT w/o FLA and a constant V_{BG} = 8 V are presented in Fig. 6.3 - 7 b) to investigate the influence of the V_{BG} on the contact quality. In Fig. 6.3 - 7 b), similar absolute I_{DS} can be observed for V_{DS} = +0.5 and -0.5 V at V_{TG} = 3 V and 4 V, which correlates qualitatively with the findings in Fig. 6.3 - 7 c) after FLA. On the other hand, the straightness is much higher after FLA, which confirms improved contacts.

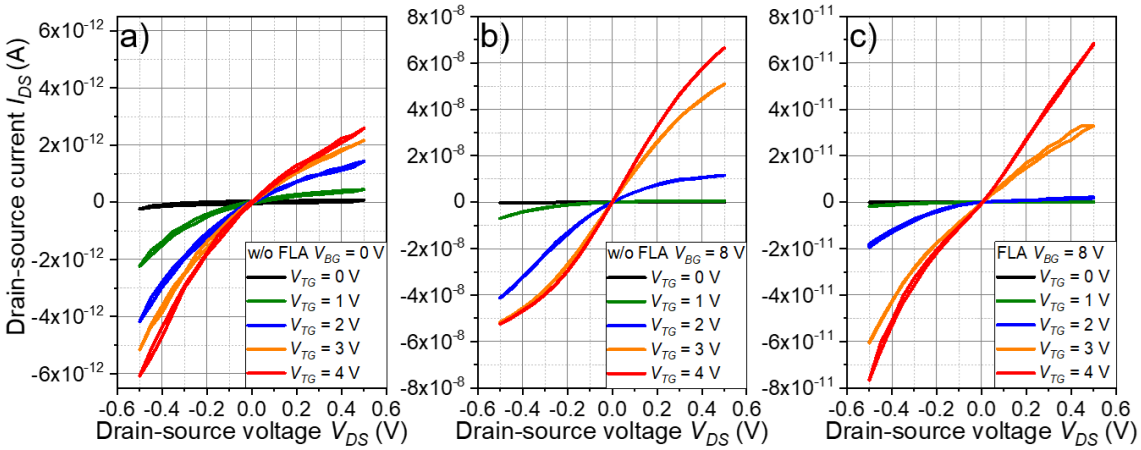


Fig. 6.3 - 7: Output characteristics of the $Ge_{1-x}Sn_x$ PLA 0.12 J cm^{-2} JNT without (w/o) post-fabrication FLA a) - b) and after post-fabrication FLA with E_d = 48 J cm^{-2} for 3.2 ms c). The measurement in a) is performed without the application of V_{BG} and b) - c) is performed under a constant V_{BG} = 8 V. The dimensions of the JNT are L_{NW} =1 µm long and W_{NW} = 78 nm wide NW with a W_{TG} = 167 nm wide TG.

6.4 Conclusion

Lateral n-type $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI transistors were successfully fabricated using a top-down gate-last JNT approach. Back-gated transfer characteristics of the as-grown $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI JNTs showed a significant evolution in device performance during manufacturing. In fact, the *SS* of the normally-Off $Ge_{0.94}Sn_{0.06}$ JNTs decreased from 3966 mV dec.$^{-1}$ after deposition of Ni source/drain contacts to 1470 mV dec.$^{-1}$ after FLA. Simultaneously, the I_{on}/I_{off}- and I_{max}/I_{off}-ratios increased from 9.7 x 10^2 and 2.5 x 10^3 after deposition of Ni source/drain contacts to 4.3 x 10^7 and 1.1 x 10^8 after FLA. The overall performance of the $Si_{0.14}Ge_{0.80}Sn_{0.06}$ JNTs was slightly worse than that of the $Ge_{0.94}Sn_{0.06}$ JNTs. The deposition of Al_2O_3 as a gate dielectric and a Pt top-gate enabled the control of the JNTs by the top-gate. The beneficial combination of the JNT device concept and the Al_2O_3 layer resulted in a small hysteresis of the top-gated JNTs. The JNT performance of the as-grown alloys could be increased due to the implementation of a post-growth PLA, which improved the layer quality and increased the amount of activated Sb-dopants inside the NWs. In the case of the top-gated $Ge_{1-x}Sn_x$ JNTs, the *SS* could be decreased from 750 mV dec.$^{-1}$ in the as-grown state to 460 mV dec.$^{-1}$ after PLA with 0.15 J cm^{-2}. Furthermore, the I_{on}/I_{off}- and I_{max}/I_{off}-ratios increased from 5.7 x 10^1 and 1.2 x 10^2 in the as-grown state to 9.1 x 10^2 and 2.5 x 10^3 after PLA.

The combined application of a constant back-gate potential and top-gate sweep simulated a kind of gate-all-around JNT architecture, which allows driving the JNT to a certain operating point by using a constant back-gate potential and modulating the current through the JNT by sweeping the TG potential. Additionally, the V_{BG} reduced the Schottky-barrier height at the source and drain contacts. This quasi gate-all-around architecture allowed us to achieve I_{on}/I_{off}- and I_{max}/I_{off}-ratios of 1 x 10^8 and 1.5 x 10^8 for the $Ge_{1-x}Sn_x$ PLA 0.12 J cm^{-2} JNT. Implementing the post-fabrication FLA generated negative charges at the Al_2O_3/NW surface, which need to be compensated by the gate potential, but it improved the contact quality slightly. Therefore, the JNTs showed further increased I_{DS}-ratios by about 130% or 170% in I_{on}/I_{off} and I_{max}/I_{off}, respectively, after FLA.

7 Conclusion and future prospects

Within the framework of this thesis, the influence of non-equilibrium post-growth thermal treatments of ion implanted and epitaxially grown $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ layers for nano- and optoelectronic devices has been investigated. The main focus has been placed on the study and development of thermal treatment conditions to improve the as-grown layer quality and the fabrication of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI JNTs. In addition, through layer characterization, exhaustive analysis has provided deep insight into key material properties and the alloy´s response to the thermal treatment. For instance, (i) the conversion of as-grown in-plane compressive strained $Ge_{1-x}Sn_x$ into in-plane tensile strained $Ge_{1-x}Sn_x$ after PLA that is required for high mobility n-type transistors and (ii) the evolution of monovacancies to larger vacancy clusters due to post-growth thermal treatments. Moreover, the adaption of CMOS-compatible fabrication approaches to the novel $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys allowed the successful fabrication of first lateral n-type JNTs on SOI with remarkable I_{on}/I_{off}-ratios of up to 10^8 to benchmark the alloy performance. This section will summarize the main findings within the presented thesis, suggest the next optimization steps, and derive possible future applications for $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys.

The low solid solubility of α-Sn in Si (< 0.1%) and Ge (< 1%) demands non-equlibirum processing technologies to fabricate $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys with active Sn concentrations above 1%. In this thesis, the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys were fabricated by a) ion beam implantation of Sn in Ge or $Si_{1-y}Ge_y$ layers followed by ms-FLA or b) epitaxial growth by MBE on Si substrates. The ion beam implantation approach enables the full incorporation of up to 2.3 at.% Sn in thick Ge-based single-crystalline $Si_{0.28}Ge_{0.72}$ layers by FLA. This novel technique complements the existing vertical growth methods by a lateral modification component and can find its application in any kind of lateral device concept. For instance, local band-gap modifications achieved by nano-structuring and Sn implantation are desired for TFETs. Furthermore, it is shown that such SiGeSn fabrication method can be transferred into $Si_{0.73}Ge_{0.27}$ films grown on SOI. Even though implantation in thin films requires precise process control and further parameter optimization, it is an important step towards lateral thin film $Si_{1-x-y}Ge_ySn_x$ devices on an insulating platform.

For the MBE approach, a state-of-the-art low-temperature growth was used to fabricate $Ge_{1-x}Sn_x$ on Ge-buffered Si substrates. Afterward, ns-PLA or ms-FLA was applied to investigate the influence of non-equilibrium post-growth thermal treatments above eutectic temperature on the material properties. The annealing temperatures of these

methods depend mainly on the applied energy density, annealing time, pre-heating conditions, and the properties of the annealed material itself, like light absorption, heat capacity, thermal conductivity, and the involved layer stack. PLA with high enough energy densities melts the $Ge_{1-x}Sn_x$ alloy. After an ultra-fast liquid phase epitaxy, the previously in-plane compressive strained $Ge_{1-x}Sn_x$ layer is converted into a strain-relaxed or even in-plane tensile strained condition. Owing to the harsh solidification, Sn-rich filaments and clusters were observed within a slightly Sn-depleted $Ge_{1-x}Sn_x$ matrix. The utilization of the presented laser melting approach on highly Sb-doped $Ge_{1-x}Sn_x$ enabled an increase in the active carrier concentration from 1×10^{20} cm^{-3} in the as-grown state to about 3×10^{20} cm^{-3} (full activation) after annealing [159]. Grating antennas, fabricated from the highly doped and strain-relaxed $Ge_{1-x}Sn_x$ materials, showed a clear shift in the plasma wavelength down to 3.6 µm [159]. This emphasizes the potential of highly doped $Ge_{1-x}Sn_x$ for plasmonic applications [159]. Furthermore, strain-relaxed $Ge_{1-x}Sn_x$ might be usable as a novel CMOS-compatible virtual substrate with a large lattice parameter for growing group IV semiconductors and their alloys. This would allow the adjustment of the in-plane and out-of-plane strain in dependence on the relaxed $Ge_{1-x}Sn_x$ substrate composition and enables the fabrication, for instance, of tensile strained Ge, $Ge_{1-x}Sn_x$, or $Si_{1-x-y}Ge_ySn_x$ alloys.

Post-growth FLA of $Ge_{1-x}Sn_x$ alloys enables thermal treatments significantly above the eutectic temperature of the alloy without melting and Sn segregation. After FLA, the partly strain-relaxed grown layers show a proceeding strain relaxation. On the other hand, the fully pseudomorphically grown $Ge_{1-x}Sn_x$ layers remain fully compressive strained. Hence, the occurrence of proceeding dislocations is mainly determined by the growth process. Independent of the strain relaxation conditions, $Ge_{1-x}Sn_x$ with active B or Sb concentrations of about 1.5×10^{20} cm^{-3} were grown and FLA-treated. ms-FLA at temperatures close to the melting point did neither cause deactivation nor dopant diffusion. This makes FLA a promising approach to improve metall-$Ge_{1-x}Sn_x$ contacts without disturbing the dopant profile. However, non-equilibrium conditions in combination with the complexity of the $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ alloys require further experiments to determine the contact resistivity and the possible formation of secondary stano-germanide or silicide-stano-germanide phases. Intensive positron annihilation lifetime experiments have shown a transformation of single-vacancies into larger vacancy clusters after PLA or FLA. This purification process can improve the electrical properties of devices fabricated on these alloys. Finally, it must be concluded that the material quality of $Ge_{1-x}Sn_x$ thick films ($d \approx$ 200-300 nm) is mainly determined by their growth conditions, and the applied post-growth thermal treatments could not significantly

improve the crystal structure. Hence, to achieve the predicted high carrier mobilities of $\mu_{e^-} \approx 6000$ cm²/Vs or $\mu_{h^+} \approx 4500$ cm²/Vs, further improving the as-grown alloy qualities is required. Furthermore, a reduced defect density in the as-grown alloys would also reduce the inherent p-type background doping, which should be considered in the device design.

For future lateral thin film devices, it is desired to have high-quality $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ alloys on an insulating platform. However, fabricating such substrates is challenging, therefore they are not available yet. Hence, MBE direct growth of n-type doped $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ on commercially available SOI wafers was evaluated as an alternative approach. Unfortunately, the large lattice mismatch between the grown alloys and the SOI substrate generates defect-rich $Ge_{0.94}Sn_{0.06}$ or $Si_{0.14}Ge_{0.80}Sn_{0.06}$ thin films. Hence, the measures depicted in Fig. 7 - 1 should be considered for future experiments to increase the as-grown material quality by using this approach.

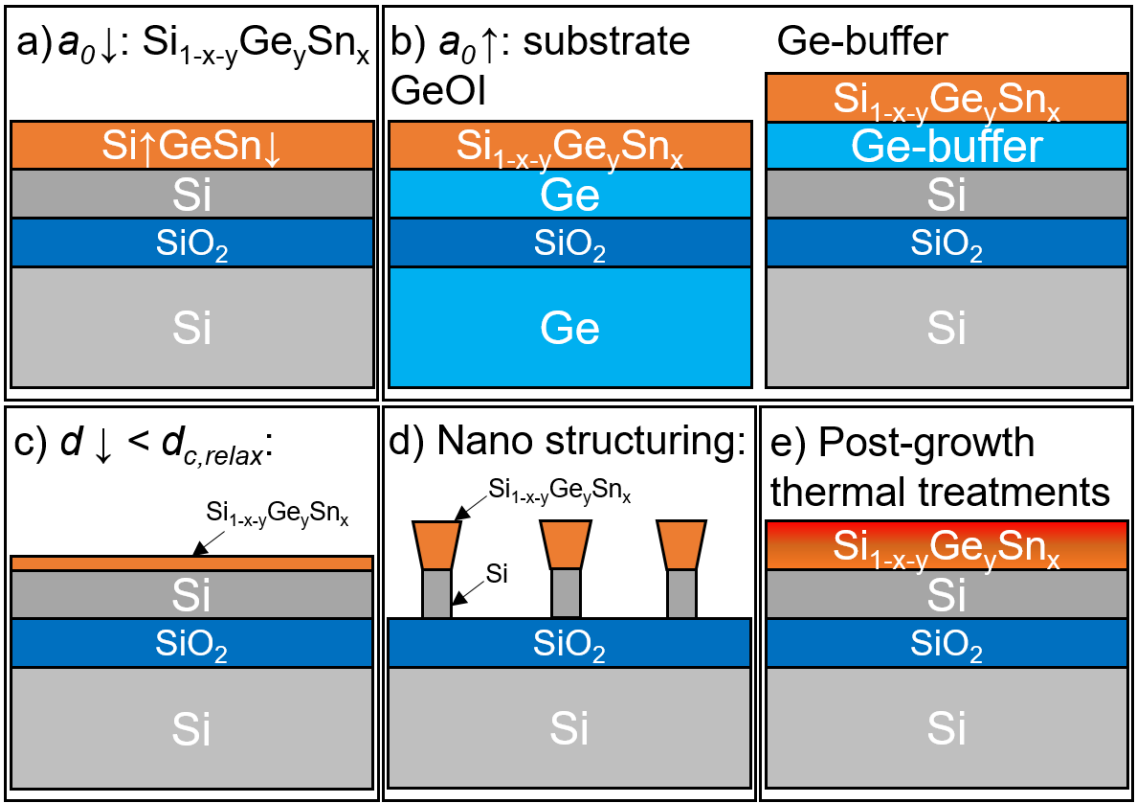


Fig. 7 - 1: Measures to increase the as-grown $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ thin film quality on an insulating platform. The relaxed lattice parameter a_0 of the alloy can be reduced by changing the alloy composition a), or a_0 of the substrate can be increased by replacing Si with Ge b) [279, 285]. The $Si_{1-x-y}Ge_ySn_x$ layer thickness d can be reduced below the critical thickness for plastically strain relaxation $d_{c,relax}$ c). Nano-structuring of the Si seed crystal allows a certain expansion of the alloy d). Post-growth thermal treatment enables the annihilation of defects e).

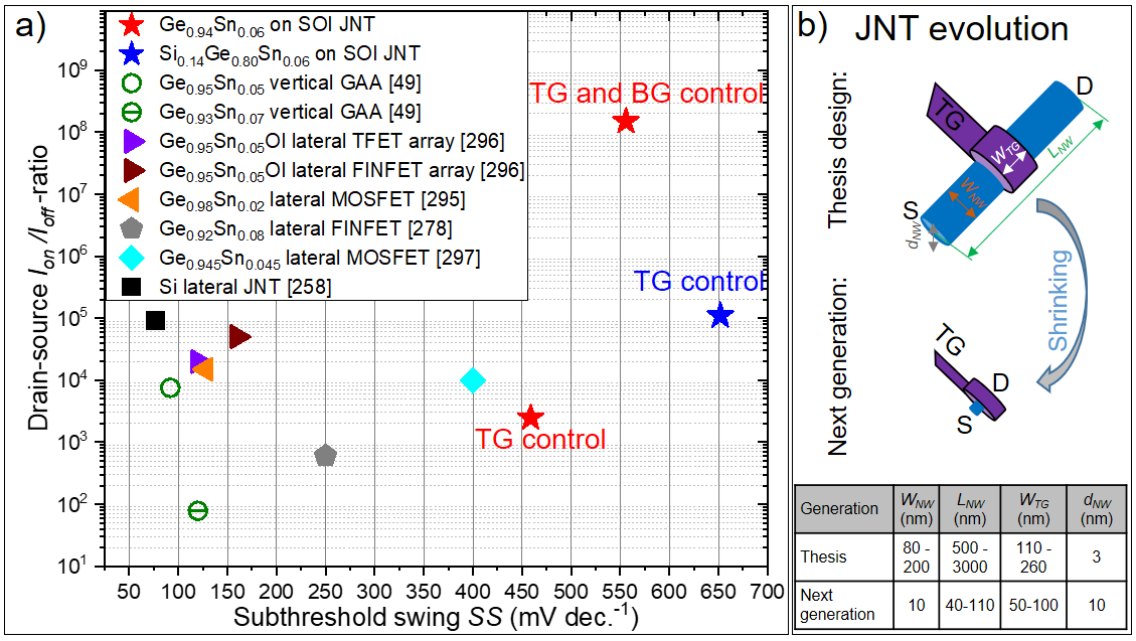
Since the lattice parameter difference plays an important role, one can modify the lattice parameter of the alloy, or the substrate, or a combination of both. The lattice parameter of the alloy can be reduced by increasing the Si concentration or decreasing the Sn concentration, as illustrated in Fig. 7 - 1 a). An improved crystal structure was already

visible in the presented results after replacing 14 at.% Ge by Si in the MBE growth recipe. However, this goes hand in hand with a reduction of the achievable electrical and optical properties of the alloys. Another option is to increase the substrate lattice parameter by inserting a Ge-buffer layer or replacing SOI with GeOI as depicted in Fig. 7 - 1 b). The lattice parameter of strain-relaxed Ge is about 4.2% larger than that of Si and would significantly reduce the in-plane strain from about -5.2% ($Ge_{0.94}Sn_{0.06}$ on Si) and -1.9% ($Si_{0.14}Ge_{0.80}Sn_{0.06}$ on Si) to -1.0% ($Ge_{0.94}Sn_{0.06}$) and +2.2% ($Si_{0.14}Ge_{0.80}Sn_{0.06}$) for the growth on Ge. As indicated by the change from in-plane compressive strain to in-plane tensile strain, it is possible to grow ternary $Si_{1-x-y}Ge_ySn_x$ latticed matched on Ge or in different strain states depending on the targeted alloy composition and final application. However, the Ge-buffer layer approach has some challenges since the buffer must be thick enough to effectively reduce the defect concentration during the *in situ* strain relaxation annealing. Furthermore, the diffusion during the annealing process can convert the Ge-buffer into a $Si_{1-y}Ge_y$-buffer with a smaller lattice parameter, and the more complex layer stack complicates the data analysis. Therefore, replacing SOI with GeOI is an easier but more expensive approach. Another option is the reduction of the grown $Ge_{1-x}Sn_x/Si_{1-x-y}Ge_ySn_x$ layer thickness below the thickness for plastically strain relaxation, as shown in Fig. 7 - 1 c). This would lead to a compositional and process-dependent very thin film of pseudomorphically grown $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys, but they can suffer from misfit dislocations at the substrate interface. Another option is the nano-structuring of the Si seed crystal before the growth, allowing a lateral expansion of the grown alloy, as shown in Fig. 7 - 1 d). Finally, there is also a possibility of applying non-equilibrium thermal treatments to improve the as-grown crystal structures, as shown in Fig. 7 - 1 e).

In the scope of this work, PLA with low energy densities was used to improve the layer quality of the 20 nm thick $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI films. The presented results confirm significantly improved crystal structure and increased active carrier concentration after PLA of the defect-rich grown thin films. On the other hand, a few nm thick Sn-rich $Si_{1-x-y}Ge_ySn_x$-oxide or $Ge_{1-x}Sn_x$-oxide layer was formed on the layer top surface during PLA and reduced the overall Sn concentration. The presence of this oxide layer might be avoidable if the PLA process is performed under an inert gas atmosphere or *in situ* in an MBE cluster toll. The fabricated PLA-treated $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ layers are almost fully strain-relaxed with a maximum lattice parameter of 0.570 nm ($Ge_{1-x}Sn_x$). This large lattice parameter would allow the fabrication of highly in-plane tensile stained Ge ($\varepsilon_{//} \approx 0.7\%$) if Ge is epitaxially grown on the presented PLA-treated $Ge_{1-x}Sn_x$ on SOI. Hence, the demonstrated thin film SiGeSn/GeSn on SOI approach could be used as a new buffer layer for various other promising materials.

In recent years, some $Ge_{1-x}Sn_x$ transistors [49, 285-295] were published to benchmark the material performance and show process capability enhancements. However, only a few n-type $Ge_{1-x}Sn_x$ transistors [49, 279, 292, 296-298] are presented among these results because of difficulties related to the unintentional p-type background doping, in-plane compressive strain, and Fermi level pinning. So far, no ternary $Si_{1-x-y}Ge_ySn_x$ transistors have been reported yet. Within the framework of this thesis, a junctionless nanowire transistor concept is applied, and CMOS-compatible processes were adapted to the n-type doped $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI materials. $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ JNTs were successfully fabricated in different post-growth annealing conditions using a top-down gate-last approach. The $Ge_{1-x}Sn_x$ JNTs are fabricated as normally-off devices, and the $Si_{1-x-y}Ge_ySn_x$ as normally-on devices, which generally shows the capability to cover different operation modes with the JNT device concept by changing the NW width. Among these JNTs, the best fabricated top-gated transistors have a *SS* of about 460 mV dec.$^{-1}$ ($Ge_{1-x}Sn_x$) and 550 mV dec.$^{-1}$ ($Si_{0.14}Ge_{0.80}Sn_{0.06}$) with maximum I_{max}/I_{off}-ratios of about 1×10^3 ($Ge_{1-x}Sn_x$) and 7×10^4 ($Si_{0.14}Ge_{0.80}Sn_{0.06}$). The fabricated JNTs are benchmarked in Fig. 7 - 2 a) with the published n-type $Ge_{1-x}Sn_x$ transistors. Even though it is difficult to compare the different device concepts directly because of different functionalities, doping levels, alloy compositions, device dimensions, etc., it gives an overview of the n-type transistor performances achieved so far.

Plotting the I_{on}/I_{off}-ratio versus the *SS* in Fig. 7 - 2 a) shows the capability to fabricate vertical GAA GeSn FETs with an almost ideal *SS* of 76 mV dec.$^{-1}$. Such small *SS* can be achieved due to high material quality, low interface defect densities, and good gate control, which proves the existence of suitable process windows for many potential applications. Here, the vertical device concept seems advantageous over the lateral configuration since the fabrication approach allows the growth of thick Ge-buffer layers, which helps to reduce the defect concentration of the active $Ge_{1-x}Sn_x$ layer. A similar growth approach was used for GeSnOI in ref. [297] before transferring the GeSn layer to the insulating substrate. Theoretically, such steep *SS* can also be achieved for JNTs made of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ since *SS* of 70 mV dec.$^{-1}$ were reported for Si JNTs with a NW diameter of about 10 nm [258].



Generation	W_{NW} (nm)	L_{NW} (nm)	W_{TG} (nm)	d_{NW} (nm)
Thesis	80 - 200	500 - 3000	110 - 260	3
Next generation	10	40-110	50-100	10

Fig. 7 - 2: Benchmark of the fabricated n-type $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI JNTs (symbol star) with n-type transistors in different device configurations measured at a constant supply voltage V_{DS} = 0.5 V for $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ [49, 258, 279, 296-298]. Details about the compared transistors are summarized in **appendix 8.26**. The supply voltage for the Si lateral JNT was V_{DS} = 0.9 V.

Fig. 7 - 2 b) illustrates suggested measures to improve the JNT device performance from the device point of view. To decrease the *SS*, the NW width is required to decrease from about 70 nm for $Ge_{1-x}Sn_x$ and about 220 nm for $Si_{1-x-y}Ge_ySn_x$ to about 10 nm. Additionally, one should reduce the NW length to lower the total resistance and decrease the channel length to about 50-100 nm [299, 300]. The relatively large top-gate width will allow sufficiently high I_{on}/I_{off}-ratios [299, 300]. Furthermore, the remaining $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ NW thickness should be increased from about 3 nm to about 10 nm to benefit more from the post-growth annealing process and reduce the impact of defects at the interface between the SOI substrate and the $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ layer. Hence, the presented $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ JNTs still have a large potential for miniaturization and better gate control. However, shrinking the NW diameter close to 10 nm requires robust processes since any NW diameter or doping level variability can affect the threshold voltage [261].

On the other hand, the application of an additional back-gate voltage while modulating the $Ge_{1-x}Sn_x$ JNTs current with the top-gate allowed to boost the I_{on}/I_{off}-ratio from 1×10^3 to record-values of up to 1×10^8. Such high I_{on}/I_{off}-ratios could be achieved since the $Ge_{1-x}Sn_x$ JNTs can be turned off entirely, which is essential for low standby power technologies. The achievable off-currents as low as <1 fA and large I_{on}/I_{off}-ratios benefit from the JNT device concept on an insulating substrate. In general, the JNT device concept is a helpful tool to evaluate the performance of new semiconductor materials in

material science since the fabrication is relatively simple and the main conduction path is located in the center of the NW, which lowers the importance of excellent interface qualities between the novel materials and the gate dielectric. Hence, the first ternary $Si_{1-x-y}Ge_ySn_x$ transistors could be fabricated.

Overall, it can be concluded that $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys are interesting semiconductor materials since they provide a wide range of electrical, optical, and chemical properties depending on their compositions and quality. This paves the way for a variety of specific group IV semiconductor applications. The predicted high carrier mobilities of up to 6000 cm^2/Vs, variable chemical etch resistance, adaptable lattice parameter, the indirect- to direct-band-gap transition, and CMOS compatibility are strong arguments for introducing these alloys as a promising material platform in nano- and optoelectronics. Furthermore, these alloys can be used in the group IV processing technology for various supporting purposes, such as etch-stop-layers, vertically stacked transistors, stressors [186], or novel virtual substrates with a large lattice parameter.

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8 Appendix

8.1 Sample list and fabrication details for Chapter 4

Table 8.1 - 1: Sample list of the $Ge_{1-x}Sn_x$ samples presented in **Chapter 4**. The layer stack (top to bottom) contains known parameters about the targeted layer thickness d, chemical composition, type of dopant, substrate temperature T_S, growth rate g_r, the flux of the Ge source Φ_{Ge}, the flux of the Sn source Φ_{Sn}, and the resistivity ρ_r of the substrate.

Sample name	Section	Layer parameters from top to bottom and fabrication parameters obtained from the MBE process log files
A4231 $Ge_{0.89}Sn_{0.11}$ as-grown	**4.1**	300 nm i-$Ge_{0.89}Sn_{0.11}$, T_S = 120 °C / 300 nm Ge-buffer T_S = 330 °C / 100 nm Ge virtual substrate T_S = 330 °C / 50 nm Si T_S = 900 °C / p-Si (100) $\rho_r \geq$ 10−20 Ω cm
PLA 0.15 J cm^{-2}	**4.1**	A4231 $Ge_{1-x}Sn_x$ after PLA with 0.15 J cm^{-2}
PLA 0.20 J cm^{-2}	**4.1**	A4231 $Ge_{1-x}Sn_x$ after PLA with 0.20 J cm^{-2}
PLA 0.25 J cm^{-2}	**4.1**	A4231 $Ge_{1-x}Sn_x$ after PLA with 0.25 J cm^{-2}
PLA 0.30 J cm^{-2}	**4.1**	A4231 $Ge_{1-x}Sn_x$ after PLA with 0.30 J cm^{-2}
PLA 0.35 J cm^{-2}	**4.1**	A4231 $Ge_{1-x}Sn_x$ after PLA with 0.35 J cm^{-2}
PLA 0.40 J cm^{-2}	**4.1**	A4231 $Ge_{1-x}Sn_x$ after PLA with 0.40 J cm^{-2}
PLA 0.50 J cm^{-2}	**4.1**	A4231 $Ge_{1-x}Sn_x$ after PLA with 0.50 J cm^{-2}
PLA 0.60 J cm^{-2}	**4.1**	A4231 $Ge_{1-x}Sn_x$ after PLA with 0.60 J cm^{-2}
A5285 $Ge_{0.89}Sn_{0.11}$ as-grown	**4.1.5**	300 nm i-$Ge_{0.89}Sn_{0.11}$, T_S = 120 °C / 300 nm Ge-buffer T_S = 330 °C / 100 nm Ge virtual substrate T_S = 330 °C / 50 nm Si T_S = 900 °C / p-Si (100) $\rho_r \geq$ 10−20 Ωcm
PLA 0.50 J cm^{-2}	**4.1.5**	A5285 $Ge_{0.89}Sn_{0.11}$ after PLA with 0.5 J cm^{-2}
A4922 $Ge_{0.91}Sn_{0.09}$ as-grown	**4.2**	200 nm n-$Ge_{0.92}Sn_{0.08}$:Sb (1 x 10^{20} cm^{-3}), T_S = 170 °C, g_r = 0.113 nm s^{-1} , Φ_{Ge} = 4.4 x 10^{14} cm^{-2}s^{-1}, Φ_{Sn} = 3.8 x 10^{13} cm^{-2}s^{-1} / 500 nm i-Ge / 50 nm Si / p-Si (100) $\rho_r \geq$ 10−20 Ω cm
r-FLA 76.6 J cm^{-2}	**4.2**	A4922 $Ge_{1-x}Sn_x$ after r-FLA 76.6 J cm^{-2}
r-FLA 84.8 J cm^{-2}	**4.2**	A4922 $Ge_{1-x}Sn_x$ after r-FLA 84.8 J cm^{-2}
r-FLA 92.6 J cm^{-2}	**4.2**	A4922 $Ge_{1-x}Sn_x$ after r-FLA 92.6 J cm^{-2}
A4925 $Ge_{0.88}Sn_{0.12}$ as-grown	**4.2**	200 nm n-$Ge_{0.88}Sn_{0.12}$:Sb (1 x 10^{20} cm^{-3}), T_S = 170 °C, g_r = 0.116 nm s^{-1} , Φ_{Ge} = 4.4 x 10^{14} cm^{-2}s^{-1}, Φ_{Sn} = 4.9 x 10^{13} cm^{-2}s^{-1} / 500 nm i-Ge / 50 nm Si / p-Si (100) $\rho_r \geq$ 10−20 Ω cm
r-FLA 68.7 J cm^{-2}	**4.2**	A4925 $Ge_{1-x}Sn_x$ after r-FLA 68.7 J cm^{-2}
r-FLA 76.6 J cm^{-2}	**4.2**	A4925 $Ge_{1-x}Sn_x$ after r-FLA 76.6 J cm^{-2}
r-FLA 84.8 J cm^{-2}	**4.2**	A4925 $Ge_{1-x}Sn_x$ after r-FLA 84.8 J cm^{-2}
A4930 $Ge_{0.84}Sn_{0.16}$ as-grown	**4.2**	200 nm p-$Ge_{0.84}Sn_{0.16}$:B (1 x 10^{20} cm^{-3}), T_S = 170 °C, g_r = 0.124 nm s^{-1} , Φ_{Ge} = 4.4 x 10^{14} cm^{-2}s^{-1}, Φ_{Sn} = 7.2 x 10^{13} cm^{-2}s^{-1} / 500 nm i-Ge / 50 nm Si / p-Si (100) $\rho_r \geq$ 10−20 Ω cm
r-FLA 68.7 J cm^{-2}	**4.2**	A4930 $Ge_{1-x}Sn_x$ after r-FLA 68.7 J cm^{-2}
r-FLA 84.8 J cm^{-2}	**4.2**	A4930 $Ge_{1-x}Sn_x$ after r-FLA 84.8 J cm^{-2}
r-FLA 92.6 J cm^{-2}	**4.2**	A4930 $Ge_{1-x}Sn_x$ after r-FLA 92.6 J cm^{-2}

The growth parameters of the MBE samples in **Chapter 4** are summarized in Table 8.1 - 1. The given material composition was measured by XRD or RBS. The sample list contains the fabrication parameters of the samples used in the allocated chapters. The given substrate temperature T_S can be lower than the actual growth

temperature on the sample surface since growth temperature is influenced by the heating power of the substrate and the radiation of the Ge and Sn effusion cells. The radiation of the effusion cells increased T_S for about 30 K during the growth of 200 nm $Ge_{1-x}Sn_x$ (measured by MIR-camera) [93]. In order to reduce the temperature rise, the power of the substrate heater was set to 0 W during the $Ge_{1-x}Sn_x$ growth. Therefore, the given T_S should be considered as relative values.

8.2 Extended RBS information

The RBS-R spectra in Fig. 8.2 - 1 show the movement of the peak and dip in the Sn spectra to lower energies of the backscattered He^+ with increasing E_d. The energy loss of the He^+ in the spectra is related to the mass of the target atomic nucleus in the investigated crystal and its depth, as mathematically shown in Eq. 8.2 - 1 for a detector angle of 170°.

$$E_1 \approx \left(\frac{m_2 - m_1}{m_2 + m_1}\right)^2 \left[E_0 - \int_0^{d_1}\left(\frac{dE}{dz}\right)dz\right] - \int_0^{d_2}\left(\frac{dE}{dz}\right)dz \qquad \text{Eq. 8.2 - 1}$$

Where E_1 is the detected He^+ energy. m_2 is the mass of the targeted atomic nucleus, e.g., Sn or Ge. m_1 is the mass of He^+. E_0 is the energy loss due to the interaction of He^+ with the targeted atom nucleus. $\int_0^{d_1}\left(\frac{dE}{dz}\right)dz$ describes the energy loss within the targeted layer until He^+ reaches the scattering atom, and $\int_0^{d_2}\left(\frac{dE}{dz}\right)dz$ is the energy loss within the targeted layer until He^+ leaves the crystal after the scattering event. Both integrals are related to the interaction of He^+ with the electrons and can be called electron loss.

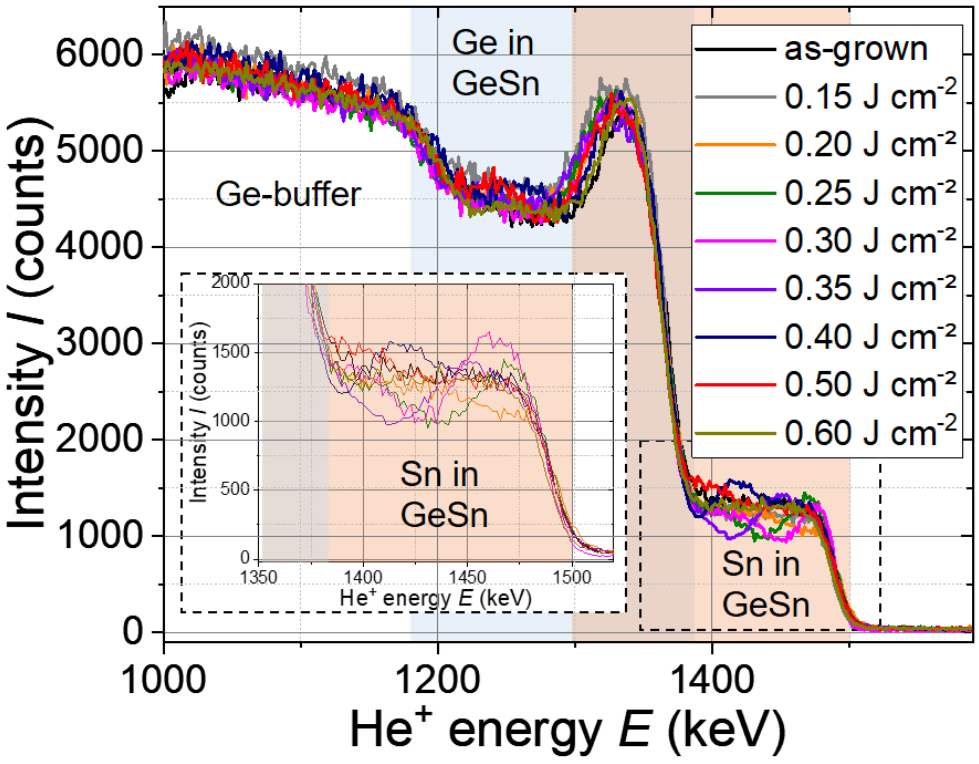

Fig. 8.2 - 1: RBS-R spectra of the $Ge_{0.89}Sn_{0.11}$ in the as-grown state and after PLA with E_d between 0.15 and 0.6 J cm^{-2}. The inset shows the enlarged Sn fraction of the $Ge_{1-x}Sn_x$ layer. The background colors are related to the signal of the backscattered He^+ from Sn (orange) in $Ge_{1-x}Sn_x$, Ge (blue) in $Ge_{1-x}Sn_x$, and Ge (white) of the Ge-buffer.

8.3 Extended TEM analysis for section 4.1.2

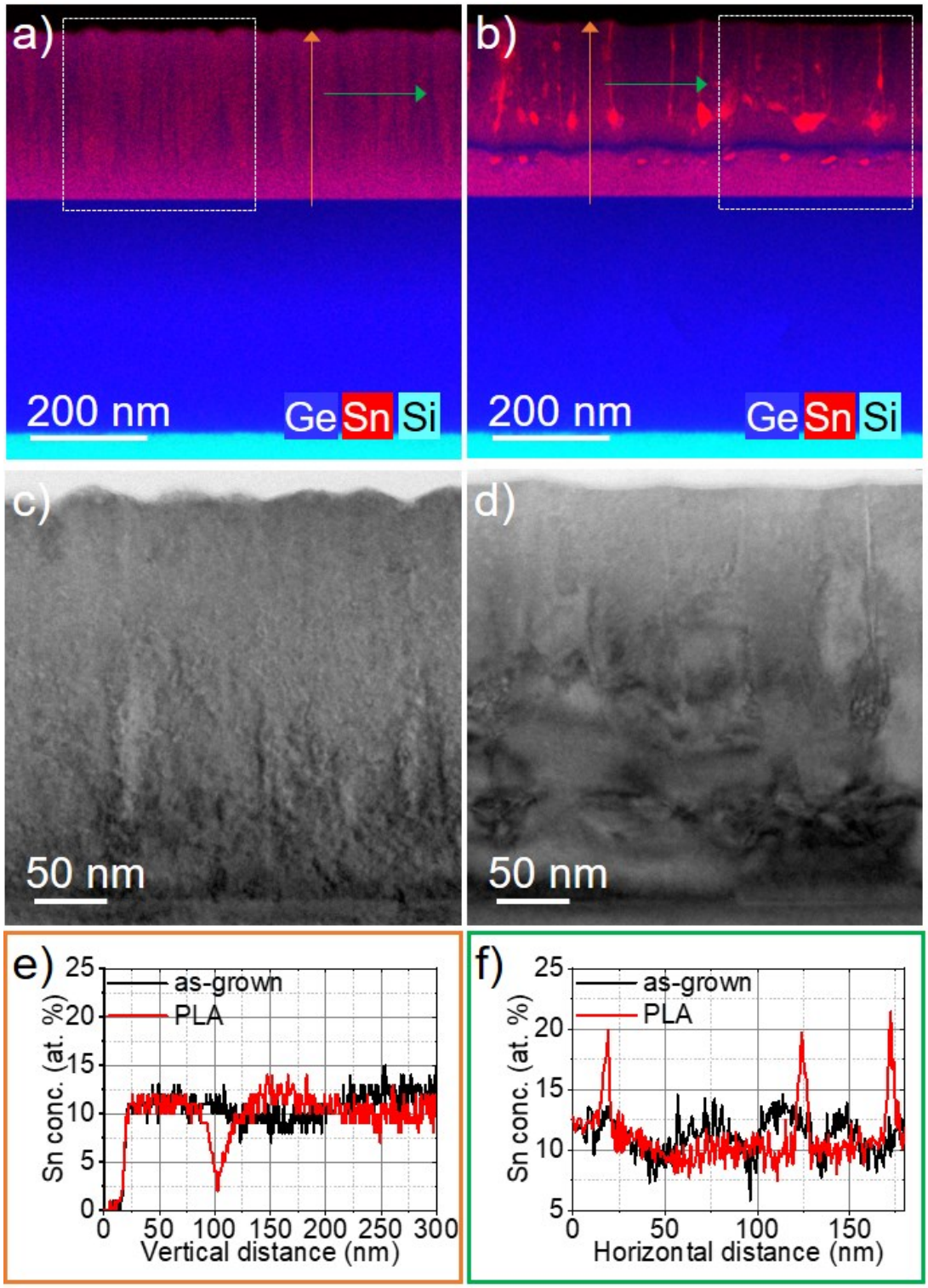

Fig. 8.3 - 1: Cross-sectional TEM-based analysis of the $Ge_{0.89}Sn_{0.11}$ as-grown sample (a), c), and e)), and after PLA treatment with an energy density of 0.5 J cm^{-2} (b), d), and f)). Panels a) and b) show representative superimposed Ge (blue), Sn (red), and Si (cyan) EDXS-based element distributions, while c) and d) present the bright-field TEM images of the regions marked with white-dashed squares in a) and b), respectively. The diagrams in e) and f) depict the vertical and horizontal line scans, indicated in a) and b) with orange and green arrows, respectively.

In order to record the TEM images in Fig. 4.1 - 3 and Fig. 8.3 - 1, the TEM specimen was oriented in Si $[1\bar{1}0]$ zone axis geometry relative to the electron beam. Fig. 8.3 - 1 a) and b) show superimposed Si, Ge, and Sn element distribution maps obtained from the upper part of the layer stack. The general setup matches the schematic presented in Fig. 4.1 - 1 a) and c). Fig. 8.3 - 1 c) and d) show enlarged bright-field TEM images recorded from the areas marked with the white-dashed squares in Fig. 8.3 - 1 a) and b), respectively. After PLA, a defect-rich zone with a thickness of about 200 nm can be obtained above the GeSn/Ge-buffer interface. However, close to the $Ge_{1-x}Sn_x$ surface, a significantly reduced defect concentration and a smoother sample surface are visible. The vertical line scan in Fig. 8.3 - 1 e) shows a sharp dip in the Sn profile of the PLA-treated sample. Unfortunately, the small dimension and wavy profile make it difficult to estimate the chemical composition since in-plane superposition effects and the dimension of the stimulation bulb can lead to uncertainties. The horizontal line scan analyses, presented in Fig. 8.3 - 1 f), confirm that the columnar structure is related to a slightly varying Sn concentration.

8.4 Strain calculation based on (224) RSM

The reciprocal peak position of each layers (224) reflection can be obtained from (224) XRD-RSM by a fit of the reflection in Rigaku SmartLab (Studio II) software with a Gaussian peak fit. The data extraction procedure is exemplary shown in Fig. 8.4 - 1 on $Ge_{0.89}Sn_{0.11}$ after PLA with E_d = 0.6 J cm^{-2}, as discussed in **section 4.1.3**. The reciprocal lattice parameter q_z is oriented parallel to the growth direction in [001]. On the other hand, q_x is oriented in [110] or, in other words, between two crystal axes that form the plane parallel to the layer surface. q_x and q_z are the directional components of the reciprocal scattering vector Q.

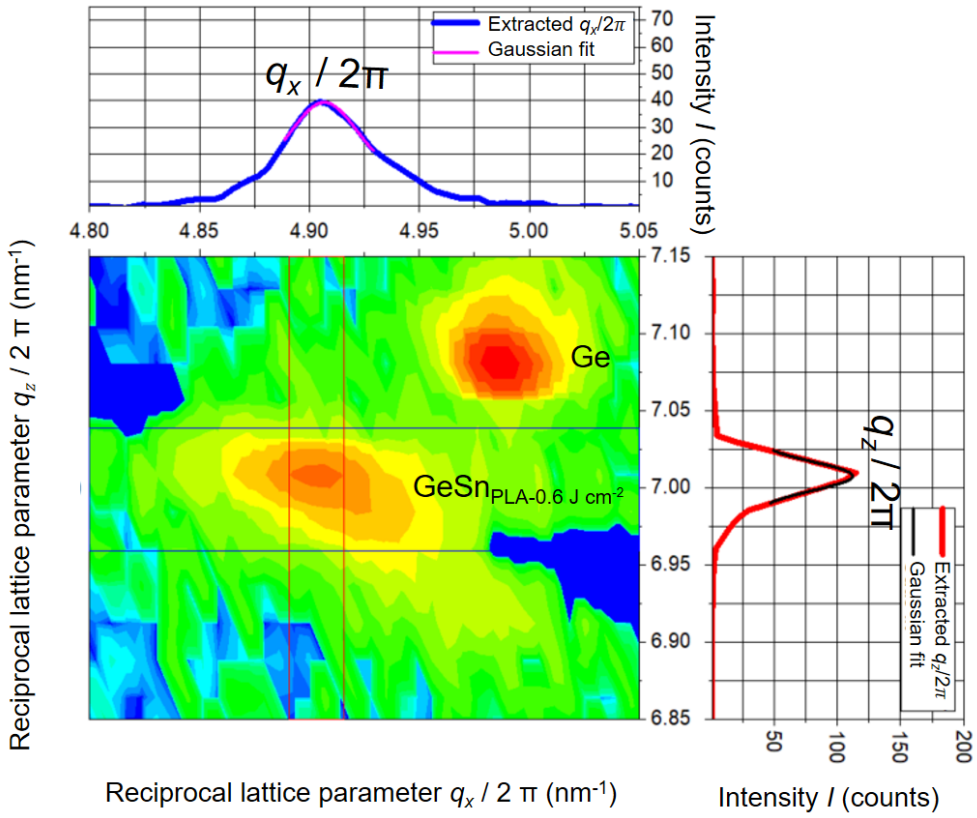

Fig. 8.4 - 1: Fitting procedure of the reciprocal (224) in-plane q_x and out-of-plane q_z lattice parameter on the example of the GeSn$_{PLA-0.6\ J\ cm^{-2}}$. For both cases, the adjusted R^2 was above 98%.

Afterward, the reciprocal lattice parameters q_x and q_z can be converted into real space in-plane a_{II} and out-of-plane $a_{\perp}$ lattice parameters by using Eq. 8.4 - 1 and Eq. 8.4 - 2, respectively.

$$a_{\perp} = 4\,\frac{2\pi}{q_z} \qquad \text{Eq. 8.4 - 1}$$

$$a_{II} = \sqrt{8}\,\frac{2\pi}{q_x} \qquad \text{Eq. 8.4 - 2}$$

In the next step, the strain-relaxed lattice parameter a_0 is calculated by Eq. 8.4 - 3. For this, it is necessary to approximate the elastic constants C_{11} and C_{12} of the alloy. Previous publications have pointed out that the linear combination using Vegard's law for C_{11} and C_{12} in Eq. 8.4 - 4 and Eq. 8.4 - 5 causes an error of about 2-3% for $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys [77]. For this step, an alloy composition has to be assumed as a starting point since C_{11} and C_{12} depend on the alloy composition.

$$a_0 = \frac{a_\perp + \frac{2C_{12}}{C_{11}} a_{II}}{1 + \frac{2C_{12}}{C_{11}}} \qquad \text{Eq. 8.4 - 3}$$

$$C_{11}\left(Si_{1-x-y}Ge_ySn_x\right) = (1-x-y)\, C_{11,Si} + x\, C_{11,Sn} + y\, C_{11,Ge} \qquad \text{Eq. 8.4 - 4}$$

$$C_{12}\left(Si_{1-x-y}Ge_ySn_x\right) = (1-x-y)\, C_{12,Si} + x\, C_{12,Sn} + y\, C_{12,Ge} \qquad \text{Eq. 8.4 - 5}$$

Afterward, a more accurate alloy composition can be calculated using Vegard's law (see Eq. 2.3 - 1). Several iterations of this procedure will result in stable alloy composition-dependent C_{11}, C_{12}, and a_0 values. This approach works well for binary systems, but for the ternary $Si_{1-x-y}Ge_ySn_x$ alloy, the concentration of one component must be fixed. Finally, the in-plane strain $\varepsilon_{II,XRD}$ can be calculated with the knowledge of a_0 by Eq. 8.4 - 6 and the assumption that the difference between the measured a_{II} and the composition-dependent a_0 is caused by elastic strain.

$$\varepsilon_{II,XRD} = \frac{(a_{II} - a_0)}{a_0} \qquad \text{Eq. 8.4 - 6}$$

8.5 Strain calculation by μ-Raman

Strain can be calculated with μ-Raman based on the frequency dependence of the main vibrational modes for a layer with a known chemical composition [251]. The difference between the measured Ge-Ge phonon peak position $\omega_{p,measurement}$ of the $Ge_{1-x}Sn_x$ alloy, and the peak position of pure Ge $\omega_{p,Ge}$ is caused by the composition of the $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ alloy $\Delta\omega_{p,alloy}$, and the strain $\Delta\omega_{p,strain}$. This can be expressed by Eq. 8.5 - 1. In the example of $Ge_{1-x}Sn_x$: $\Delta\omega_{alloy}$ is influenced by (i) the different mass $\Delta\omega_{p,mass}$ of the Ge and Sn atoms in the alloy, and (ii) the change of bond length $\Delta\omega_{p,bond}$ between Ge atoms due to alloying with Sn. Since the strain, mass difference, and bond length depend linearly on the concentration of Sn, the value for $\Delta\omega_{p,alloy}$ can be calculated with Eq. 8.5 - 2 by using the disorder parameter b_d. With b_d = -83.11 [201], the Raman shift in a fully relaxed $Ge_{1-x}Sn_x$ with a low concentration of Sn can be calculated. The shift due to the in-plane strain $\varepsilon_{II,Raman}$ can be calculated using Eq. 8.5 - 3 and Eq. 8.5 - 4. The strain coefficient b_ε = -374.53 [201] was used. One example is shown in Table 8.5 - 1.

$$\Delta\omega_p = \omega_{p,measurement} - \omega_{p,Ge-Ge} = \Delta\omega_{p,alloy} + \Delta\omega_{p,strain} \quad \text{Eq. 8.5 - 1}$$

$$\Delta\omega_{p,alloy} = \Delta\omega_{p,mass} + \Delta\omega_{p,bond} = b_d * c_{Sn} \quad \text{Eq. 8.5 - 2}$$

$$\Delta\omega_{p,strain} = \omega_{p,measurement} - \Delta\omega_{p,alloy} \quad \text{Eq. 8.5 - 3}$$

$$\varepsilon_{II,Raman} = \frac{\Delta\omega_{p,strain}}{b_\varepsilon} \quad \text{Eq. 8.5 - 4}$$

Table 8.5 - 1: In-plane strain $\varepsilon_{II,Raman}$ calculation results used for Fig. 4.2 - 3 b) in **section 4.2.2** of $Ge_{1-x}Sn_x$ (x ≈ 9, 12 and 16 at.%) by using the Ge-Ge phonon mode. $\omega_{p,measurement}$ is obtained by Lorentzian fitting of the spectra presented in Fig. 4.2 - 3 a). The Sn concentration $c_{Sn,RBS}$ is determined by RBS-R and SIMNRA simulations.

Sample		$\omega_{p,measurement}$ (cm^{-1})	$\Delta\omega_{p,alloy}$ (cm^{-1})	$c_{Sn,RBS}$ (at.%)	$\varepsilon_{II,Raman}$	T (°C)
$Ge_{0.91}Sn_{0.09}$	as-grown	299.12	-7.646	9.2 ± 0.1	-0.0167	-
	84.8 J cm^{-2}	299.10	-7.646	9.2 ± 0.1	-0.0167	470
	92.6 J cm^{-2}	299.12	-7.646	9.2 ± 0.1	-0.0167	506
$Ge_{0.88}Sn_{0.12}$	as-grown	295.75	-10.056	12.1 ± 0.1	-0.0142	-
	76.6 J cm^{-2}	295.85	-9.724	11.7 ± 0.1	-0.0135	428
	84.8 J cm^{-2}	294.39	-10.721	12.9 ± 0.1	-0.0123	470
$Ge_{0.84}Sn_{0.16}$	as-grown	284.79	-14.378	17.3 ± 0.1	0.0035	-
	84.8 J cm^{-2}	284.79	-13.962	17.0 ± 0.1	0.0042	470
	92.6 J cm^{-2}	284.35	-14.295	17.2 ± 0.1	0.0049	506

8.6 Analysis of Hall-effect measurements

Hall-effect measurements in van-der-Pauw configuration is a four-probe method to determine the resistivity ρ_r, sheet carrier concentration (n_{e^-} for electrons and n_{h^+} for holes), and the Hall-voltage V_H for a known layer thickness d. During the measurement, a current I_H is applied between two of the four contacts and the Hall-voltage V_H is measured depending on the applied magnetic flux density B on the other two contacts. For Hall-effect measurements in van-der-Pauw configuration, it is necessary to meet the following requirements in the sample preparation: i) the contacts must be small compared to the sample dimension, ii) the contacts are placed on the periphery of the sample, and iii) the investigated layer has a uniform thickness [301]. Based on Eq. 8.6 - 1 V_H depends on the I_H, B, d, sheet carrier concentration n_{e^-} for electrons or n_{h^+} for holes and the elementary charge q. I_H, B, d, and q are known or applied parameters, and V_H can be extracted.

$$V_H = -\left(\frac{1}{n_{e-/h+}\ q}\right)\frac{I_H B}{d} \qquad \text{Eq. 8.6 - 1}$$

The used measurement setups (see **section 3.9**) perform the following measurement sequence: a) applying the selected current I_H between two neighbor contacts, e.g., 1 and 2, and measuring the V_H between the other two contacts, e.g., 3 and 4*[7]. This procedure is performed for all 8 possible configurations in forward and backward directions without applying the magnetic field B. Based on the extracted V_H and the knowledge of the layer thickness d and tabulated form factor f_A and f_B, the resistivity ρ_{rA} and ρ_{rB} are extracted by Eq. 8.6 - 2 and Eq. 8.6 - 3.

$$\rho_{rA} = \frac{\pi}{\ln 2} f_A\, d \left(\frac{(V_{H1} - V_{H2}) + (V_{H3} - V_{H4})}{4 I_H}\right) \qquad \text{Eq. 8.6 - 2}$$

$$\rho_{rB} = \frac{\pi}{\ln 2} f_B\, d \left(\frac{(V_{H5} - V_{H6}) + (V_{H7} - V_{H8})}{4 I_H}\right) \qquad \text{Eq. 8.6 - 3}$$

Eq. 8.6 - 2 and Eq. 8.6 - 3 can be simplified with the help of Eq. 8.6 - 4 to Eq. 8.6 - 5 and Eq. 8.6 - 6. Afterward, ρ_r can be determined by the average value of ρ_{rA} and ρ_{rB} (see Eq. 8.6 - 7).

$$R_H = \frac{V_H}{I_H} \qquad \text{Eq. 8.6 - 4}$$

$$\rho_{rA} = \frac{\pi}{\ln 2} f_A\, d \left(\frac{(R_{12,34}) + (R_{23,41})}{2}\right) \qquad \text{Eq. 8.6 - 5}$$

$$\rho_{rB} = \frac{\pi}{\ln 2} f_B\, d \left(\frac{(R_{34,12}) + (R_{41,23})}{2}\right) \qquad \text{Eq. 8.6 - 6}$$

$$\rho_r = \frac{\rho_{rA} + \rho_{rB}}{2} \qquad \text{Eq. 8.6 - 7}$$

[7] The four contacts on the square-shaped samples are named clockwise from one to four, with “1” at 10 pm, “2” at 2 pm, “3” at 4 pm, and “4” at 8 pm.

b) In the next step, the Hall-coefficient A_H is determined. For this, a homogeneous magnetic field perpendicular to the layer is applied, and R_H is measured between the diagonal contacts. This means I_H is applied, e.g., between contact 1 and 3, and V_H is measured between contact 2 and 4. Here, R_H depends on the applied B since the active carriers are deflected by the B-dependent Lorenz force. The same measurement is also performed without B. The difference between $R_{H13.24}$ with and without application B is used to determine the Hall-coefficient A_H by Eq. 8.6 - 8. Now n_{e-} for electrons and n_{h+} for holes can be calculated by Eq. 8.6 - 9. For measurements with a variable B, $n_{e-/h+}$ can be extracted by the slope coefficient k of the R_H versus B plot by Eq. 8.6 - 10.

$$A_H = \frac{d}{B} \Delta R_{\mathrm{H13.24}} \qquad \text{Eq. 8.6 - 8}$$

$$n_{e-/h+} = \frac{1}{A_H\, q} \qquad \text{Eq. 8.6 - 9}$$

$$n_{e-/h+} = \frac{1}{q \cdot d \cdot k} \qquad \text{Eq. 8.6 - 10}$$

c) Finally, the determined n_{e-} or n_{h+}, q, and ρ_r can be used to calculate the carrier mobility of electrons μ_{e-} or of holes μ_{h+} by equation Eq. 8.6 - 11.

$$\mu_{e-/h+} = \frac{1}{n_{e-/h+} \cdot q \cdot \rho_r} \qquad \text{Eq. 8.6 - 11}$$

8.7 VEPFit and ATSUP simulations

The layer stack is a basic parameter for accurate VEPFit and ATSUP calculations performed in **section 4.1.4** for Table 4.1 - 5 and Fig. 4.1 - 10. The estimation of important parameters will be explained in this section.

i) Assumed layer stacks for simulations

The density ρ of the $Ge_{0.89}Sn_{0.11}$ and $Ge_{1-x}Sn_x$ layers after PLA, used in Table 4.1 - 5, was calculated by Eq. 8.7 - 1, Eq. 8.7 - 2 and Eq. 8.7 - 3.

$$\rho = \frac{m_{GeSn}}{V} \quad \text{Eq. 8.7 - 1}$$

$$m_{GeSn} = m_{Ge}\, N_{Ge} + m_{Sn}\, N_{Sn} \quad \text{Eq. 8.7 - 2}$$

$$V = a_{II}\, a_{II}\, a_{\perp} \quad \text{Eq. 8.7 - 3}$$

Within these equations, m_{GeSn} belongs to the mass of the $Ge_{1-x}Sn_x$ alloy diamond unit cell with their presented composition c_{Ge} and c_{Sn} in Table 8.7 - 1. N is the amount of Ge or Sn atoms in the unit cell. The volume V is calculated using the in-plane a_{II} and out-of-plane $a_{\perp}$ lattice parameters determined by (004) HR-XRD and $(\bar{2}\bar{2}4)$ RSM in ref. [128]. The results are summarized in Table 8.7 - 1 and are used for ATSUP and VEPFit code simulations.

Table 8.7 - 1: Overview of the expected layer stack based on TEM (see Fig. 4.1 - 3 and Fig. 8.3 - 1), XRD (Table 4.1 - 2) and RBS (Fig. 8.2 - 1) results. For Ge and Si literature densities were used from Table 2.1 - 1. c_{Ge} and c_{Sn} describe the chemical composition of the layer.

Sample	Layer	Layer thickness d (nm)	c_{Ge} (at.%)	c_{Sn} (at.%)	Density ρ (g cm^{-3})
$Ge_{0.89}Sn_{0.11}$ as-grown	$Ge_{0.89}Sn_{0.11}$	290 ± 8	89 ± 0.5	11 ± 0.5	5.14
PLA 0.3 J cm^{-2}	$Ge_{1-x}Sn_x$ PLA	100 ± 10	90	10	5.11
	Sn-depleted Interface $Ge_{1-x}Sn_x$	15	>92	<8	-
	$Ge_{0.89}Sn_{0.11}$	180 ± 10	90 ± 0.5	10 ± 0.5	5.16
PLA 0.4 J cm^{-2}	$Ge_{1-x}Sn_x$ PLA	140 ± 10	90.4 ± 0.5	9.6 ± 0.5	5.11
	Sn-depleted Interface $Ge_{1-x}Sn_x$	15	>92	<8	-
	$Ge_{0.89}Sn_{0.11}$	135 ± 10	90 ± 0.5	10 ± 0.5	5.16
PLA 0.5 J cm^{-2}	$Ge_{1-x}Sn_x$ PLA	195 ± 8	91.1 ± 0.5	8.9 ± 0.5	5.10
	Sn-depleted Interface $Ge_{1-x}Sn_x$	15	>92	<8	-
	$Ge_{0.89}Sn_{0.11}$	80 ± 8	90 ± 0.5	10 ± 0.5	5.16

ii) Calculation of defect concentration based on positron diffusion length

Assuming that the films mostly contain one major defect type (as indicated by PALS), the vacancy concentration c_V can be calculated by Eq. 8.7 - 4 [302]:

$$c_V = \frac{1}{\nu_V \tau_B}\left(\frac{L_{+,B}^2}{L_+^2} - 1\right), \qquad \text{Eq. 8.7 - 4}$$

where ν_V is a specific positron trapping rate (trapping coefficient), τ_B and $L_{+,B}$ are the positron bulk lifetime and the positron diffusion length in a defect-free material. $L_{+,B}$ can be calculated by Eq. 8.7 - 5

$$L_{+,B} = \sqrt{D_+ \tau_B}, \qquad \text{Eq. 8.7 - 5}$$

where D_+ is the room temperature positron diffusion coefficient.

According to our ATSUP calculations and existing literature, the bulk lifetime of Ge should be close to $\tau_B \approx 228$ ps [303]. The values of D_+ are often difficult to find in literature. For semiconductors, the diffusion coefficient is typically in the range D_+ = 1-2 cm^2 s^{-1} [304]. On the other hand, by using Eq. 8.7 - 5 and D_+ = 0.54 cm^2 s^{-1}, we obtain $L_{+,B} \approx 111$ nm, which is equal to the value calculated for our Ge reference sample. D_+ = 0.7 cm^2 s^{-1}, which is close to our case, was proposed in [305]. The specific positron trapping rate in Si is $\nu_V \approx 1 \times 10^{15}$ s^{-1} and can safely be utilized for Ge, too. The calculated defect density c_V using the above considerations is presented in Table 4.1 - 5.

iii) ATSUP calculations

Theoretical calculations of positron lifetimes for different possible defect configurations were performed employing the so-called atomic superposition technique ATSUP [219]. The electron-positron correlations were treated according to the gradient-correction (GC) scheme with the correction factor α = 0.22 proposed in ref. [306]. For calculations, we assume that the vacancy clusters are formed by removing the Ge atom, followed by nearest-neighbors and next-nearest-neighbors. The calculated positron lifetime using the GC scheme and the corresponding binding energy E_b for bulk, mono- and bi-vacancy of Ge are shown in Table 8.7 - 2. Both lifetime and binding energy increase with the vacancy size, which is expected for $Ge_{0.89}Sn_{0.11}$, too.

Table 8.7 - 2: ATSUP calculated positron bulk lifetime τ_B and binding energy E_b for the annihilation states of defect-free bulk Ge (Ge bulk), Ge with a single-vacancy on a Ge substitutional lattice site (V_{Ge}) and a double vacancy cluster in Ge (V_{2Ge}).

Annihilation state	τ_B (ps)	E_b (eV)
Ge bulk	227.60	-
V_{Ge}	258.13	0.27
V_{2Ge}	325.89	0.91

The τ_B and τ_{VGe} increase with increasing a_{II} according to the ATSUP simulation results summarized in Table 8.7 - 3.

Table 8.7 - 3: ATSUP calculated positron bulk lifetime τ_B and positron single-vacancy lifetime τ_{VGe} for different in-plane lattice parameters a_{II} corresponding to the as-grown and PLA-treated samples (taken from Table 4.1 - 2).

Sample	a_{II} (Å)	τ_B (ps)	τ_{VGe} (ps)
$GeSn_{as\text{-}grown}$	5.6928	231.68	265.04
$GeSn_{PLA\text{-}0.4\ J\ cm^{-2}}$	5.7361	233.29	265.18
$GeSn_{PLA\text{-}0.5\ J\ cm^{-2}}$	5.7478	233.41	265.28
$GeSn_{PLA\text{-}0.6\ J\ cm^{-2}}$	5.7536	233.67	265.50

As shown in Table 8.7 - 4, the bulk lifetime $Ge_{0.9}Sn_{0.1}$ τ_B remains almost constant when Ge is replaced by Sn. However, vacancies on Ge lattice sites in the neighborhood of Sn increase τ_{VGe} significantly.

Table 8.7 - 4: ATSUP calculated positron bulk lifetimes in $Ge_{0.9}Sn_{0.1}$ for the increasing number of Sn nearest-neighbor atoms decorating a Ge atom τ_B and germanium vacancy τ_{VGe}.

No. of Sn-atoms	τ_B (ps)	τ_{VGe} (ps)
0 (pure Ge)	230.44	260.50
1	230.26	252.68
2	230.11	245.17
3	229.98	238.93
4	229.88	234.63

8.8 Strain relaxation of $Ge_{0.89}Sn_{0.11}$ for section 4.1.5

The presented µ-Raman result in Fig. 8.8 - 1 shows the $Ge_{0.89}Sn_{0.11}$ sample of the second sample series in the as-grown state and after PLA with E_d = 0.5 J cm^{-2}. The peak position of the as-grown sample is 296.2 ± 0.1 cm^{-1}, which perfectly coincides with the as-grown state in the first fabrication series (see Table 4.1 - 3). After PLA with E_d = 0.5 J cm^{-2}, the Ge-Ge mode shifts clearly to lower wavenumbers and is located at 289.5 ± 0.1. The observed shift confirms the strain relaxation before the second MBE growth of $Ge_{0.89}Sn_{0.11}$ on the strain-relaxed PLA-treated $Ge_{1-x}Sn_x$-VS.

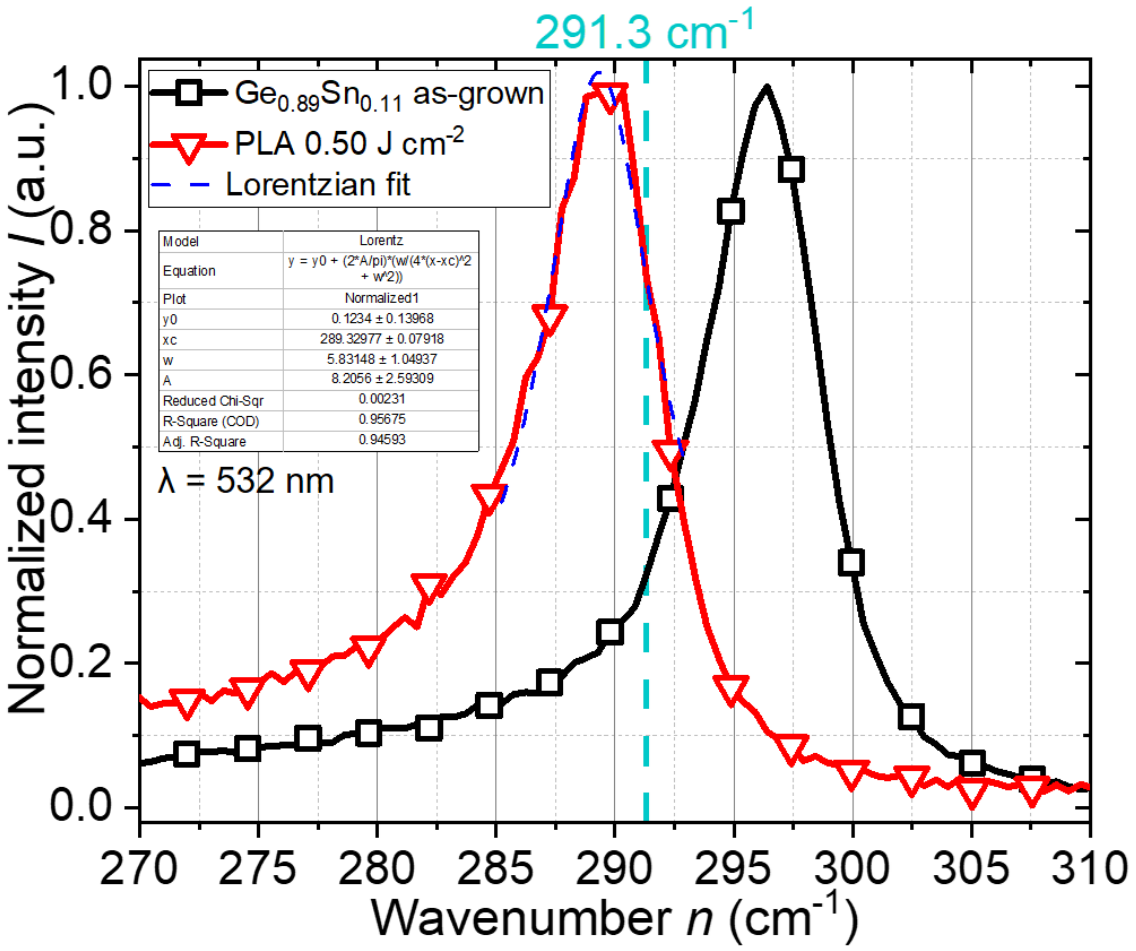

Fig. 8.8 - 1: Normalized µ-Raman spectra for the Ge-Ge phonon mode of the $Ge_{0.89}Sn_{0.11}$ in the as-grown state and after PLA with E_d = 0.50 J cm^{-2}. The vertical light blue dashed line highlights the theoretically expected peak position of strain-relaxed $Ge_{0.89}Sn_{0.11}$ at 291.3 cm^{-1}. The peak position of each spectrum was fitted with the Lorentzian peak function, as exemplarily shown for $Ge_{1-x}Sn_x$ after PLA with E_d = 0.50 J cm^{-2}.

8.9 COMSOL simulation of FLA temperature

COMSOL Multiphysics 6 [175] is a simulation software for physical processes and was used to approximate the occurring temperature in the layer stack due to the FLA process. The one-dimensional continuum simulation was performed in collaboration with Dr. Lars Rebohle, and Thomas Schuman provided the FLA calibration data.

The sample temperature during the FLA process depends on many parameters, as explained in **section 2.4.2.** The average absorption of light $\overline{A_\lambda}$ within the sample was approximated by the following procedure: 1) The spectra S_λ of the selected FLA pulse length were measured in previous calibration experiments [307]. 2) The reflection R_λ and transmission T_λ of each sample type was measured with Schmadzu SolidSpec-3700 DUV spectrometer equipped with tungsten (W) and deuterium (D) lamps and lead sulfide (PbS, λ = 1650-3300 nm), indium gallium arsenide (InGaAs, λ = 870-1650 nm) and silicon photomultiplier tube (PMT λ = 200-870 nm) detectors. Aluminum reference mirrors were used as a reflectance reference. Next, the spectra were converted from wavelength into energy, normalized to 100%, and folded using Eq. 8.9 - 1.

$$\overline{R_\lambda} = \frac{\int R_\lambda(E) S_\lambda \, dE}{\int S_\lambda \, dE} \qquad \text{Eq. 8.9 - 1}$$

Finally, $\overline{A_\lambda}$ was calculated by Eq. 8.9 - 2.

$$\overline{A_\lambda} = 1 - \overline{R_\lambda} \qquad \text{Eq. 8.9 - 2}$$

The used layer stacks for r-FLA simulations are simplified since:

i) the layer parameters of the complex $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys are not well known yet,

ii) the thin layers have a negligible influence on the thermal conduction compared to thick Si substrate, and

iii) the absorption is mainly located in the first micrometers of the Si substrate.

Therefore, the $Si_{1-x-y}Ge_ySn_x$ and $Ge_{1-x}Sn_x$ with high Ge content are replaced by Ge, and the Si-based alloys are replaced by Si. Hence, we used the following layer stacks from top to bottom: 750 nm Ge on 525 µm Si substrate (unpolished back side) for **section 4.2** and 27 nm Si, on 21 nm SiO_2 on 750 µm Si substrate (polished backside) for **section 5.1**. The material-specific data of the heat capacity C_p(T), thermal conductivity K(T), and density ρ of Si, Ge, and SiO_2 were taken from the COMSOL database and ref. [308-310]. The energy density E_d and the pre-heating temperature were measured as explained in **section 3.4**. For r-FLA simulations, a mesh with an asymmetric geometric distribution of 3990 (Ge on 525 µm Si) or 5890 (SOI on 775 µm Si) elements with a

pre-defined element ratio of 2000 is used. An exemplary result for 3 different energy densities E_d can be obtained in Fig. 8.9 - 1.

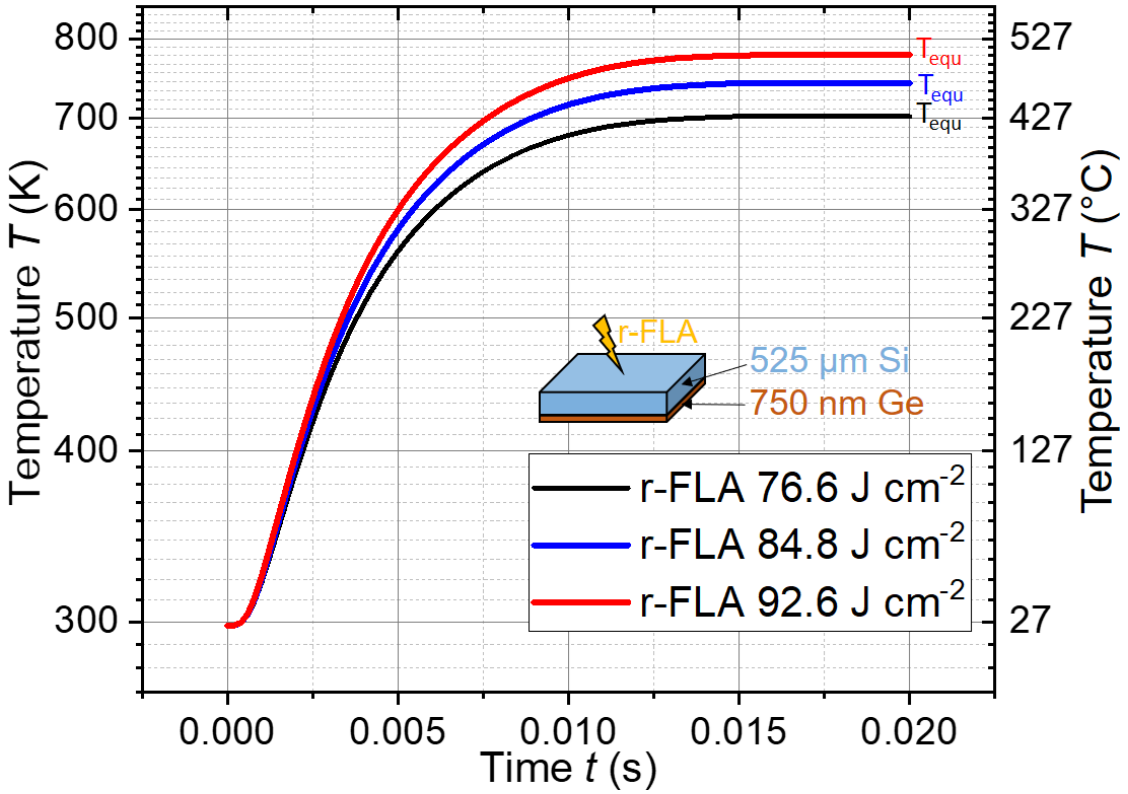

Fig. 8.9 - 1: Exemplary temperature-time simulation at the Ge surface during r-FLA with a 3.2 ms pulse length and E_d = 76.6, 84.8 and 92.6 J cm^{-2}. The calculated quasi-equilibrium temperatures T_{equ} are 429 °C for 76.6 J cm^{-2}, 470 °C for 84.8 J cm^{-2}, and 506 °C for 76.6 J cm^{-2}.

8.10 ECV measurement setup

The ECV measurements were performed by Horst Windgassen and Michail Michailow at RWTH Aachen as project partners. The experimental results were analyzed in collaboration. ECV is based on the formation of a depletion zone at the interface between the GeSn-semiconductor and the used electrolyte. Under reverse voltage between the semiconductor and the electrolyte, a depletion zone is formed at the contact interface. The capacitance of the Schottky-like contact is used to determine the carrier concentration using a conventional capacitance-voltage approach. The electrochemical etching works via recombination of h^+ formed in electrolyte with valence e^- from the semiconductor. By removing the valence electrons, the elemental bonds break up, and the atom is dissolved in the electrolyte. In the case of the p-type semiconductor, the e^- are generated by illuminating the sample with light. A schematic of the measurement setup is shown in Fig. 8.10 - 1. Ammonium bifluriede NH_4HF_2 (0.1 molar) is used as an electrolyte. The electrolyte wets an area of 0.9 mm², which is defined by the sealing ring diameter. The depletion zone causes in a capacitance, which is measured and used to calculate the active carrier concentration. Afterward, the GeSn layer is thinned down with an electrochemical etching process. The etching and single measurements are performed with steps of about 10 nm.

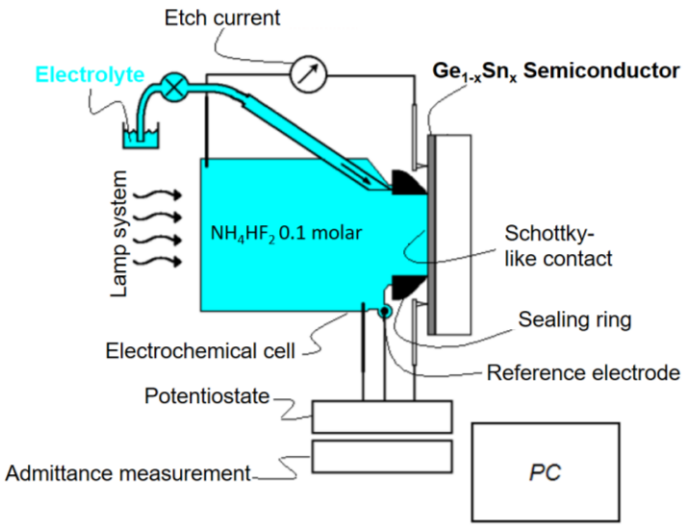

Fig. 8.10 - 1: Schematic of the ECV measurement setup of the Wafer Profiler CVP21 from the company WEP.

8.11 Datasheet of the SOI wafers

The final aim of this thesis is the fabrication of lateral transistors with $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ alloys. Therefore, it appears to be suitable to use isolated substrates, like the SOI platform, as a starting material. SOI substrates can be produced in a large scale via “separation by implanted oxygen” (SIMOX) [311], “bond and etch back SOI” (BESOI) [4], or “smart cut” [312] techniques. Si on insulator (SOI) wafers have an Si layer on an insulating material. For ICs, the main isolation material is SiO_2. SOI comes with some advantages for electronic devices, like lower power consumption, faster switching speed, lower fabrication complexity compared to the bulk planar technique, and a general decoupling of the device performance from the bulk wafer. The known parameters of the used SOI wafers in **sections 5.1.2 - 5.1.4** and **5.2** are summarized in Table 8.11 - 1. Unfortunately, the SOI technique can suffer from a localized self-heating effect during device operation because of the limited heat dissipation through the underlying insulator [282]. Therefore, the operation voltage should be restricted, especially when metastable materials like $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ are involved [3, 282].

Table 8.11 - 1: Datasheet of the two different SOI wafer types A) and B). Data for wafer A) is directly obtained from the delivery datasheet of the company Shin-Etsu Handotai. Data for wafer B) is measured by variable angle spectroscopic ellipsometry (VASE) measurements at GlobalFoundries Dresden.

Wafer type			A	B
Used in chapter/section			**5.2** and **6**	**5.1.2 - 5.1.4**
Diameter			300 mm	300 mm
SOI layer	Growth method		MCZ	-
	Conductivity (type)		p-type	-
	Resistivity		9 - 15 ohm cm	-
	Plane orientation	Target	(100)	(100)
		tolerance	±1.0°	-
	Notch or Flat & orientation		Notch	-
		Target	(01T)	-
		tolerance	±1.0°	-
	Oi User		7.0 - 10.0 ppma ASTM (80)	-
	SOI thickness	Target	20 nm	12 nm
	Uniformity	Sec/definition	20 ±1 nm / all points	12 ± 0.1 nm
		Edge exclusion (EE)	3 mm	-
	Particle & surface		0.09 µm ≤ 50 pcs/wafer	-
			0.25 µm ≤ 25pcs/wafer	-
		Edge exclusion	3 mm	-

	Other inspection	Void	0 (Dia ≥ 0.5 (*1))	-
		Non-SOI edge	Max 2.5 mm	-
		Scratches	0 (*1)	-
		Roughness	Max 0.5 nm (*2)	-
BOX	BOX thickness	Target	100 nm	21 nm
	Uniformity	Spec/definition	100±5 nm avg of wafer	21 ± 0.16 nm
		Edge exclusion	3 mm	-
Nase Wafer	Crystal growth method		MCZ	-
	Conductivity (type)		p-type	-
	Dopant		Boron	-
	Resistivity		9-15 ohm cm	-
	Plane orientation	Target	(100)	-
		Tolerance	±1.0°	-
	Notch or Flat / orientation		Notch	-
		Target	(01T)	-
		Tolerance	±1.0°	-
	Oi User		11.0 – 13.2 ppma (ASTM80)	-
	Cs User		Max 0.2 ppma	-
	Beveling		SEMI std	-
	Substrate thickness	Target	775 µm	-
		Tolerance	775 ± 25 µm	750 µm
	Laser Mark		HLM on the rear-side T7+M12	-
Backside	Backside		Polished without Ox film	Polished without Ox film
Surface metal contamination level spec/metal			Max 1×10^{10} atoms cm^{-2} Fe, Ni, Cu, Cr, Zn, Ca, K, Na, Al	-
Warp –bf	Spec		Max 60 µm	-
	Edge exclusion		3 mm	-
Flatness	Edge exclusion		3 mm	-
	Equipment		E+	-
	GBIR		Max 1.0 µm	-
	GFLR		Max 1.0 µm	-
	Site Flatness	Spec	SFQR max 0.08 µm	-
		Cell/offset/partial	26 x 8 mm / (0,0) / active	-
Package (inner)			SEH std	-
Package (outer)			SEH std	-

8.12 Sample list of Chapter 5

The sample list in Table 8.12 - 1 summarizes the fabrication parameters of the used materials in **Chapter 5**. The implantation parameters were designed using SRIM [249] simulations. The FLA peak temperatures were calculated by the software "COMSOL Multiphysics 6" [175] under the assumption of a simplified layer stack (see **section 8.9**).

Table 8.12 - 1: Sample list of the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ samples presented in **Chapter 5**. The layer stack (top to bottom) contains known parameters about the layer thickness *d*, chemical composition, type of dopant, targeted implantation parameters like the implantation energy *E*, implantation fluence D_I, and the projected range R_p. The r-FLA annealing conditions consist of a pre-heating temperature from the top side, energy density E_d, and a flash length. The respective process temperatures *T* are given for each step. For the MBE growth process the substrate temperature T_S, growth rate g_r, the flux of the Ge source Φ_{Ge}, the flux of the Sn source Φ_{Sn}, and the resistivity ρ_r of the substrate are provided in addition to the PLA energy density E_d.

Sample name	Chapter/ section	Layer parameter from top to bottom and fabrication parameter obtained from the Implantation / MBE process log files
Ge:Sn	**5.1**	200 nm i-Ge:Sn (^{120}Sn implantation: E = 250 kV, $D_I = 4 \times 10^{16}$ cm^{-2}, ω = 7)
$Si_{0.28}Ge_{0.72}$ as-grown	**5.1.1**	600 nm i-$Si_{0.28}Ge_{0.72}$, p-Si (001)
$Si_{0.28}Ge_{0.72}$:Sn as-implanted	**5.1.1**	100 nm $Si_{0.28}Ge_{0.72}$:Sn:P (^{120}Sn implantation: E = 250 kV, $D_I = 1 \times 10^{16}$ cm^{-2}, $R_p \approx$ 100 nm, T < 100 °C, ω = 7°; P implantation: E = 80 kV, $D_I = 3 \times 10^{15}$ cm^{-2}, $R_p \approx$ 80nm, T < 100 °C, ω = 7°), ≈500 nm i-$Si_{0.28}Ge_{0.72}$, p-Si (001)
$Si_{0.278}Ge_{0.699}Sn_{0.023}$ r-FLA	**5.1.1**	100 nm $Si_{0.278}Ge_{0.699}Sn_{0.023}$, ≈500 nm i-$Si_{0.28}Ge_{0.72}$, p-Si (001) after r-FLA with pre-heating of 330 °C for 30 s and a 3.2 ms flash with E_d = 72.5 Jcm^{-2}
SiGe as-grown	**5.1.3**, **5.1.2**	15 nm $Si_{0.73}Ge_{0.27}$, SOI wafer B from **section 8.11**
SiGe:Sn as-implanted	**5.1.3**, **5.1.2**	8.6nm SiN_x, 15 nm $Si_{0.73}Ge_{0.27}$:Sn (^{120}Sn implantation: E = 26 kV, $D_I = 1.2 \times 10^{15}$ cm^{-2} (about 3% Sn) ω = 7°, $R_p \approx$ 16 nm, T < -100 °C), SOI wafer B from **section 8.11**
SiGeSn r-FLA 60 J cm^{-2} 3.2 ms	**5.1.3**, **5.1.2**	15 nm $Si_{0.73-0.5x}Ge_{0.27-0.5x}Sn_x$ after r-FLA with a peak pre-heating temperature of 570 °C, E_d = 60 J cm^{-2} and a flash length of 3.2 ms ($T \approx$ 730 °C), SOI wafer B from **section 8.11**
SiGeSn r-FLA 120 J cm^{-2} 6 ms	**5.1.3**, **5.1.2**	15 nm $Si_{0.73-0.5x}Ge_{0.27-0.5x}Sn_x$ after r-FLA with a peak pre-heating temperature of 570 °C, E_d = 120 J cm^{-2} and a flash length of 6 ms ($T \approx$ 880 °C), SOI wafer B from **section 8.11**
SiGeSn r-FLA 150 J cm^{-2} 20 ms	**5.1.3**, **5.1.2**	15 nm $Si_{0.73-0.5x}Ge_{0.27-0.5x}Sn_x$ after r-FLA with a peak pre-heating temperature of 570 °C, E_d = 150 J cm^{-2} and a flash length of 20 ms ($T \approx$ 960 °C), SOI wafer B from **section 8.11**

SiGeSn:P as-implanted	**5.1.4**	16 nm $Si_{0.681}Ge_{0.308}Sn_{0.011}$:P ($^{31}P$ implantation: E = 12 kV, D_I = 7.4 x 10^{13} cm^{-2}, ω = 7°, R_p ≈ 15 nm including ≈ 8.6 nm SiN_x in layer stack, T < -100 °C), SOI wafer B from **section 8.11**
SiGeSn:P r-FLA 120 J cm^{-2} 6 ms	**5.1.4**	16 nm $Si_{0.681}Ge_{0.308}Sn_{0.011}$:P after r-FLA with a peak pre-heating temperature of 570 °C, E_d = 120 J cm^{-2} and a flash length of 6 ms (T ≈ 880 °C), SOI wafer B from **section 8.11**
SiGeSn:Ga as-implanted	**5.1.4**	16 nm $Si_{0.681}Ge_{0.308}Sn_{0.011}$:Ga ($^{69}Ga$ implantation: (E = 20 kV, 7°, D_I = 1.4 x 10^{14} cm^{-2} , ω = 7°, R_p ≈ 15 nm including ≈ 8.6 nm SiN_x in layer stack, T < -100 °C), SOI wafer B from **section 8.11**
SiGeSn:Ga r-FLA 120 J cm^{-2} 6 ms	**5.1.4**	16 nm $Si_{0.681}Ge_{0.308}Sn_{0.011}$:Ga after r-FLA with a peak pre-heating temperature of 570 °C, E_d = 120 J cm^{-2} and a flash length of 6 ms (T ≈ 880 °C), SOI wafer B from **section 8.11**
$Ge_{0.94}Sn_{0.06}$ as-grown	**5.2, 6**	20 nm n-$Ge_{0.94}Sn_{0.06}$:Sb (5 x 10^{19} cm^{-3}), T_S ≈ 180 °C, g_r = 0.1 nm s^{-1} , Φ_{Ge} = 4.045 x 10^{14} $cm^{-2}s^{-1}$, Φ_{Sn} = 2.58 x 10^{13} $cm^{-2}s^{-1}$, SOI wafer A from **section 8.11**
$Ge_{1-x}Sn_x$ PLA 0.12	**5.2, 6**	$Ge_{0.94}Sn_{0.06}$ as-grown after PLA with E_d =0.12 J cm^{-2}, SOI wafer A from **section 8.11**
$Ge_{1-x}Sn_x$ PLA 0.15	**5.2, 6**	$Ge_{0.94}Sn_{0.06}$ as-grown after PLA with E_d =0.15 J cm^{-2}, SOI wafer A from **section 8.11**
$Ge_{1-x}Sn_x$ PLA 0.18	**5.2**	$Ge_{0.94}Sn_{0.06}$ as-grown after PLA with E_d =0.18 J cm^{-2}, SOI wafer A from **section 8.11**
$Ge_{1-x}Sn_x$ PLA 0.2	**5.2**	$Ge_{0.94}Sn_{0.06}$ as-grown after PLA with E_d =0.20 J cm^{-2}, SOI wafer A from **section 8.11**
$Ge_{1-x}Sn_x$ f-FLA	**5.2**	$Ge_{0.94}Sn_{0.06}$ as-grown after f-FLA with E_d = 48 J cm^{-2} and a pulse length of 3.2 ms, SOI wafer A from **section 8.11**
$Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown	**5.2, 6**	20 nm n-$Si_{0.14}Ge_{0.80}Sn_{0.06}$:Sb (5 x 10^{19} cm^{-3}), T_S ≈ 200 °C, g_r = 0.17 nm s^{-1} , Φ_{Si} = 1.173 x 10^{14} $cm^{-2}s^{-1}$, Φ_{Ge} = 6.646 x 10^{14} $cm^{-2}s^{-1}$, Φ_{Sn} = 4.99 x 10^{13} $cm^{-2}s^{-1}$, SOI wafer A from **section 8.11**
$Si_{1-x-y}Ge_ySn_x$ PLA 0.15	**5.2, 6**	$Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown after PLA with E_d =0.15 J cm^{-2}, SOI wafer A from **section 8.11**
$Si_{1-x-y}Ge_ySn_x$ PLA 0.20	**5.2, 6**	$Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown after PLA with E_d =0.20 J cm^{-2}, SOI wafer A from **section 8.11**
$Si_{1-x-y}Ge_ySn_x$ PLA 0.25	**5.2, 6**	$Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown after PLA with E_d =0.25 J cm^{-2}, SOI wafer A from **section 8.11**
$Si_{1-x-y}Ge_ySn_x$ f-FLA	**5.2**	$Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown after f-FLA with E_d = 48 J cm^{-2} and a pulse length of 3.2 ms, SOI wafer A from **section 8.11**

8.13 Calculation of the ion beam implantation parameter by SRIM

In order to estimate the implantation parameters, “transport of ions in matter” (TRIM) simulations with the software code “stopping and range of ions in matter” (SRIM) [249] are performed with different Si_3N_4 capping layer thicknesses of 5, 8.6 and 15 nm and Sn implantation acceleration energies between 15 and 50 kV. At this stage, it must be mentioned that the software SRIM is suspect to some assumptions like the complete layer stack is amorphous, implantation temperature is 0 K, and every ion is simulated independently of previously implanted ions (dose always zero). The challenging task is to have, on the one hand, a thick enough capping layer to protect the $Si_{1-y}Ge_y$ surface from surface degradation (see **section 5.1 i)**) and on the other hand, the cap should be thin enough to implant the $Si_{0.73}Ge_{0.27}$ layer without amorphization of the single-crystalline seed layer. As visible in Fig. 8.13 - 1 a) for an acceleration voltage of 26 kV and an 8.6 nm thick Si_3N_4 layer, the maximum Sn concentration is close to the center of the $Si_{0.73}Ge_{0.27}$ layer, and the Sn ion collision cascade stops slightly in front of the BOX SiO_2. The reduction of Si_3N_4 layer thickness to 5 nm shifts the peak concentration deeper in the $Si_{0.73}Ge_{0.27}$ layer and leads to an Sn implantation into the SiO_2 interface. This deep end-of-range implantation tail can convert the entire seed crystal into an amorphous state (depending on the selected fluence). Hence, amorphization until SiO_2 must be avoided to maintain a seed crystal. An increase in the Si_3N_4 layer thickness shifts the maximum of the Sn peak closer to the Si_3N_4 / $Si_{0.73}Ge_{0.27}$ interface into the Si_3N_4, as visible for 15 nm thick Si_3N_4. This could lead to a shallow Sn implantation close to the $Si_{0.73}Ge_{0.27}$ surface. Another solution would be to adjust the acceleration voltage, as shown in Fig. 8.13 - 1 b). A reduction of the ion beam implantation energy from 26 kV to 15 kV for a 5 nm thick Si_3N_4 layer might be a solution in terms of the implantation profile but might be close to the critical threshold thickness to maintain the surface quality. On the other hand, an increase in the implantation energy to 50 kV for 15nm Si_3N_4 would cause a long tail of collision cascades and can destroy the Si seed crystal. Therefore, an Si_3N_4 capping layer below 10 nm is favorable for this thin film SiGeSn fabrication approach.

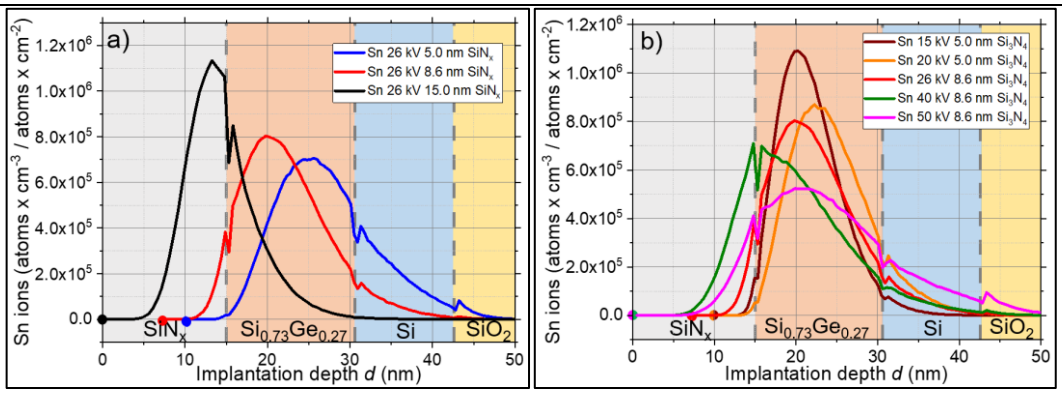

Fig. 8.13 - 1: Simulated Sn implantation depth profile with a constant implantation energy of E = 26 kV and different Si_3N_4 layer thickness of d = 5, 8.6 and 15 nm a). Simulated Sn implantation depth profile for different implantation energies E = 15, 20, 26, 40, and 50 kV b). The simulations were performed with TRIM for the used $Si_{0.73}Ge_{0.27}$ on SOI material under an implantation angle of 7°. The Si_3N_4 thickness-dependent starting point of the simulation results is highlighted with large dots.

The required implantation fluence D_I is calculated by Eq. 8.13 - 1 with the help of the ions per depth profile n_I generated by the TRIM simulation and the required dopant concentration c_D.

In general, it can be assumed that the low-temperature implantation is fortunate for the amorphization because the diffusion-related self-healing process of the crystal during the ion beam implantation is inhibited due to the temperature-dependent diffusion mechanism.

$$D_I = \frac{c_D}{n_I} \qquad \text{Eq. 8.13 - 1}$$

$$c_D = \frac{N_D}{c_{Sn}} \qquad \text{Eq. 8.13 - 2}$$

The required dopant concentration c_D can be calculated by Eq. 8.13 - 2 with the knowledge of the total atom concentration N_D and the targeted Sn concentration c_{Sn}.

8.14 RBS simulation results for section 5.1

The investigated SiGeSn layers in **section 5.1.3** are about 15 nm thick. This small thickness is close to the depth resolution limit of RBS of about 10 nm for the used setup and requires additional measurements to confirm the commonly used RBS-R measurements under an incident angle ω = 0°. Fortunately, the used setup (see **section 3.6**) allows to increase ω from 0° to 80°. This measure increases the probed SiGeSn layer thickness from 15 nm to about 85 nm, as illustrated in the inset of Fig. 8.14 - 1. The RBS-R peak intensity of thin layers depends on the chemical composition and thickness. Hence, the peak width and height of each element in the spectra appear to be larger under ω = 80°, compared to the ω = 0° case in Fig. 8.14 - 1. The higher intensities allow a more accurate extraction of the chemical composition by the spectra simulation with SIMNRA. The simulated elemental spectra of the Sn, Ge, and Si are shown in Fig. 8.14 - 1 for the ω = 80° case and correspond to an about 16 nm thick layer of $Si_{0.681}Ge_{0.308}Sn_{0.011}$. The simulation accuracy is about ± 0.1 at.%. For this simulation, a homogeneous $Si_{1-x-y}Ge_ySn_x$ layer on Si is assumed without taking into account a Gaussian implantation profile. Therefore, deeper trail regions of the measured Ge and Sn spectra are not covered by the simulation.

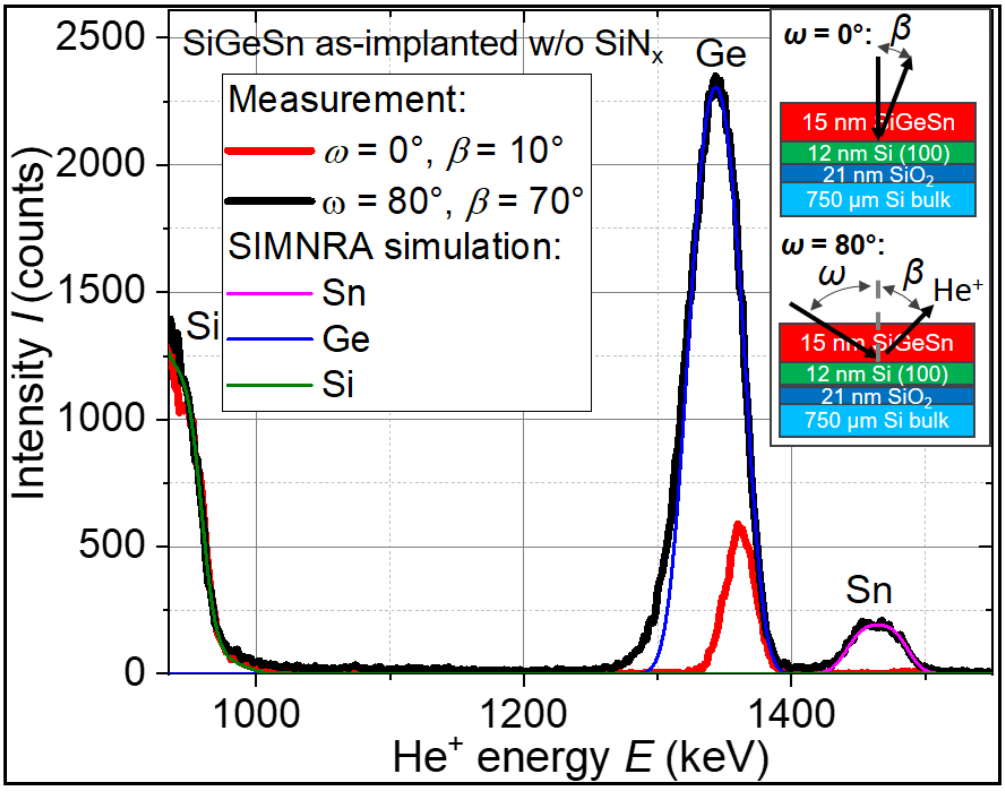

Fig. 8.14 - 1: RBS-R results of the SiGeSn samples in the as-implanted state measured ander an incident angle ω of 0° and 80°, exit angle β of 10° and 70° and a constant detector angle of 170°. SIMNRA simulated elemental spectra of Sn (magenta), Ge (blue), and Si (green) of the SiGeSn as-implanted sample measured with ω = 80° and β = 70°. The inset illustrates the two different measurement configurations.

8.15 GI-XRD and (224) XRD-RSM results for section 5.1

The GI-XRD measurements in Fig. 8.15 - 1 neither show β-Sn nor any other diffraction peak. Hence, the crystal structure in the SiGe as-grown material, after Sn implantation and after r-FLA, is mainly single-crystalline.

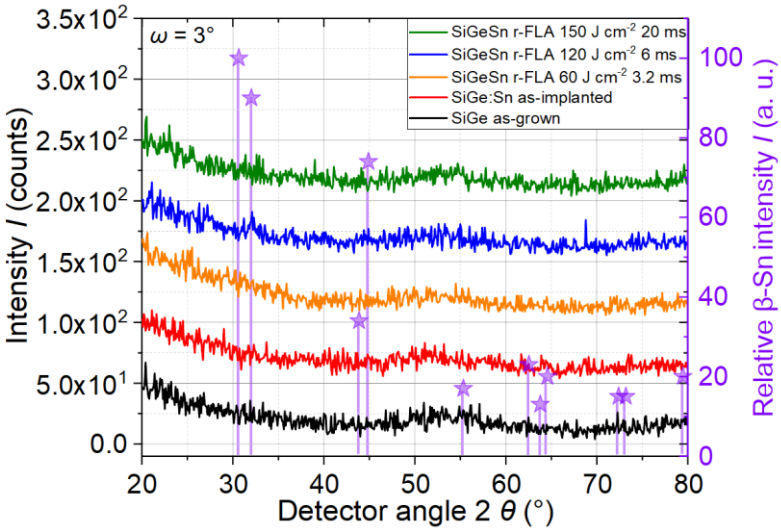

Fig. 8.15 - 1: Grazing incidence GI-XRD with a constant incident angle $\omega = 3°$ of the SiGe as-grown reference, SiGe:Sn as-implanted state and SiGeSn after r-FLA with $E_d = 60$ J cm^{-2} and a pulse length of 3.2 ms, $E_d = 120$ J cm^{-2} and a pulse length of 6 ms and $E_d = 150$ J cm^{-2} and a pulse length of 20 ms. The relative intensities of β-Sn-related diffraction, obtained from ref. [76], are added with purple stars. In order to distinguish between the measurement results, a visualization offset with increasing energy densities is applied.

The (224) XRD-RSM results in Fig. 8.15 - 2 complete the measurement results in Fig. 5.1 - 6 and confirm the partial strain relaxation state of the fabricated $Si_{1-x-y}Ge_ySn_x$ alloys after ion beam implantation of Sn in pseudomorphically grown SiGe on SOI and r-FLA.

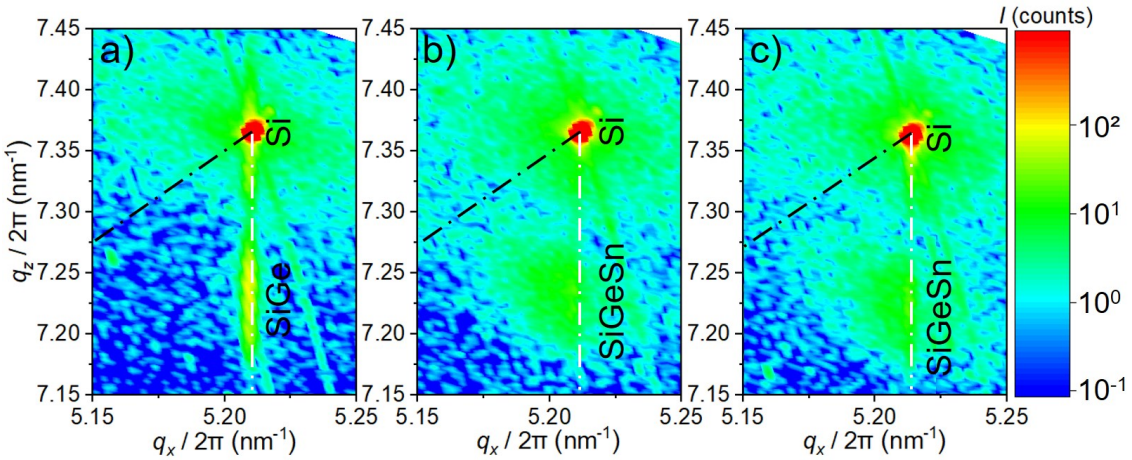

Fig. 8.15 - 2: (224) XRD-RSM of the SiGe reference on SOI a), $Si_{1-x-y}Ge_ySn_x$ after r-FLA for 3.2 ms with $E_d = 60$ J cm^{-2} b), $Si_{1-x-y}Ge_ySn_x$ after r-FLA for 20 ms with $E_d = 150$ J cm^{-2} c). The white vertical dash-dot line corresponds to the fully pseudomorphically grown state, and the black dash-dot line is the strain relaxation line for a fully relaxed alloy on Si.

8.16 SIMS limitations for section 5.1.4

SIMS is a method to investigate the chemical composition of solid materials on the surface. The technique is based on the sputtering of investigated material with a primary ion beam. Afterward, the mass/charge - ratio of the generated secondary ions is analyzed using a mass spectrometer and detector (see **section 3.8**). This method is highly sensitive and accurate as long as the sputter rate is stable and a well-calibrated reference is available. However, the interpretation of the SIMS data obtained from special alloys, like $Si_{1-x-y}Ge_ySn_x$, and thin films causes some uncertainties, which will be briefly discussed. For quantitative analysis of the obtained SIMS results, a reference sample with known parameters is necessary for high accuracy. In this particular case, a $Si_{0.669}Ge_{0.311}$ doped with P sample form IHP was used to quantify Ge, Si, and P. This reference sample is slightly different than the actual SIMNRA simulated $Si_{0.681}Ge_{0.308}Sn_{0.011}$ layer concentration. Therefore, the quantitative data should be treated carefully. Owing to the isolation by the SiN_x capping, charging of the samples was observed. This further decreases the focus and increases redeposition during the measurement, which again decreases the depth resolution of the measurement. For that reason, the sputter depth of the Ga and P implanted series is slightly different. In order to reduce the charging influence, sputtering breaks were included in the measurement procedure (“Non-interlaced” measurement mode). Additionally, the quantification of elements within the SiN_x cap was not possible, and O was found within the cap (therefore, the SiN_x results are not shown in Fig. 5.1 - 8). The presence of O coincides with the cross-sectional TEM-EDXS results. Unfortunately, O influences the sputter yield dramatically, and recoil implantation of O might also influence the sputter yield within the $Si_{1-x-y}Ge_ySn_x$ layer. Furthermore, the investigated layers are quite thin, which decreases the sensitivity. Finally, the Gaussian implantation profiles can cause deviations in the sputtering rate across the layer thickness.

8.17 RBS of $Ge_{1-x}Sn_x$ on SOI for section 5.2.3

As explained in **appendix 8.14** in detail, the layer thickness of the investigated $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ is close to the resolution limit of RBS. Hence, small changes in the chemical composition and layer thickness are better visible when the layers are investigated under a large incident angle. Therefore, the $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ are measured under an incident angle $\omega = 80°$ and exit angle $\beta = 70°$ before and after post-growth thermal treatments.

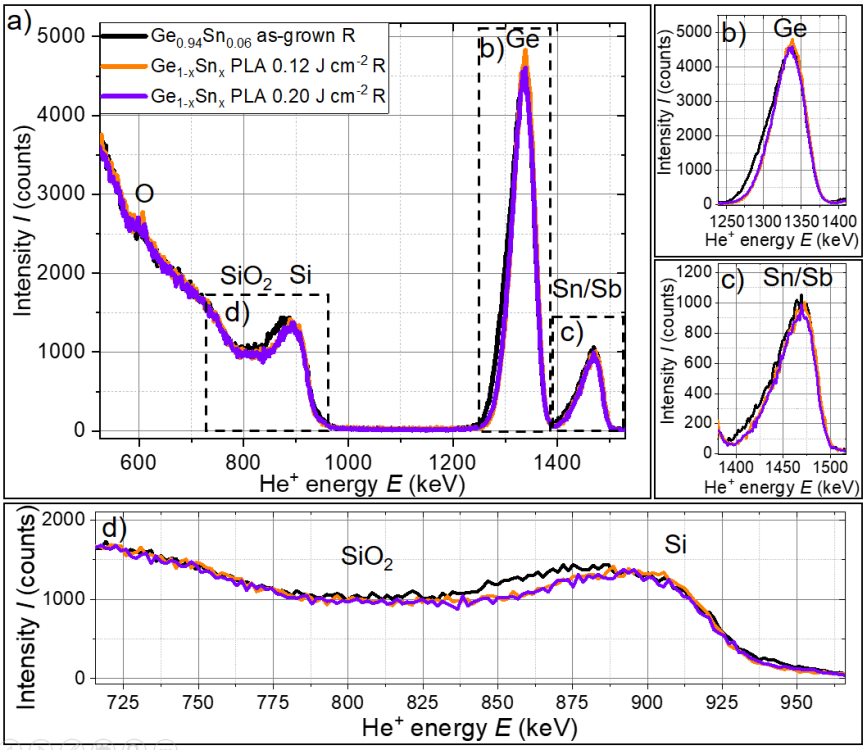

Fig. 8.17 - 1: RBS-R results of the $Ge_{1-x}Sn_x$ on SOI material in the as-grown state, after PLA with 0.12 and 0.2 J cm^{-2} a). The marked windows in a) show the enlargements of the Ge b) and Sn/Sb c) contributions in $Ge_{1-x}Sn_x$. The measurements are performed under an incident angle $\omega = 80°$ and exit angle $\beta = 70°$.

The representative results of the $Ge_{1-x}Sn_x$ sample series are shown in Fig. 8.17 - 1 in the as-grown state and after PLA with the smallest and highest used E_d. Ge and Sn/Sb contributions in Fig. 8.17 - 1 b) and c) indicate a slightly smaller layer thickness after PLA, but the intensities are almost the same as the as-grown state. At the same time, the Si signal remains in its position at high energies (see Fig. 8.17 - 1 d)). If the E_d is too high, then a diffusion of Si towards the surface (spectra extension to higher energies) and diffusion of Ge and/or Sn/Sb towards Si (spectra extension to smaller energies) would be expected, causing a $Si_{1-x-y}Ge_ySn_x$ alloy formation at the interface. Furthermore, the observed shifts between the as-grown state and PLA-treated samples are in the same range as the O signal at around 600 keV from the $Ge_{1-x-y}Sn_xO_y$ layer on the surface. Hence, the results suggest no intermixing between Si and $Ge_{1-x}Sn_x$ due to PLA.

8.18 Fit procedure for SOI RSM peak positions

Knowledge of a tilt between the thick Si carrier substrate and the SiGeSn layer is necessary for quantitative strain calculation within the $Si_{1-x-y}Ge_ySn_x$ layer. In the case of the epitaxial growth on a single-crystalline substrate, an epitaxially grown $Si_{1-x-y}Ge_ySn_x$ with an almost preserved lattice orientation compared to the used substrate can be assumed. However, the 20 nm thick SOI layer, which was used as the seed for the epitaxial growth of $Ge_{0.94}Sn_{0.06}$ or $Si_{0.14}Ge_{0.80}Sn_{0.06}$ in **section 5.2** can be tilted relative to the about 750 µm thick carrier substrate. The tilt was investigated with XRD-RSM around the (004) reflection after a rocking curve pre-alignment on the Si carrier substrate reflection. The symmetrical (004) reflection was used since $q_x/2\pi$ must be located at 0 nm^{-1} if the layer is epitaxially grown. Any deviation of the $Si_{1-x-y}Ge_ySn_x$ signal from $q_x / 2\pi = 0$ nm^{-1} can be understood as a layer tilt. The reciprocal lattice parameters q_x and q_z of the (004) Si substrate and the (004) $Si_{1-x-y}Ge_ySn_x$ layer were determined by fitting their RSM reflection positions, as shown in Fig. 8.18 - 1.

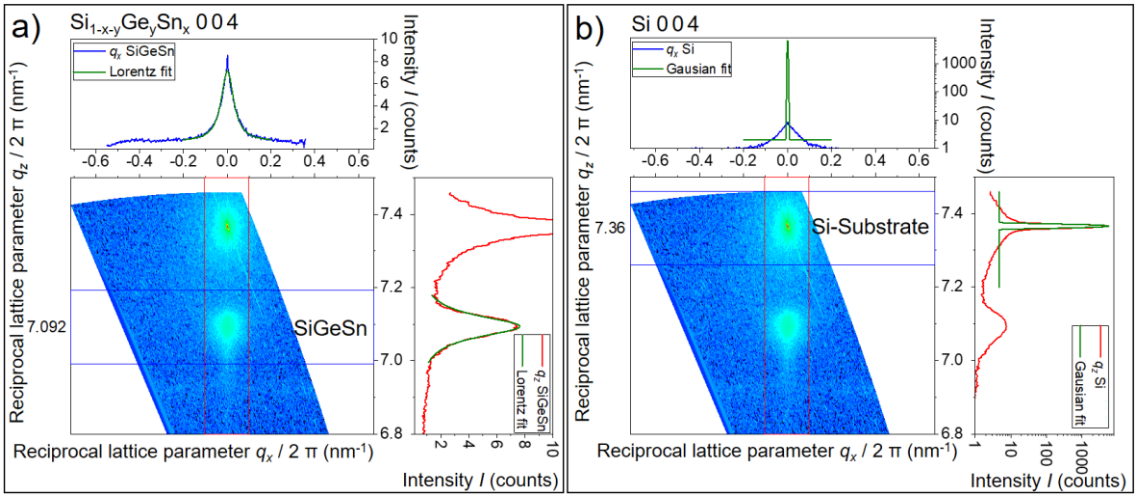

Fig. 8.18 - 1: Fitting procedure of the reciprocal lattice parameters q_x and q_z based on RSM around the (004) reflection of epitaxially grown $Si_{1-x-y}Ge_ySn_x$ layer a) and (004) Si carrier substrate b). The SiGeSn peak position was fitted with a Lorentzian function, and the Si substrate was fitted with a Gaussian function. For both cases, the adjusted R^2 was above 98%.

Afterward, the tilt angle δ was calculated using Eq. 8.18 - 1. The calculated tilt between the Si substrate and the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys was between 1×10^{-2}° and 1×10^{-5}° for all investigated samples. This tilt is small enough to be neglected. Therefore, it can be concluded that all shifts of the asymmetrical (224) in Fig. 5.2 - 5 and Fig. 5.2 - 6 are caused by changes in the $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ alloy lattice parameters, respectively.

$$\delta = \arctan\left(\frac{q_{x,Si(004)}}{q_{z,Si(004)}}\right) - \arctan\left(\frac{q_{x,SiGeSn(004)}}{q_{z,SiGeSn(004)}}\right) \qquad \text{Eq. 8.18 - 1}$$

8.19 Supporting µ-Raman results for section 5.2.3

µ-Raman is performed to support the XRD and RBS data. The µ-Raman spectra in Fig. 8.19 - 1 a) and b) contain the Ge-Ge (≈300 cm^{-1}), Si-Ge (≈400 cm^{-1}), Si-Si (≈475 cm^{-1}), and Si-Si (520.5 cm^{-1}) phonon modes. The Si-Si mode at 520.5 cm^{-1} belongs mainly to the strain-relaxed Si carrier substrate but also contains contributions of the 20 nm thick SOI layer. The other modes can be attributed to the thin $Ge_{1-x}Sn_x$ or $Si_{1-x-y}Ge_ySn_x$ layer and appear as slightly red-shifted due to the interaction between the Sn concentration and strain, as explained in **section 4.1.3** on the example of $Ge_{1-x}Sn_x$. None of the measured Raman spectra showed an Sn-Sn, which was expected at around 190 cm^{-1}. This might be related to the relatively low Sn concentration in combination with the thin layer thickness, which decreases the Sn-Sn detection probability and intensity. The $Ge_{0.94}Sn_{0.06}$ as-grown and f-FLA state in Fig. 8.19 - 1 a) shows a broad Ge-Ge mode, which can be divided in a main peak slightly below 300 cm^{-1} and a small kink slightly above 300 cm^{-1}. Similar double peaks can be obtained in Fig. 8.19 - 1 b) for the Ge-Ge and Si-Ge modes of $Si_{0.14}Ge_{0.8}Sn_{0.06}$. The similarities between the as-grown and f-FLA states indicate that the selected FLA parameters do not influence the strain or alloy composition, which coincides with the RBS and XRD findings in **section 5.2.3**. Furthermore, the double peak suggests two different strain states within the as-grown layers, which supports the hypothesis of a Stranski-Krastanov growth mechanism. The first nanometers are mainly pseudomorphically grown layer by layer on the SOI. This highly compressive strained layer belongs to the smaller kinks at higher wavenumbers in the Ge-Ge and Si-Ge modes. When the layer exceeds the critical layer thickness, the layer starts to relax by defect formation, which shifts the peak towards lower wavenumbers. After PLA, the observed double peaks merge for both alloys in Fig. 8.19 - 1, the FWHM is reduced, and the overall intensity increases. This is related to an improvement of the layer quality or homogeneity. Additionally, an Si-Ge mode emerged for $Ge_{1-x}Sn_x$ in Fig. 8.19 - 1 a) after PLA with 0.2 J cm^{-2}. The presence of this peak indicates a local formation of $Si_{1-x-y}Ge_ySn_x$ or $Si_{1-y}Ge_y$ due to diffusion between the former $Ge_{0.94}Sn_{0.06}$ and the SOI layer. The Raman spectra in Fig. 8.19 - 1 b) contain additional Si-Si modes at ≈ 460 cm^{-1} after PLA, which could either come from $Si_{1-x-y}Ge_ySn_x$ or from highly tensile strained SOI. However, similar Si-Si modes were observed in thick film $Si_yGe_{1-x-y}Sn_x$ (x = 2 - 12 at.% and y = 4 - 19 at.%) grown on a thick Ge-buffer [187]. Therefore, it is more likely that the Si-Si modes are only more pronounced compared to the as-grown state due to the generally higher intensity. The asymmetrical peak shape of the Si-Ge-Sn-related modes can be observed independent of the annealing conditions for both materials. This can be caused by different

phenomena: I) The strain and concentration-dependent peak position might be affected by an inhomogeneous strain distribution across the layer thickness, which was already concluded for $E_d \leq 0.15$ J cm^{-2}. II) It is known from comprehensive Raman studies on thicker $Si_{1-x-y}Ge_ySn_x$ layers and different laser wavelengths that the main Raman modes in the Ge-Sn and Si-Ge-Sn systems tend to overlap each other depending on their concentration and strain [187]. For example, the expected peak positions for the not well-distinguishable main phonon modes of Ge-Sn and Si-Sn are located at around 260 cm^{-1} and 370 cm^{-1}, respectively [187]. III) The Fano effect, which describes the interaction between carriers and phonons, can cause a peak broadening and peak shift in the highly Sb-doped (5×10^{19} cm^{-3}) samples.

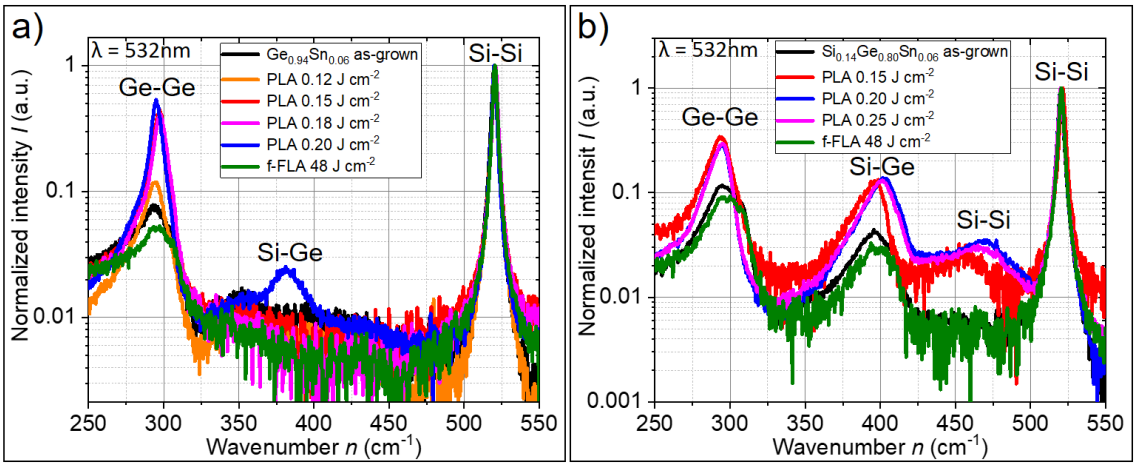

Fig. 8.19 - 1: µ-Raman spectra of the $Ge_{1-x}Sn_x$ on SOI a) and $Si_{1-x-y}Ge_ySn_x$ on SOI b) in the as-grown state, after PLA with energy densities between 0.12 and 0.25 J cm^{-2} and f-FLA with 48 J cm^{-2} for 3.2 ms. This figure is a reprint of Fig. 5.2 - 7.

By comparing the Ge-Ge peak positions in Fig. 8.19 - 1 a), it can be concluded that the slight out diffusion due to PLA does not affect the peak position significantly. This might be related to the low incorporation rate of Sn on substitutional lattice positions. For $Si_{1-x-y}Ge_ySn_x$ in Fig. 8.19 - 1 b), the Ge-Ge and Si-Ge mode after PLA with E_d = 0.2 and 0.25 J cm^{-2} are located at similar wavenumbers compared to the main peaks of the as-grown state, which indicates only a limited out-diffusion of alloy components. However, the PLA 0.15 J cm^{-2} sample shows red-shifted phonon modes due to the presence of tensile strain. This can be understood by introducing tensile strain into the SiGeSn layer, which was already concluded from (224) XRD-RSM in Fig. 5.2 - 6 b).

8.20 Process details for n-JNT fabrication

The presented JNTs were manufactured in the “Nanofabrication Facility in Rossendorf (NanoFaRo)” at HZDR and at “Leibniz-Institut für Festkörper- und Werkstoffforschung Dresden (IFW)”. Details about the most relevant JNT process steps (see Fig. 6.2 - 1) are summarized in Table 8.20 - 1. The thermal treatments (PLA step (2) and FLA step (19)) were performed with the setups introduced in **sections 3.3** and **3.4**. Most of the wet chemical processes were performed in the cleanroom (see **section 3.12**) facility at HZDR. The EBL designs for steps (4), (9), and (15) were developed by Oliver Steuer with the commercial software of Raith GmbH. Afterward, EBL was performed either with the Raith 150-TWO or the e_LiNE EBL system of Raith GmbH. ALD (13) and RIE (6) were performed at “Leibniz-Institut für Festkörper- und Werkstoffforschung Dresden (IFW)”. Processes that have been carried out more than once have more steps, and the second number describes the chronological order.

Table 8.20 - 1: Overview of the most important process steps used to fabricate $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI JNTs in **Chapter 6**. The fabrication steps and step numbers are related to the description of Fig. 6.2 - 1. The column equipment and recipe describe the details of the step.

Process	Step	Equipment	Recipe
MBE	(1)	MBE (see **section 3.1**)	See **appendix 8.12**
Sample cleaning	(2-1), (3-1)	Wet bench, USB	Acetone (aq.) 10 min, IPA (aq.) 10 min, N_2 blow-drying
PLA	(2-2)	PLA (see **section 3.3**)	PLA with E_d between 0.12 and 0.25 J cm^{-2}
GeO_x etching	(3-2), (13-1)	Wet bench	Acetic acid:DI-water volume ratio 1:7, etch time 10 min, DI-water dip for 10 s, N_2 blow-drying
HSQ spin coating	(3-3)	Spin coater, hot plate	3% HSQ:MIBK (ratio between HSQ 6% and MIBK 50:50) spin coating at 3000 rpm for 45 s gives ≈ 70 nm thick resist layer, post bake T = 120 °C for 2 min
EBL HSQ	(4)	Raith 150-TWO, Raith e_LiNE	Acceleration voltage: 10 kV; aperture: 30 µm; write field: 100 x 100 µm²; area step size NW: 4 nm, area dose NW ≈ 550 – 480 µC cm^{-2}; area step size 10 x 10 µm² pads and trapezoids: 10 nm; area dose pads and trapezoids ≈ 170 – 300 µC cm^{-2}
Development HSQ	(5)	Wet bench	25 wt.% TMAH:DI for 15 s, MF-319 for 30 s, DI rinse for 30 s, IPA for 30 s, N_2 blow-drying
ICP-RIE	(6)	Oxford ICP-RIE	Gas: BCl_2 10 sccm, Cl_2 20 sccm, Argon 20 sccm, Helium 7 sccm; pressure 0.02 mbar, radio-frequency power (RF) = 50 W, DC Bias = 230 V, ICP power = 350 W; Etch time = 15 s

HSQ stripping	(7)	Wet bench	1% HF:DI for 55 s, DI rinse for 30 s, IPA for 10 s, N_2 blow-drying
ZEP spin coating	(8),	Spin coater, hot plate	Pre-bake at T = 180 °C for 3 min; spin coating ZEP520A at 3000 rpm for 60 s gives a ≈ 300 nm thick resist layer; post-bake at T = 180 °C for 10 min
EBL source/drain contacts	(9)	Raith 150-TWO, Raith e_LiNE	Acceleration voltage: 10 kV; aperture: 30 µm, write field: 1000 x 1000 µm², area step size 40 nm for 120 x 110 µm Ni pads; Area dose: 35 µC cm^{-2}
ZEP development	(10)	Wet bench	n-Amyl-Acetate (ZED-N50) for 90 s, IPA for 30s, N_2 blow-drying
Native oxide etching	(11-1)	Wet bench	0.5% HF:DI for 50 s, 30 s DI, N_2 blow-drying
Ni evaporation	(11-2)	Creavac Creamet 600 thermal evaporator	Thermal evaporation of a 50 nm thick Ni layer with a deposition rate of 0.25 nm s^{-1}
ZEP lift-off	(12)	Wet bench	Acetone for 30 min, IPA for 2 min, N_2 blow-drying
ALD Al_2O_3	(13-2)	ALD Veeco Savannah S200	Thermal ALD at 120 °C; sequences with a pulse length of 0.015 s for the precursor DI and Trimethylaluminum (TMA) and wait periods of 5 s, number of cycles: 70, Al_2O_3 thickness ≈ 7 nm; ALD starts with a H_2O pre-pulsing
PMMA spin coating	(14)	Spin coater, hot plate	Pre-bake at T = 180 °C for 3 min; spin coating 950K0.2 PMMA at 3000 rpm for 60 s gives a ≈ 60 nm thick resist layer; post-bake at T = 180 °C for 10 min
EBL top-gate	(15)	Raith 150-TWO, Raith e_LiNE	Acceleration voltage: 10 kV, aperture: 30 µm write field: 1000 x 1000µm², area step size 20 nm; line dose 1500, 1750, 2205 pC cm^{-1}
PMMA development	(16)	Wet bench	DI:IPA 7:3 for 30 s, IPA for 30s, N_2 blow-drying
Pt and Au evaporation	(17)	Creavac Creamet 600 thermal evaporator	Thermal evaporation of a 25 nm thick Pt layer with a deposition rate of 0.4 nm s^{-1} and a 5 nm thick Au layer with a deposition rate of 0.3 nm s^{-1}.
PMMA lift-off	(18)	Wet bench	Acetone for 30 min, IPA for 2 min, N_2 blow-drying
f-FLA	(19)	FLA (see **section 3.4**)	f-FLA with E_d = 48 J cm^{-2} and a pulse length of 3.2 ms under N_2 atmosphere

8.21 Flat-band voltage V_{FB} and on-current I_{on} of JNTs

The flat-band voltage V_{FB} is the gate voltage V_G at which the JNT channel is entirely open in the flat-band condition (see Fig. 6.1 - 1 c)). This means the JNT is turned on, and the I_{on} can flow between the drain and the source. V_{FB} is located at the maximum of transconductance g_m, which can be calculated using Eq. 8.21 - 1.

$$g_m = \frac{dI_{DS}}{dV_G} \qquad \text{Eq. 8.21 - 1}$$

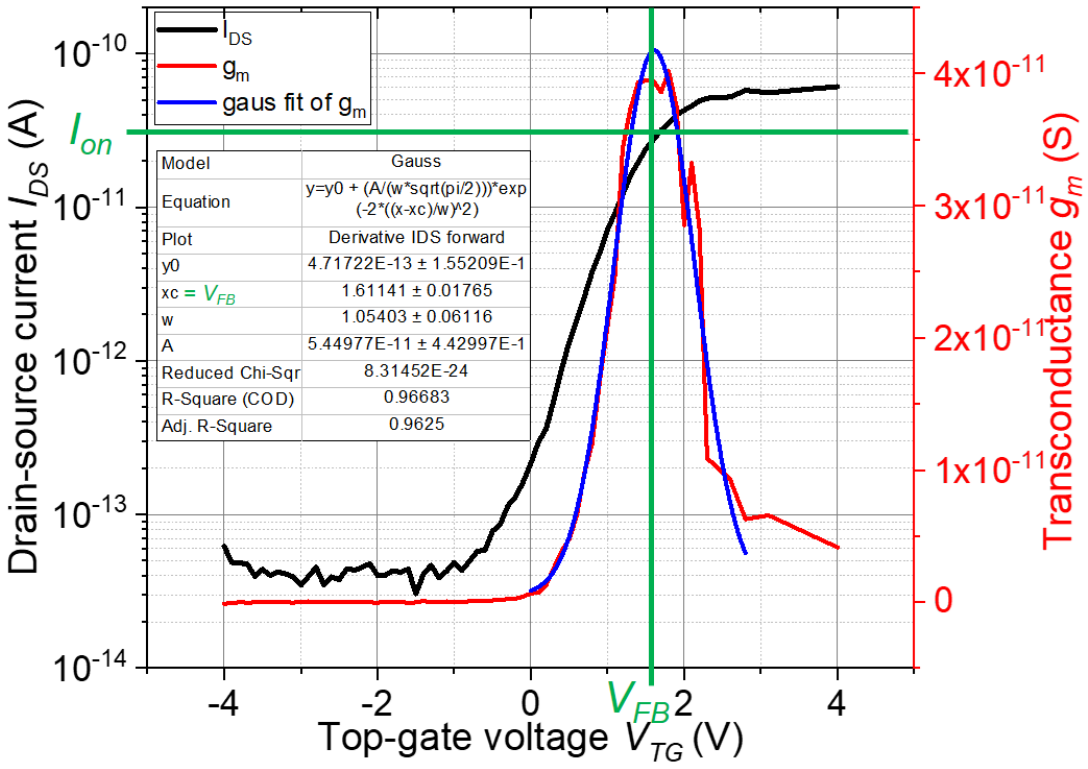

Fig. 8.21 - 1: Extraction of V_{FB} and I_{on} using the transconductance g_m and a Gauss peak fit of g_m.

8.22 I_{off}, I_{max}, I_{on}/I_{off}- and I_{max}/I_{off}-ratio of JNTs

The off-current I_{off} is a leakage current between the drain and the source I_{DS} when the JNT is in the depletion mode (see Fig. 6.1 - 1 a)). This means that the channel is entirely depleted of carriers, which prevents a sufficient current flow. On the other hand, the maximum drain-source current I_{max} is the I_{DS} in the accumulation mode of the JNT (see Fig. 6.1 - 1 d)). Furthermore, the on-current I_{on} is the I_{DS} at the flat-band voltage, which is explained in **section 8.21** in detail. The I_{off} and I_{max} parameters can be obtained directly from the transfer characteristic. In this work, the transfer characteristics were determined with a double sweep from 0 V to +40 V to -40 V to +40 V to -40 V to 0 V for the back-gating case or 0 V to +4 V to -4 V to +4 V to -4 V to 0 V for the top-gating case. Then, the I_{off} was defined as the measured minimum I_{DS} and I_{max} as the maximum I_{DS} of the forward sweep between -40 V and +40 V (back-gating) or -4 V and +4 V (top-gating). The I_{max}/I_{off}-ratio, as well as the I_{on}/I_{off}-ratio, are transistor figures of merits, which describe the ratio between I_{max} and I_{off} or I_{on} and I_{off} calculated by Eq. 8.22 - 1 and Eq. 8.22 - 2.

$$I_{max}/I_{off} = \frac{I_{max}}{I_{off}} \qquad \text{Eq. 8.22 - 1}$$

$$I_{on}/I_{off} = \frac{I_{on}}{I_{off}} \qquad \text{Eq. 8.22 - 2}$$

8.23 Subthreshold swing *SS* calculation of JNTs

The subthreshold swing *SS* is defined as the amount of voltage required to change the subthreshold current by one order of magnitude (decade). This can be approximated from the transfer characteristic with the drain-source current I_{DS} in a logarithmical scale and the gate voltage V_G in a linear scale with the help of Eq. 8.23 - 1. Since the slope in the subthreshold region is not everywhere exactly the same, it is common to select the steepest subthreshold slope (SS^{-1}) by using the inflection point of the logarithmic I_{DS}-V_G plot, as shown in Eq. 8.23 - 1. In this thesis, the inflection point was placed in the middle of I_{DS1} and I_{DS2}. Furthermore, a distance of approximately one decade is selected between I_{DS1} and I_{DS2}. Using Eq. 8.23 - 1 and the obtained values of ΔV_G, I_{DS1}, and I_{DS2} from Fig. 8.23 - 1 results in a *SS* of about 740 mV dec.$^{-1}$. In general, *SS* should be as small as possible for an effective switching between the OFF-state and the ON-state. On the other hand, *SS* can also be determined by using Eq. 8.23 - 2 with the depletion capacitance of the gate C_D, oxide capacitance C_{ox}, interface trap capacitance C_{it}, Boltzmann constant k_b, elementary charge q, and the absolute temperature T [313]. Therefore, changes in *SS* at a constant temperature correspond to changes in C_D, C_{ox}, and/or C_{it}.

$$SS = \frac{\Delta V_G}{\log\left(\frac{I_{DS1}}{I_{DS2}}\right)} \qquad \text{Eq. 8.23 - 1}$$

$$SS = \left(1 + \frac{C_{ox} + C_D + C_{it}}{C_{ox}}\right) \times \left(\frac{kT}{q}\right) \ln(10) \qquad \text{Eq. 8.23 - 2}$$

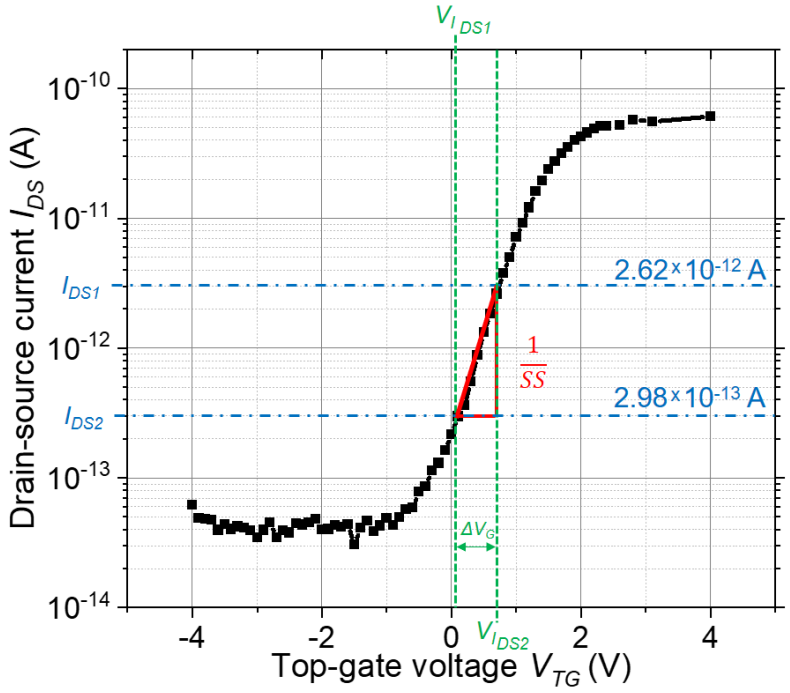

Fig. 8.23 - 1: Extraction of the subthreshold swing *SS* from a logarithmic transfer characteristic of a top-gated JNT. In this case, $V_{TG} = V_G$ and $\Delta V_G = 0.7$ V.

8.24 Threshold voltage V_{th} of JNTs

The threshold voltage V_{th} of a JNT is defined as the transition from a fully depleted to a partial depletion state (see Fig. 6.1 - 1 b)). In the case of partial depletion, the mobile charge changes non-linearly with the application of a gate voltage V_G. Therefore, the application of conventional linear extrapolation methods, like the ”Y-function” method or the linear extrapolation of I_{DS} versus $V_{G,}$ causes deviations in the device parameters [266, 268]. The recently presented approach by ref. [266] suggests applying the first derivative of the ratio between the transconductance g_m divided by the I_{DS} versus the gate voltage. The V_g at the minimum of the obtained $\frac{\mathrm{d}\frac{g_m}{I_{DS}}}{\mathrm{d}V_G}$ is taken as V_{th} [266]. However, the suggested approach did not lead to reasonable V_{th} for the back-gated JNTs, which might be related to the slightly different device behavior due to the p-Si layer below the n-$Ge_{1-x}Sn_x$ or n-$Si_{1-x-y}Ge_ySn_x$ layers. Therefore, the V_{th} is approximated for the back-gated devices by the following sequence: i) $V_{th,max}$ is calculated with Eq. 8.24 - 1. ii) Tangent equation is applied for the forward sweep of I_{DS} versus V_{BG} plot at $V_{BG} = V_{th,max}$. iii) Finally, the intercept of the tangent with the V_{BG} axis corresponds to the extracted V_{th}.

$$V_{th,max} = \frac{\mathrm{d}^2 I_{DS}}{\mathrm{d}{V_g}^2} \qquad \text{Eq. 8.24 - 1}$$

8.25 Gate configuration of $Si_{1-x-y}Ge_ySn_x$ JNTs

Fig. 8.25 - 1 a) shows the transfer characteristics of $Si_{1-x-y}Ge_ySn_x$ JNTs in dependence on a constant applied back-gate potential. The I_{on} and I_{max} increase with increasing V_{BG}. At the same time, I_{off} increases since the wide NW structures cannot be fully depleted by using the TG. Fig. 8.25 - 1 b) summarizes the evolution of the *SS* and I_{DS}-ratios in dependence on the back-gate potential. The lowest *SS* is 550 mV dec.$^{-1}$ achieved at V_{BG} = 0 V. Additionally, this configuration has remarkable I_{DS}-ratios of about 1 x 10^5. The I_{DS}-ratios can be slightly increased to about 2.5 x 10^5 (I_{on}/I_{off}) or 5 x 10^5 (I_{max}/I_{off}) by increasing V_{BG} to 6V. Hence, it is possible to boost the I_{DS}-ratios by applying an additional constant V_{BG} and sweeping the TG, but the inability to turn off the $Si_{1-x-y}Ge_ySn_x$ JNTs lowers the beneficial impact.

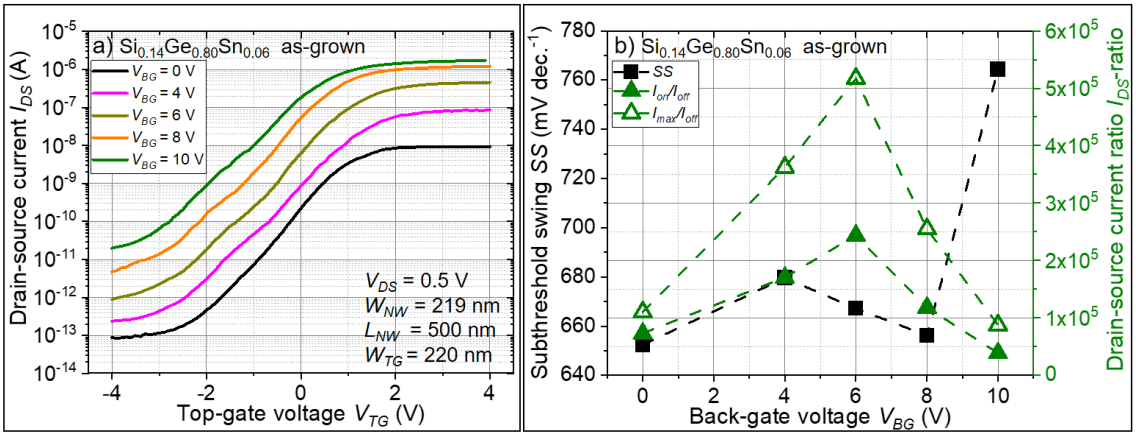

Fig. 8.25 - 1: Top-gated transfer characteristics of a $Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown JNT with a NW length of L_{NW} = 500 nm, width of W_{NW} of 219 nm, and a top-gate width W_{TG} of 220 nm in dependence on a constant back-gate potential V_{BG} between 0 and 10 V a). Extracted minimum subthreshold swing *SS* and drain-source current I_{DS}-ratios of the JNTs shown in a) plotted in dependence on V_{BG} b). Details about the parameter extraction can be obtained in **appendix 8.22** and **8.23**.

8.26 n-type transistors compared in Chapter 7

Table 8.26 - 1: Summary of the n-type $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ devices parameters compared in Fig. 7 - 2.

Year	Reference	SS (mV dec.$^{-1}$)	I_{on}/I_{off}-ratio	Channel material	Device structure
2024	This work	460	2.5×10^3	$Ge_{0.94}Sn_{0.06}$ on SOI	$Ge_{1-x}Sn_x$ PLA 0.15 on SOI JNT with a L_{NW} = 3 µm long, W_{NW} = 90 nm wide NW, and a W_{TG} = 210 nm wide top-gate. The measurement was performed with V_{DS} = 0.5 V by sweeping the top-gate (shown in Fig. 6.3 - 2).
2024	This work	550	1.5×10^8	$Ge_{0.94}Sn_{0.06}$ on SOI	$Ge_{1-x}Sn_x$ PLA 0.12 on SOI JNT with a NW length of L_{NW} = 500 nm, NW width of W_{NW} = 90 nm, and a top-gate width W_{TG} = 140 nm. The measurement was performed with V_{DS} = 0.5 V by sweeping the top-gate under a constant back-gate potential of 17 V (shown in Fig. 6.3 - 5).
2024	This work	625	1.1×10^5	$Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI	$Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI JNT with a NW length of L_{NW} = 500 nm, width of W_{NW} = 219 nm, and top-gate width of W_{TG} = 219 nm. The measurement was performed with V_{DS} = 0.5 V by sweeping the top-gate (shown in Fig. 8.25 - 1).
2023	[49]	92	7.5×10^3	$Ge_{0.95}Sn_{0.05}$	Vertical GAA n-FET with a NW diameter of 25 nm and gate length of 100 nm. The structure consists of a $GeSnO_x$/1 nm Al_2O_3/ 5 nm HfO_2 dielectric, and a 40 nm TiN gate. The measurement was performed with V_{DS} = 0.5 V.
2023	[49]	120	7.5×10^1	$Ge_{0.922}Sn_{0.078}$	Vertical GAA n-FET with a NW diameter of 50nm and gate length of 70 nm; The dielectric is $GeSnO_x$/1 nm Al_2O_3/ 5 nm HfO_2, and the gate material is 40 nm TiN. The measurement was performed with V_{DS} = 0.5V.
2019	[297]	120	2×10^4	$Ge_{0.95}Sn_{0.05}$	Lateral $Ge_{0.95}Sn_{0.05}$OI n-FinFET array (5 fins) with a fin width of 20 nm, fin height of 50 nm, a gate dielectric of 4 nm HfO_2, and a Mo/W gate. The measurement was performed with V_{DS} = 0.5 V.
		160	5×10^4	$Ge_{0.95}Sn_{0.05}$	Lateral $Ge_{0.95}Sn_{0.05}$OI n-TFET array (5 fins) with a fin width of 20 nm, fin height of 50 nm, a gate dielectric of 4 nm HfO_2, and a Mo/W gate. The measurement was performed with V_{DS} = 0.5 V.
2017	[279]	250	6×10^2	$Ge_{0.92}Sn_{0.08}$ on Ge-buffered SOI	$Ge_{0.92}Sn_{0.08}$ inversion mode n-FinFETs with a fin width between 40 nm and 100 nm and $Ge_{0.92}Sn_{0.08}$ height of 50 nm. The gate dielectric is $GeSnO_x$ + Al_2O_3, and a TiN top-gate was used. The measurement was performed with V_{DS} = 0.5 V.
2015	[298]	400	1×10^4	$Ge_{0.955}Sn_{0.045}$ on Ge	Planar $Ge_{0.955}Sn_{0.045}$ n-MOSFETs with a channel width of 80 µm and length of 20 µm. The dielectric is $GeSnO_x$ / 20 nm Al_2O_3, and TaN is used as the top-gate. The measurement was performed with V_{DS} = 0.5 V.
2012	[296]	128	1.5×10^4	$Ge_{0.976}Sn_{0.024}$ on Ge	Planar $Ge_{0.976}Sn_{0.024}$ n-MOSFETs with a gate length of 6.5µm. The dielectric is $GeSnO_2$ and 6 nm Al_2O_3, and TaN was used as gate metal. The measurement was performed with V_{DS} = 0.5 V.

2012	[258]	70	9.1×10^4	Si	Lateral SOI JNT with an n-type doping concentration of P with $n_{e^-} = 4 \times 10^{19}$ cm^{-3}. The vertical NW height is $d_{NW} = 9$ nm, and the gate length is $W_{TG} = 13$ nm. A 2.3 nm HfSiON (EOT ≈ 1.2 nm) dielectric and a top-gate with 5 nm TiN and 50 nm polysilicon were used. Measured at $V_{DS} = 0.9$V

8.27 Annealing setup description

Flash lamp annealing (FLA) and pulse laser annealing (PLA) are the methods used intensively in this thesis. The schematics of both methods are shown in Fig. 8.27 - 1 a) and b).

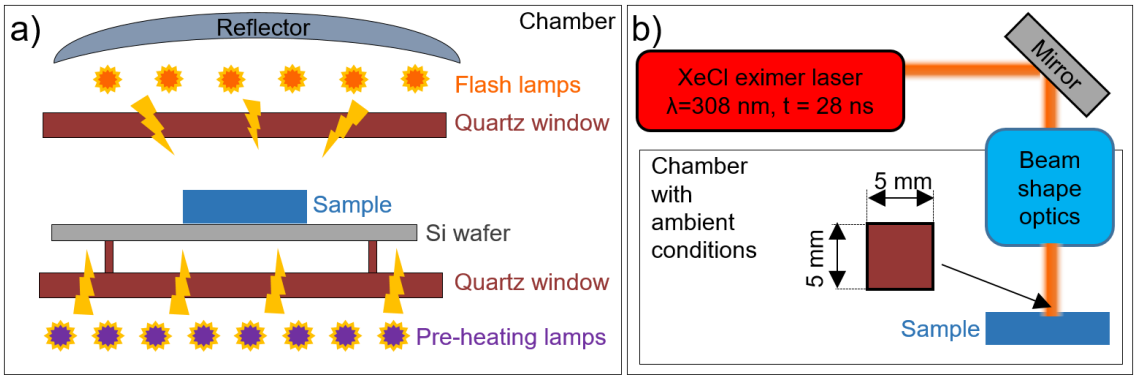

Fig. 8.27 - 1: Schematically shown setups for FLA a) and PLA b).

Publication list

Publications published until thesis submission:

- G.X. Zhang, **O. Steuer**, R. Li, Y. Cheng, R. Hübner, M. Helm, S.Q. Zhou, Y.F. Liu, S. Prucnal, Al-delta-doped ZnO films made by atomic layer deposition and flash-lamp annealing for low-emissivity coating, Applied Surface Science 648 (2024). https://doi.org/10.1016/j.apsusc.2023.159046
- **O. Steuer**, M.O. Liedke, M. Butterling, D. Schwarz, J. Schulze, Z. Li, A. Wagner, I.A. Fischer, R. Hubner, S. Zhou, M. Helm, G. Cuniberti, Y.M. Georgiev, S. Prucnal, Evolution of point defects in pulsed-laser-melted Ge(1-x)Sn(x)probed by positron annihilation lifetime spectroscopy, J Phys Condens Matter 36 (2023) 085701. https://doi.org/10.1088/1361-648X/ad0a10
- Y. Li, **O. Steuer**, K. Lin, F. Samad, D. Sokolova, A. Erbe, M. Helm, S. Zhou, S. Prucnal, Influence of Dielectric Capping on the Optical Properties of Two-Dimensional Transition-Metal Dichalcogenides: Implications for Nano-Optoelectronics, ACS Applied Optical Materials 1 (2023) 1733-1741. https://doi.org/10.1021/acsaom.3c00296
- D. Scheffler, **O. Steuer**, S. Zhou, L. Siegl, S.T.B. Goennenwein, M. Lammel, Aluminium substituted yttrium iron garnet thin films with reduced Curie temperature, Phys Rev Mater 7 (2023). https://doi.org/10.1103/PhysRevMaterials.7.094405
- S. Wen, M.S. Shaikh, **O. Steuer**, S. Prucnal, J. Grenzer, R. Hübner, M. Turek, K. Pyszniak, S. Reiter, I.A. Fischer, Y.M. Georgiev, M. Helm, S. Wu, J.-W. Luo, S. Zhou, Y. Berencén, Room-temperature extended short-wave infrared GeSn photodetectors realized by ion beam techniques, Appl Phys Lett 123 (2023) 081109. https://doi.org/10.1063/5.0166799
- F. Berkmann, **O. Steuer**, F. Ganss, S. Prucnal, D. Schwarz, I.A. Fischer, J. Schulze, Sharp MIR plasmonic modes in gratings made of heavily doped pulsed laser-melted Ge1-xSnx, Optical Materials Express 13 (2023) 752-763. https://doi.org/10.1364/OME.479637
- **O. Steuer**, D. Schwarz, M. Oehme, J. Schulze, H. Maczko, R. Kudrawiec, I.A. Fischer, R. Heller, R. Hubner, M.M. Khan, Y.M. Georgiev, S. Zhou, M. Helm, S. Prucnal, Band-gap and strain engineering in GeSn alloys using post-growth pulsed laser melting, J Phys Condens Matter 35 (2022) 055302. https://doi.org/10.1088/1361-648X/aca3ea
- A. Echresh, S. Prucnal, Z. Li, R. Hübner, F. Ganss, **O. Steuer**, F. Bärwolf, S. Jazavandi Ghamsari, M. Helm, S. Zhou, A. Erbe, L. Rebohle, Y.M. Georgiev, Fabrication of Highly n-Type-Doped Germanium Nanowires and Ohmic Contacts Using Ion Implantation and Flash Lamp Annealing, ACS Applied Electronic Materials 4 (2022) 5256-5266. https://doi.org/10.1021/acsaelm.2c00952

Talks and Posters:

- **O. Steuer**. Group IV semiconductor alloys: Fabrication and characterization of GeSn and SiGeSn alloys. Statusvortrag TU Dresden, 18.01.2024 (Talk)
- **O.Steuer**, D. Schwarz, M. Oehme, F. Ganss, M. M. Khan, Y Cheng, L. Rebohle, S. Zhou, M. Helm, G. Cuniberti, Y. Georgiev, S. Prucnal. Post growth thermal treatments of $Si_{1-x-y}Ge_xSn_y$ alloys. E-MRS 2023 Spring Meeting, 29. Mai - 02 June 2023, Strasbourg, France (Talk Young Researchers Award)
- **O.Steuer**, D. Schwarz, M. Oehme, F. Ganss, M. M. Khan, Y Cheng, L. Rebohle, S. Zhou, M. Helm, G. Cuniberti, Y. Georgiev, S. Prucnal. Post growth thermal treatments of Silicon-Germanium-Tin-on-insulator alloys. E-MRS 2023 Spring Meeting, 29. Mai - 02 June 2023, Strasbourg, France (Poster)
- **O.Steuer**, D. Schwarz, M. Oehme, F. Ganss, M. M. Khan, Y Cheng, L. Rebohle, S. Zhou, M. Helm, G. Cuniberti, Y. Georgiev, S. Prucnal. Post growth thermal treatments of $Ge_{1-x}Sn_x$ alloys. 3rd Joint International Conference on Silicon Epitaxy and Heterostructures & International SiGe Technology and Device Meeting (ICSi-ISTDM), 21-25 May 2023 Como, Italy (Poster)
- **O. Steuer**, D. Schwarz, M. Oehme, J. Schulze, H. Mączko, R. Kudrawiec, I. A. Fischer, R. Heller, R. Hübner, M. M. Khan, Y. M. Georgiev, S. Zhou, M. Helm, S. Prucnal. Band-gap and strain engineering in GeSn alloys using post-growth pulsed laser melting. DPG-Tagung 2022, 04. - 09.September 2022, Regensburg, Germany (Talk)
- **O. Steuer**, D. Schwarz, M. Oehme, J. Schulze, H. Mączko, R. Kudrawiec, I. A. Fischer, R. Heller, R. Hübner, M. M. Khan, Y. M. Georgiev, S. Zhou, M. Helm, S. Prucnal. Defect evolution in GeSn alloys using post-growth pulsed laser melting. NanoNet+ Annual Workshop 2022, 04.- 06. October 2022, Görlitz, Germany (talk)
- **O Steuer**, M. M. Khan, D. Schwarz, R. Hübner, C. Fowley, A. Erbe, S. Zhou, S. Prucnal, Y. Georgiev. Fabrication and Electrical Characterization of Germanium-Tin-on-insulator Junction–Less Nanowire Transistors. NanoNet+ Annual Workshop 2022, 04. - 06. October 2022, Görlitz, Germany (poster)
- **O. Steuer**, D. Schwarz, M. Oehme, J. Schulze, H. Mączko, R. Kudrawiec, I. A. Fischer, R. Heller, R. Hübner, M. M. Khan, Y. M. Georgiev, S. Zhou, M. Helm, S. Prucnal. Band-gap and strain engineering in GeSn alloys using post-growth pulsed laser melting. EMRS Spring Meeting-2021, 31st May to 3rd June 2021, Virtual conference (Talk)

Selbstständigkeitserklärung

Ich erkläre hiermit, dass ich die vorliegende Arbeit mit dem Thema:

Fabrication, characterization and application of $Si_{1-x-y}Ge_xSn_y$ alloys

selbständig und ohne Benutzung anderer als der angegebenen Hilfsmittel angefertigt habe; die aus fremden Werken wörtlich oder sinngemäß übernommenen Gedanken sind unter Angabe der Quellen gekennzeichnet.

Ich versichere, dass ich bisher keine Prüfungsarbeit mit gleichem oder ähnlichem Thema bei einer Prüfungsbehörde oder anderen Hochschule vorgelegt habe.

Dresden, den 13. Februar 2024

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Oliver Steuer