3rd Thesis Advisory Committee (TAC) Meeting

1) Theses update
2) Post growth thermal treatment of $Si_{1-x-y}Ge_ySn_x$ OI
3) 10 theses about the theses

03.05.2023

Oliver Steuer

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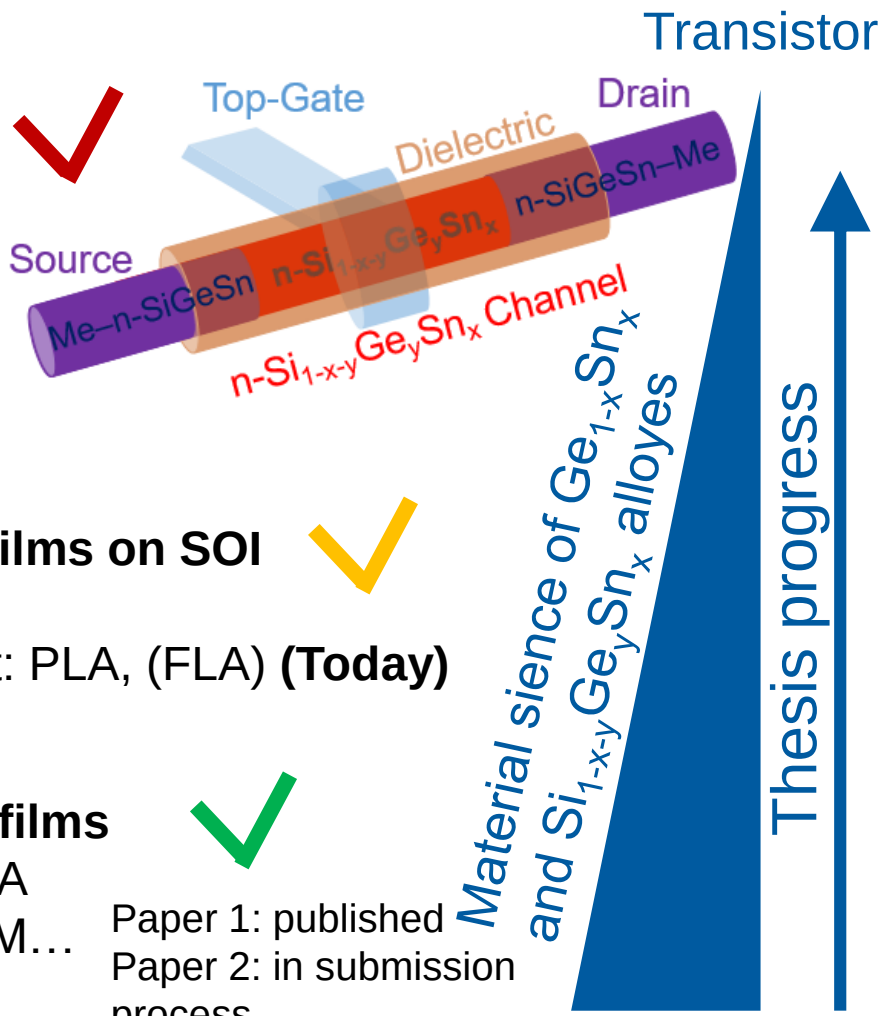
GEFÖRDERT VOM
Bundesministerium für Bildung und Forschung

Update

Title: Fabrication and characterisation of $Si_{1-x-y}Ge_ySn_x$ alloys

III. Fabrication and characterisation of junction less transistors

- Device fabrication
- Influence of post growth PLA on device performance **(Today)**



II. Fabrication of GeSn and SiGeSn **thin films on SOI**

- Ion implantation + FLA
- MBE and post growth thermal treatment: PLA, (FLA) **(Today)**

I. Fabrication of GeSn and SiGeSn **thick films**

- Post growth thermal treatment: FLA, PLA
- Characterisation: RBS, SIMS, XRD, TEM…

Paper 1: published
Paper 2: in submission process

DRESDEN concept SCIENCE AND INNOVATION CAMPUS
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HELMHOLTZ ZENTRUM DRESDEN ROSSENDORF

Outline

- Fabrication and characterisation of $Si_{1-x-y}Ge_ySn_x$ alloys -

Update

Transistor fabrication

- Material analysis $Si_{1-x-y}Ge_xSn_xOI$ -

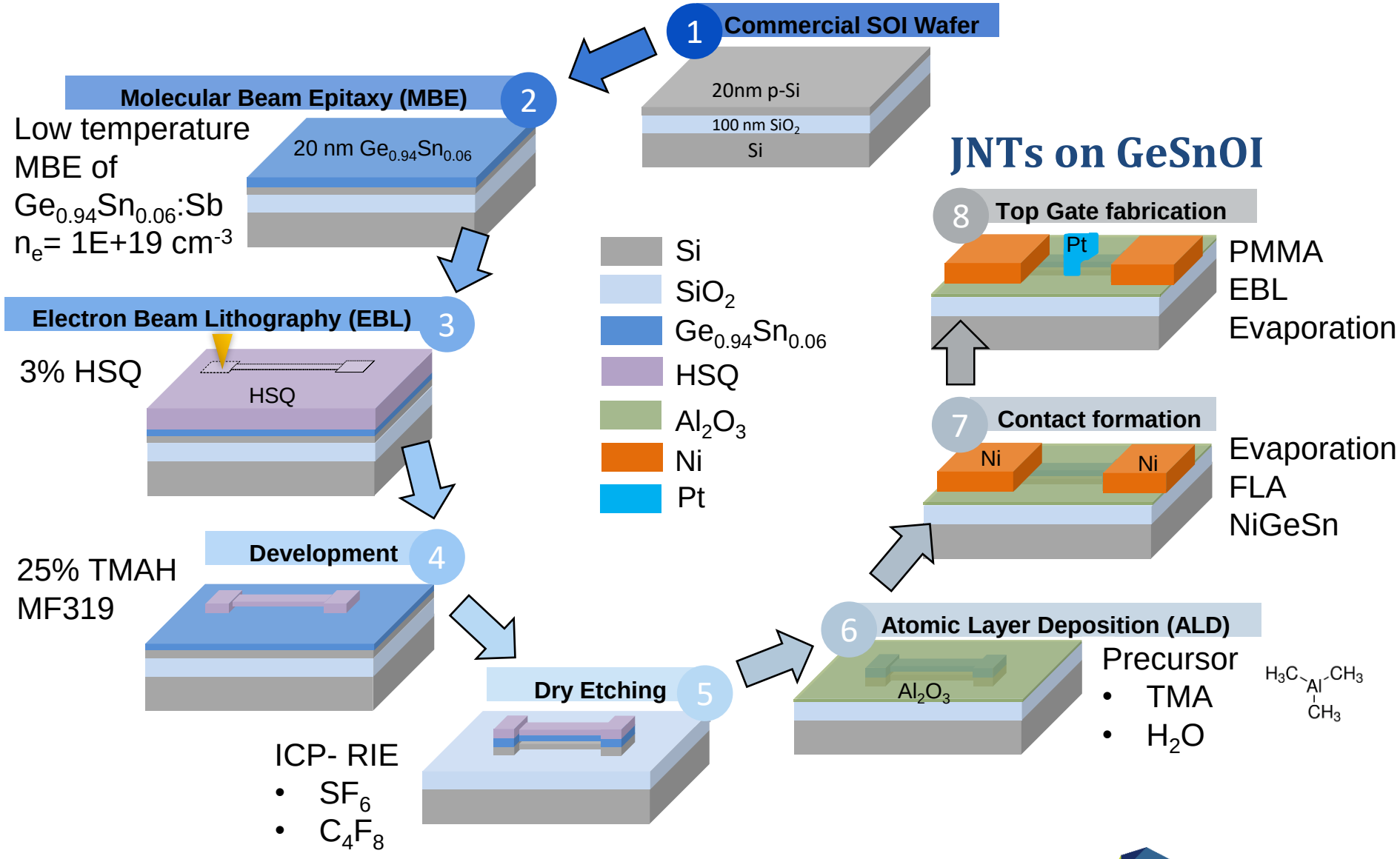
- Device analysis -

- Summary $Si_{1-x-y}Ge_xSn_xOI$ -

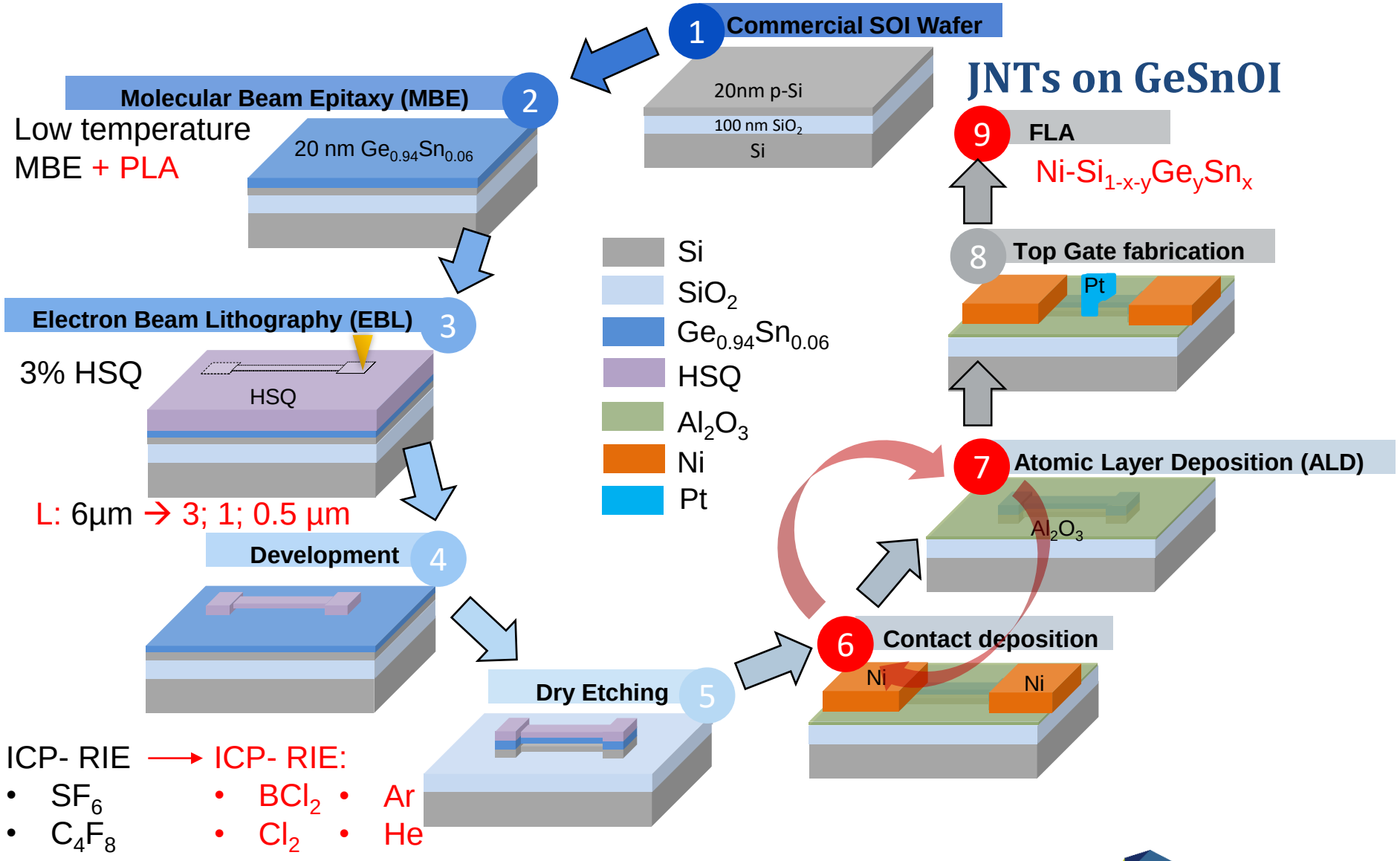
- 10 theses about the theses -

DRESDEN concept

Transistor fabrication – general process flow



Transistor fabrication – general process flow



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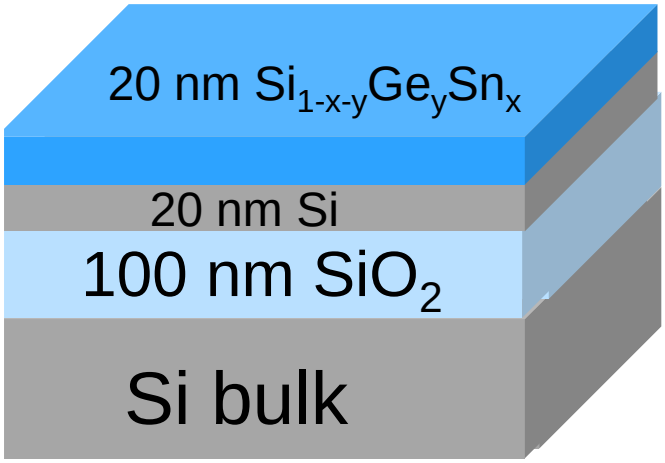
DRESDEN concept

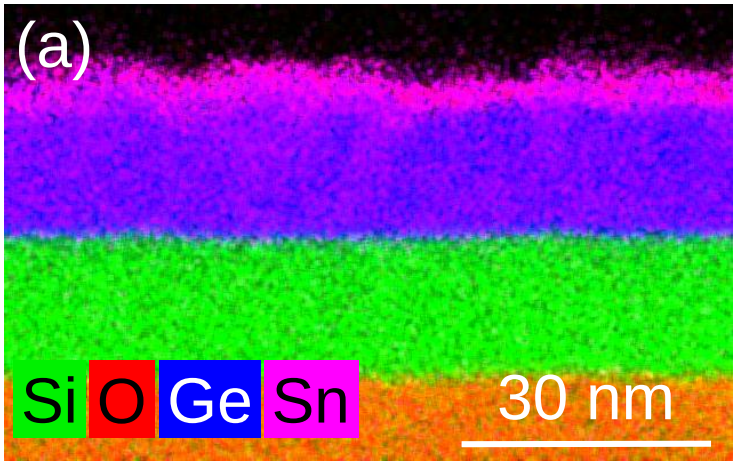
$Si_{1-x-y}Ge_ySn_x$ OI characterisation

As grown: Elemental distribution

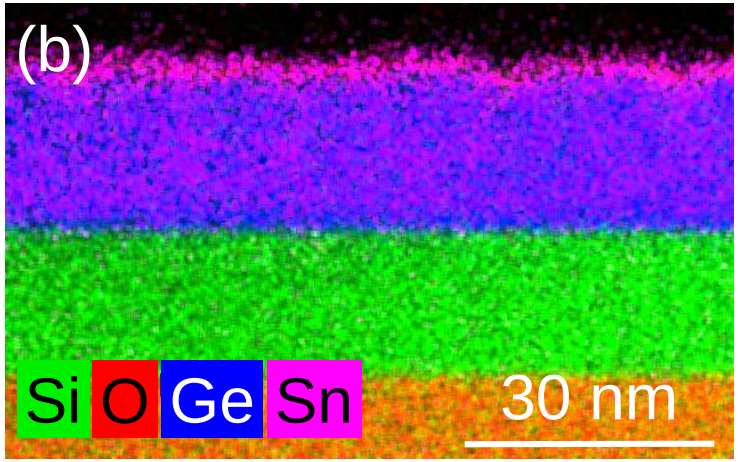
- Targeted layer stack
- No O at $Si_{1-x-y}Ge_ySn_x$ / SOI interface
- Homogeneous Sn distribution
- Slightly inhomogeneous surface with oxides



$Ge_{0.94}Sn_{0.06}$



$Si_{0.14}Ge_{0.80}Sn_{0.06}$

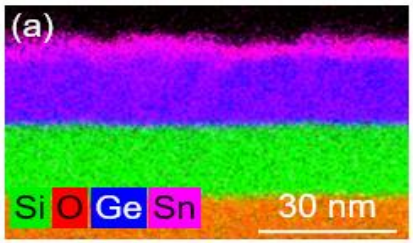


Lattice mismatch Ge on Si: 4.1%

$Si_{1-x-y}Ge_ySn_x$ OI characterisation

As grown: crystal structure: mainly single crystalline

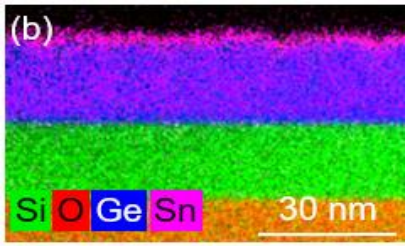
$Ge_{0.94}Sn_{0.06}$

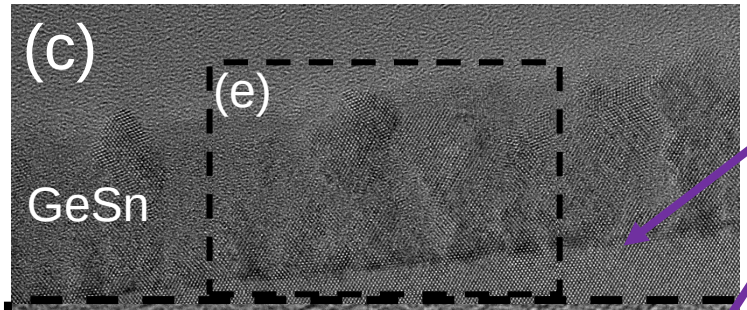


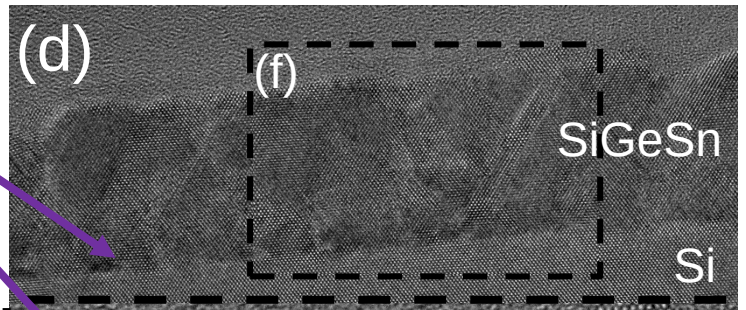
Lattice mismatch:
5.3%
→ strain or defect formation

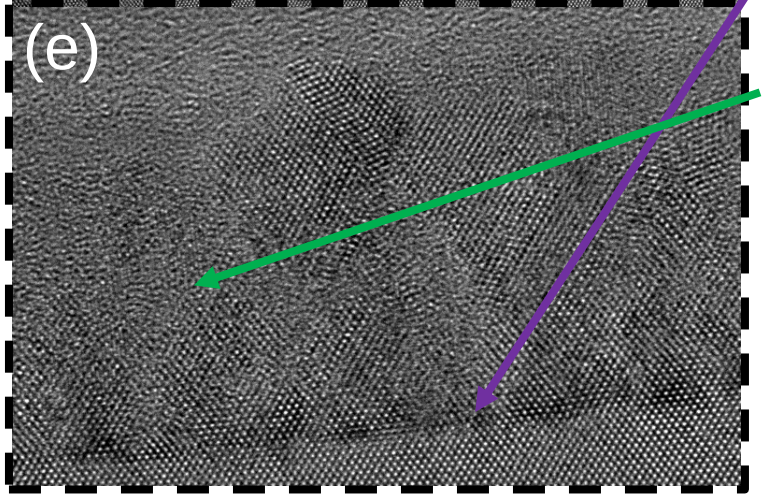
$Si_{0.14}Ge_{0.80}Sn_{0.06}$

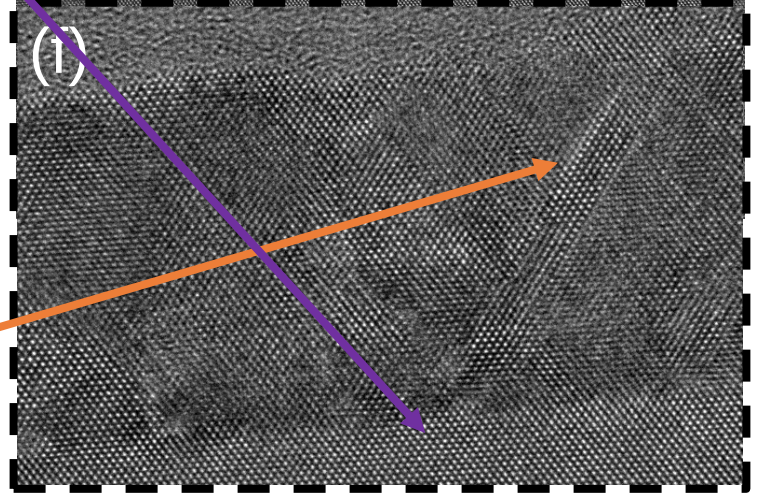
1.8%











Interface
Staking fouls

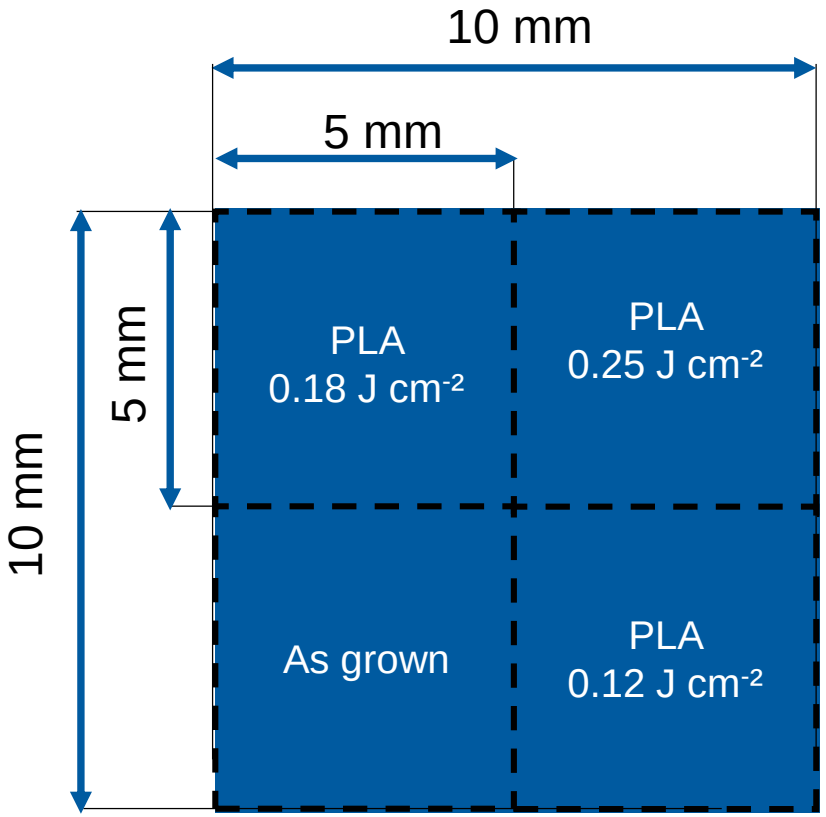
Amorphous
inclusions or
misoriented
grains

Interlayer
Staking fouls

$Si_{1-x-y}Ge_ySn_x$ OI characterisation
Post growth PLA

Experiment:
PLA with 3 different energy densities on one 10x10 mm² sample

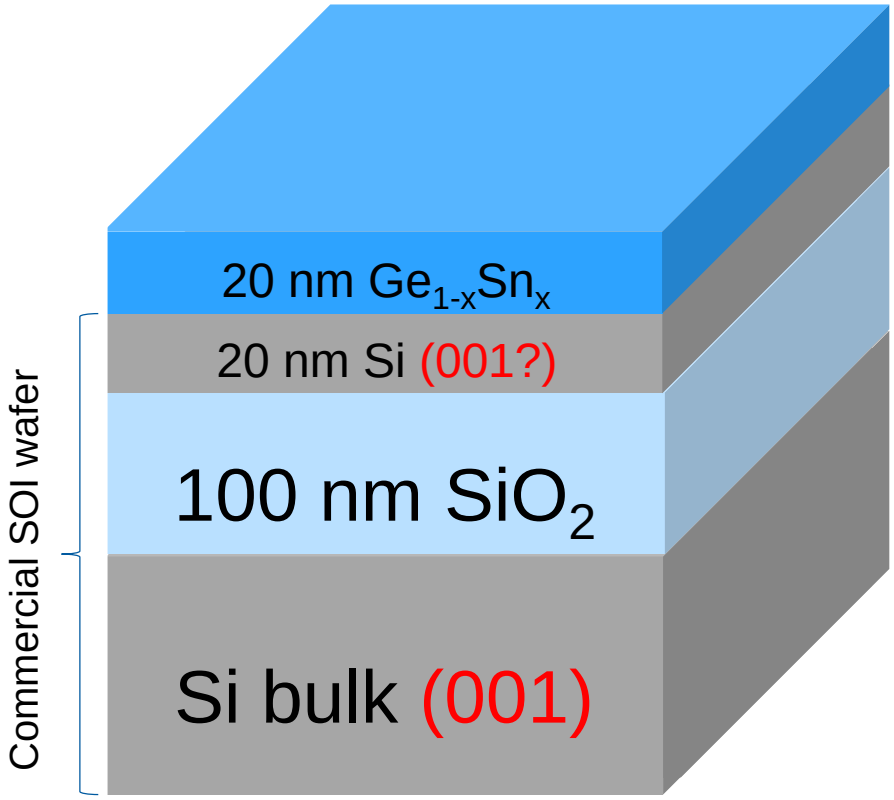
Analysis:
- XRD
- RBS
- µ-Raman
- SIMS
- TEM
- Hall effect



$Si_{1-x-y}Ge_ySn_x$ OI characterisation
Post growth PLA - XRD

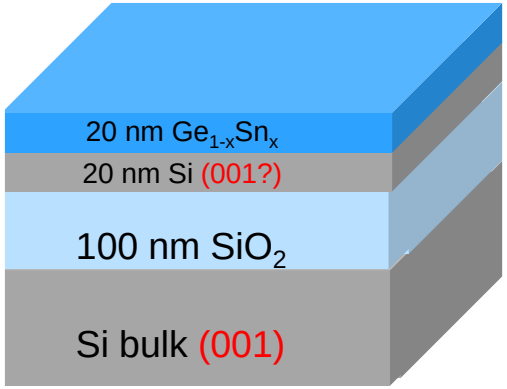
SOI material leads to some challenges:

- Low intensities
- Alignment issues



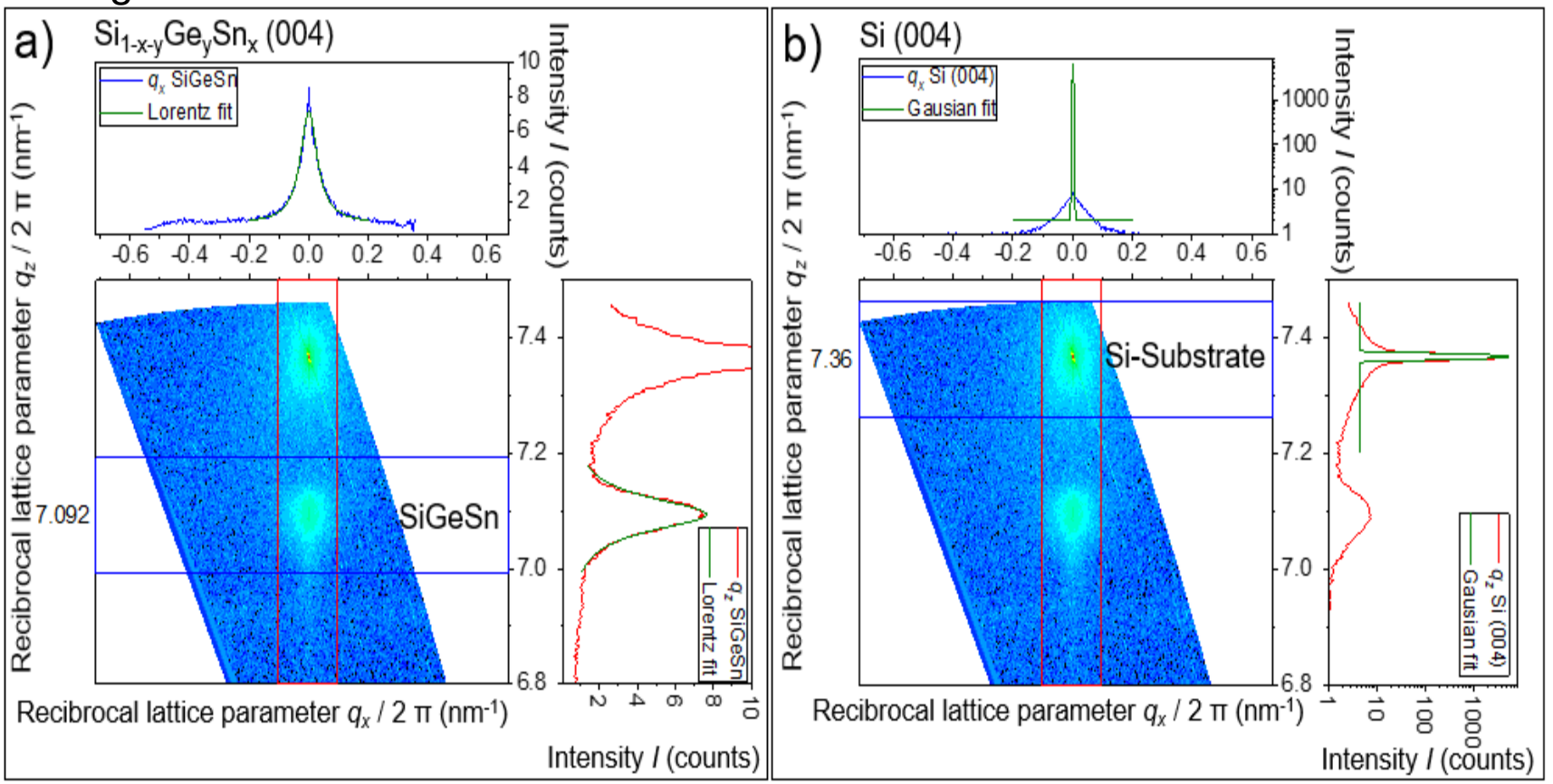
$Si_{1-x-y}Ge_ySn_x$ OI characterisation

Post growth PLA – XRD: RSM (004)



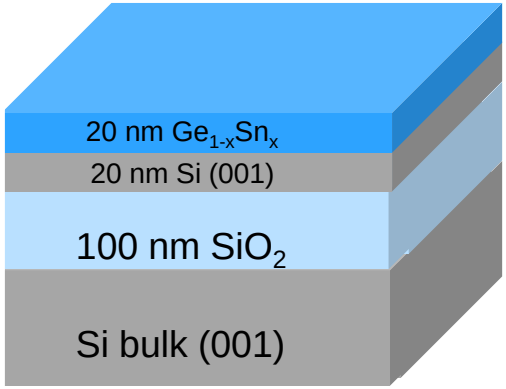
Layer tilt: $\arctan(\delta) = \frac{q_{xSi}}{q_{zSi}} - \frac{q_{xSiGeSn}}{q_{xSiGeSn}}$ ≈ 1E-2° and 1E-5°

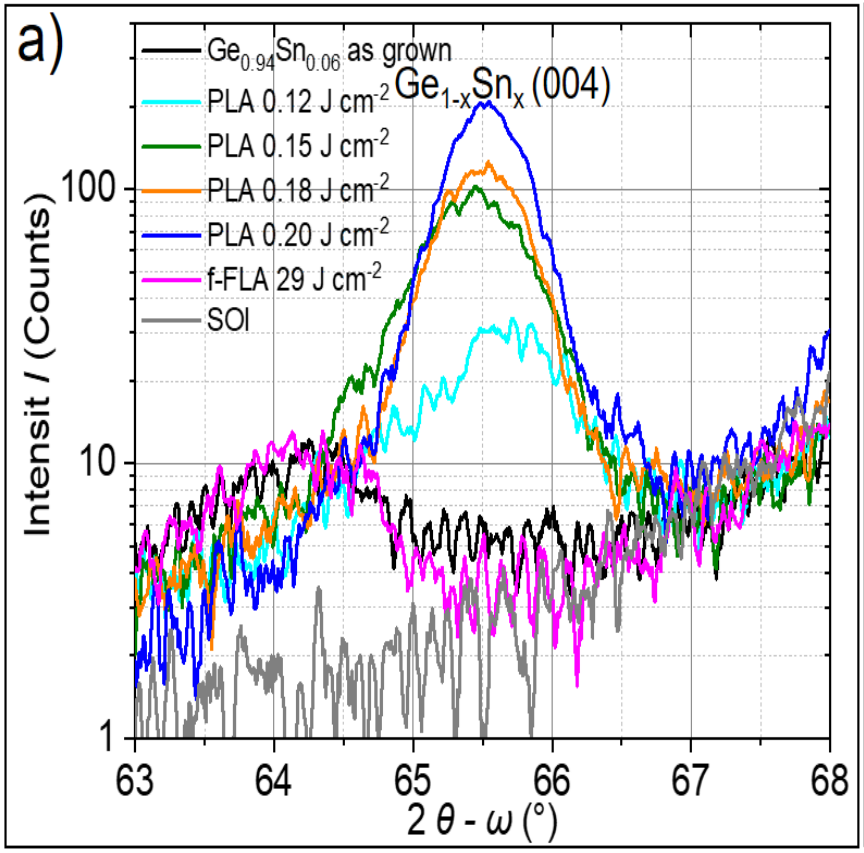
→ Alignment on Si bulk ok

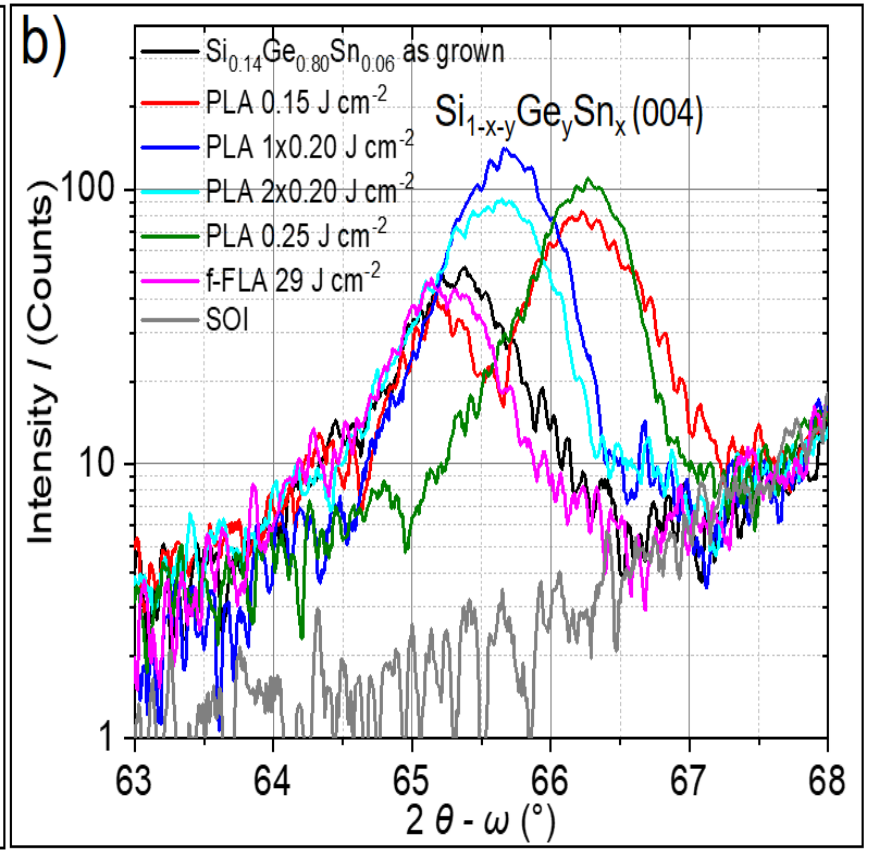


$Si_{1-x-y}Ge_ySn_x$ OI characterisation
Post growth PLA – XRD: HRXRD (004)

- No influence due to FLA
- Higher intensity and peak shift after PLA







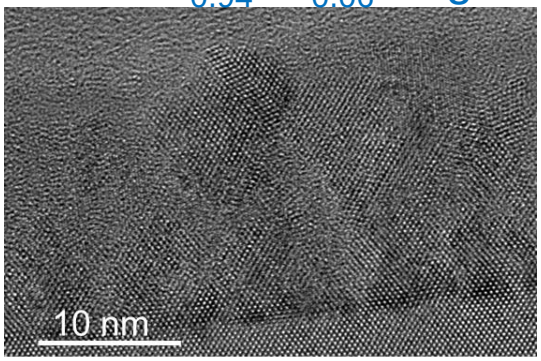
$Si_{1-x-y}Ge_ySn_x$ OI characterisation

Post growth PLA – XRD: RSM (224)

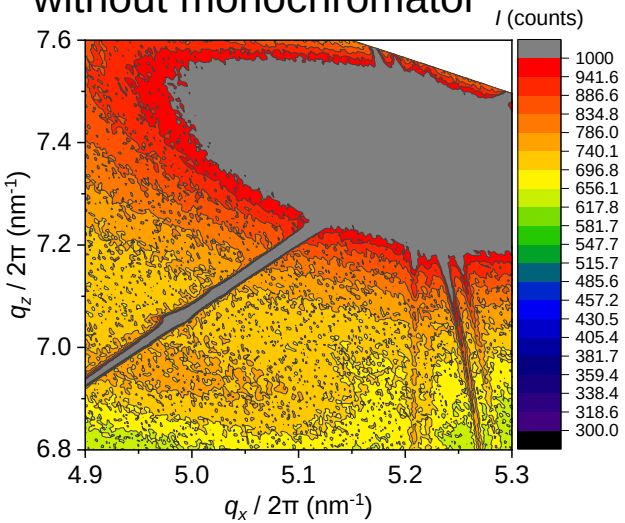
$Ge_{1-x}Sn_xOI$

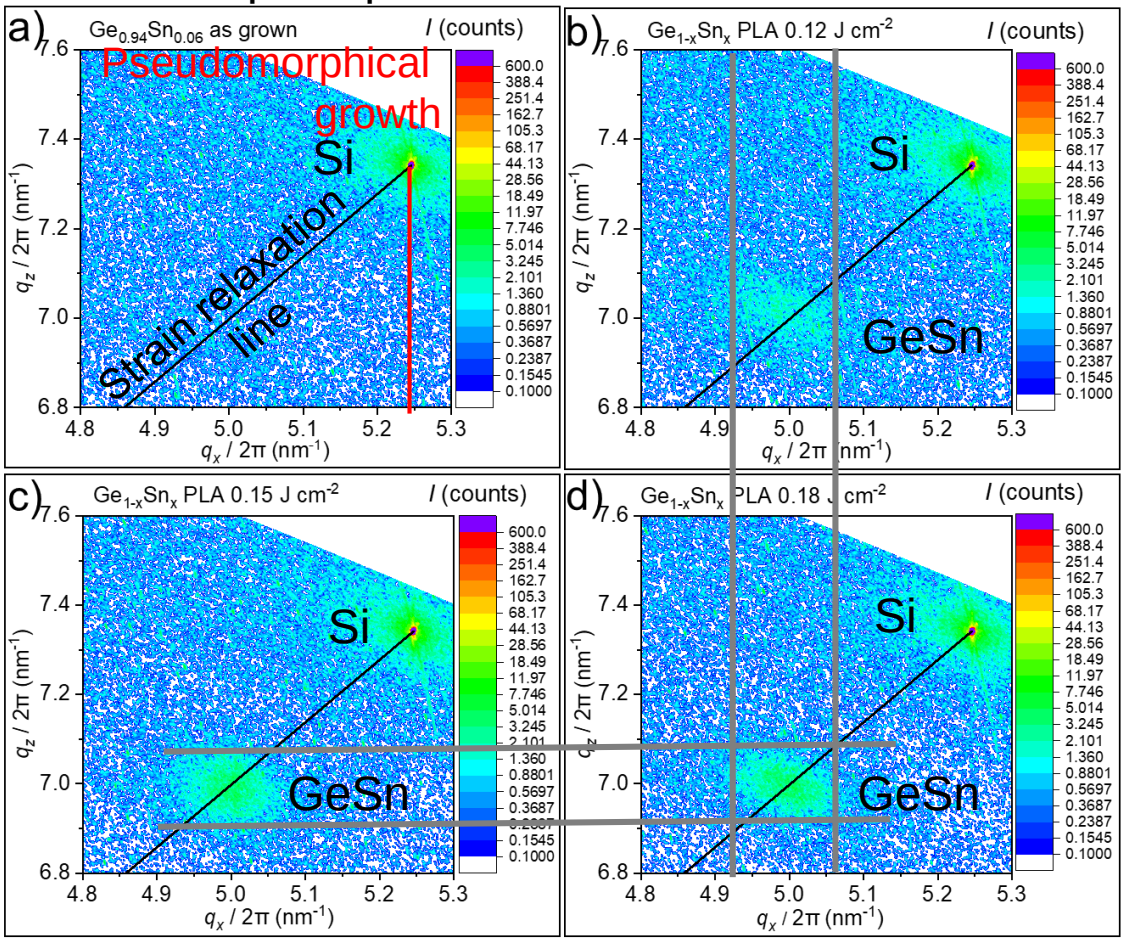
- Almost strain relaxed as grown state
- Recrystallization due to PLA
- Similar peak position

TEM $Ge_{0.94}Sn_{0.06}$ as grown



$Ge_{0.94}Sn_{0.06}$ as grown 1x1 cm², without monochromator



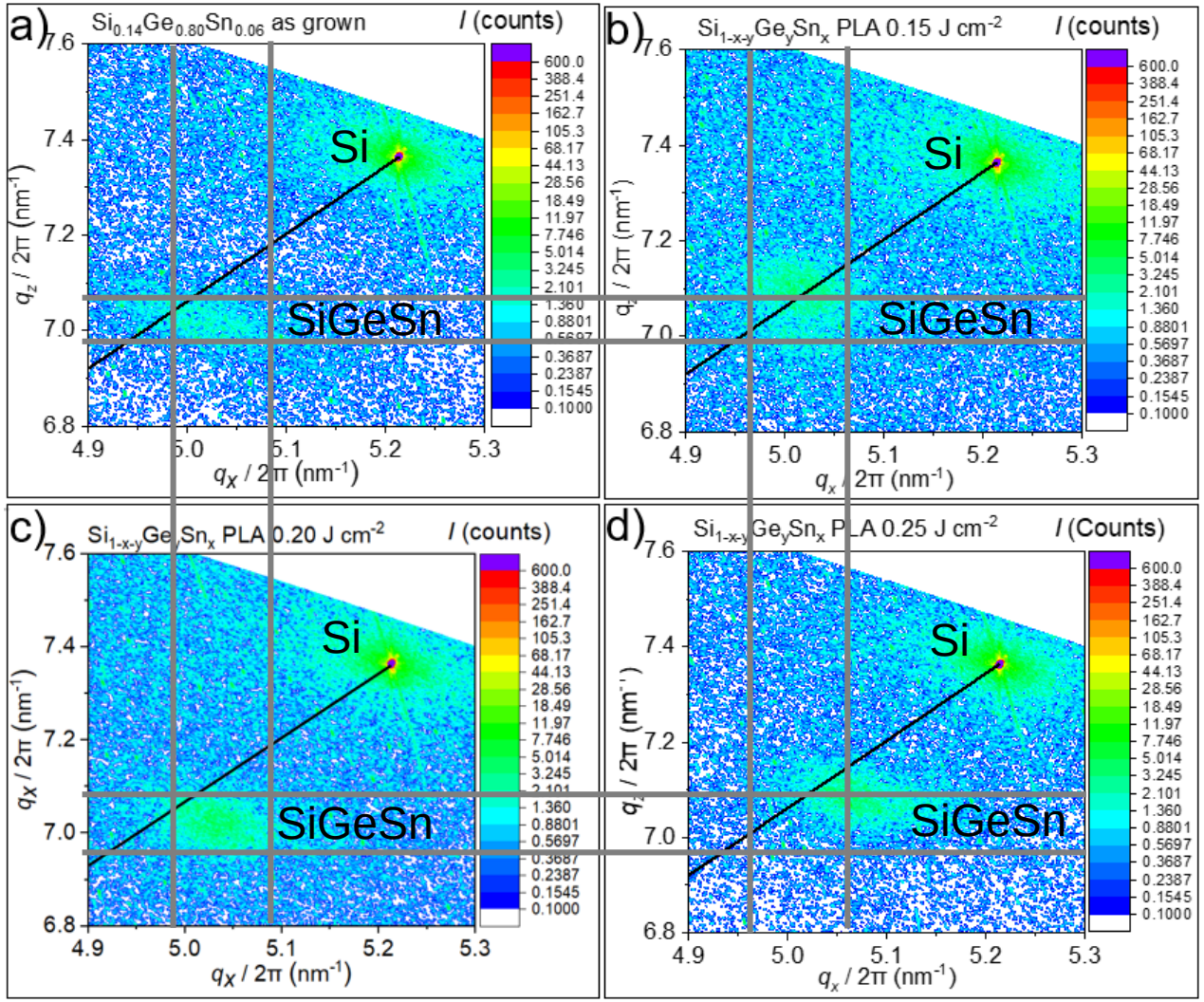


$Si_{1-x-y}Ge_ySn_x$ OI characterisation

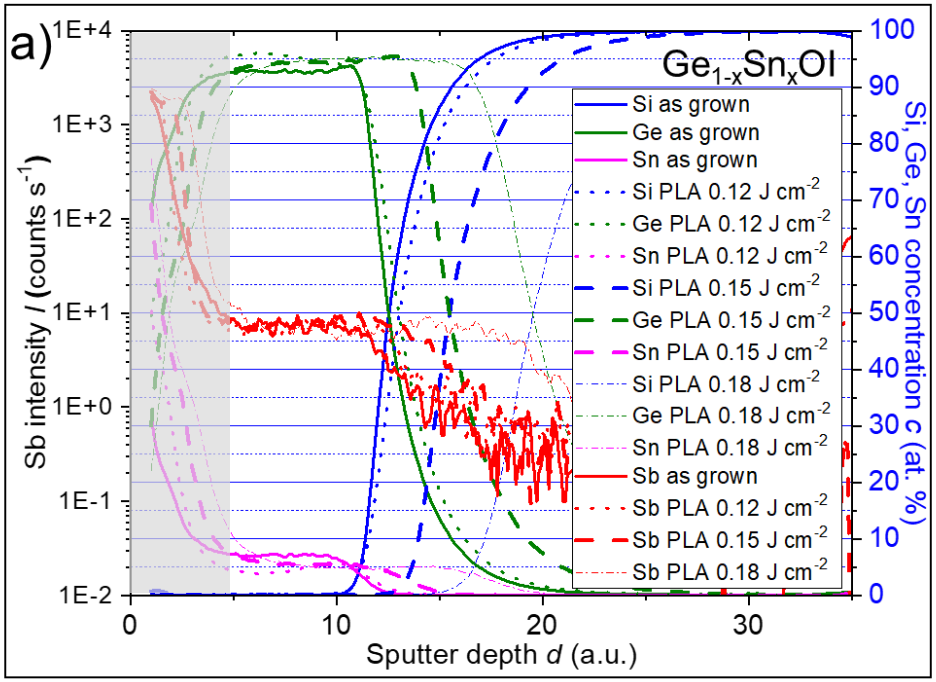
Post growth PLA – XRD: RSM (224)

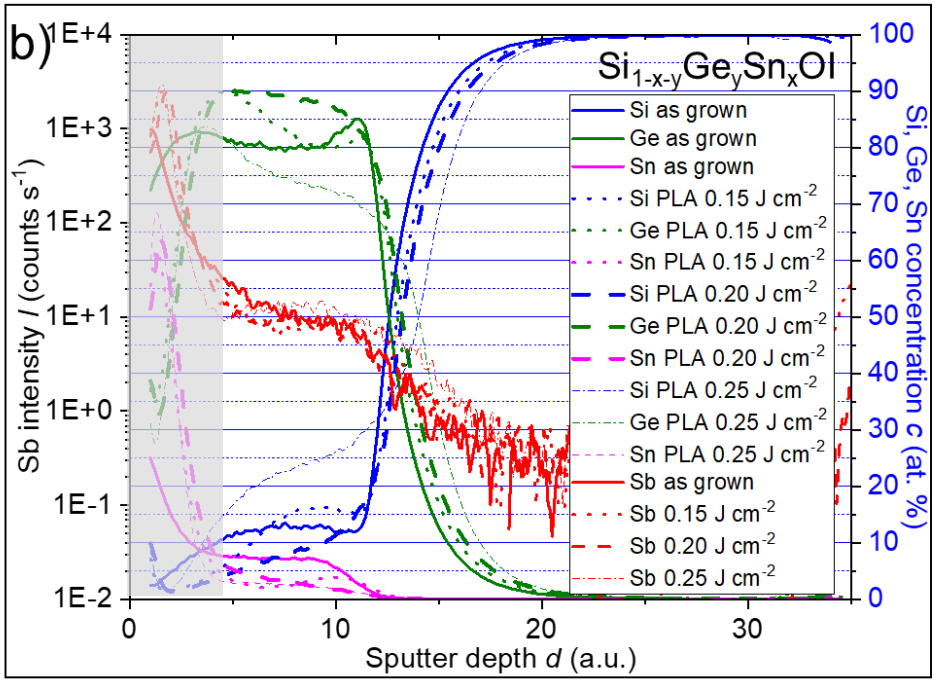
$Si_{1-x-y}Ge_ySn_xOI$

- Slight compressive strained
- Peak shift upwards after PLA 0.15 J cm^{-2}
- PLA > 0,2 shift towards Si
- Next step: Strain calculation



$Si_{1-x-y}Ge_ySn_x$ OI characterisation
Post growth PLA – SIMS





- Shift towards deeper sputter depth due to sputter rate
- Out diffusion of Sn
- Sb concentration almost unaffected

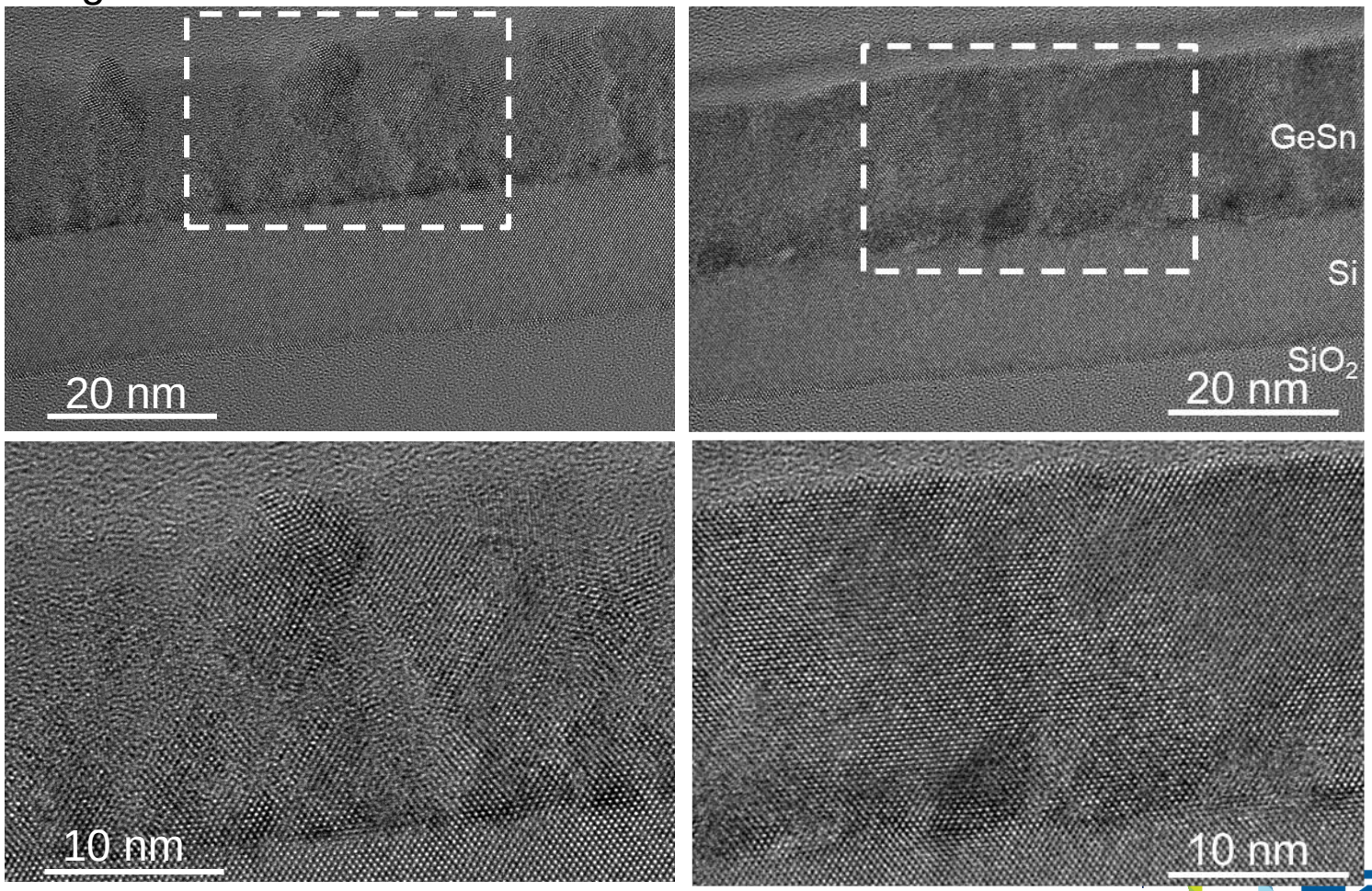
$Si_{1-x-y}Ge_ySn_x$ OI characterisation

Post growth PLA – TEM

$Ge_{1-x}Sn_xOI$

As grown

PLA 0.2 J cm^{-2}



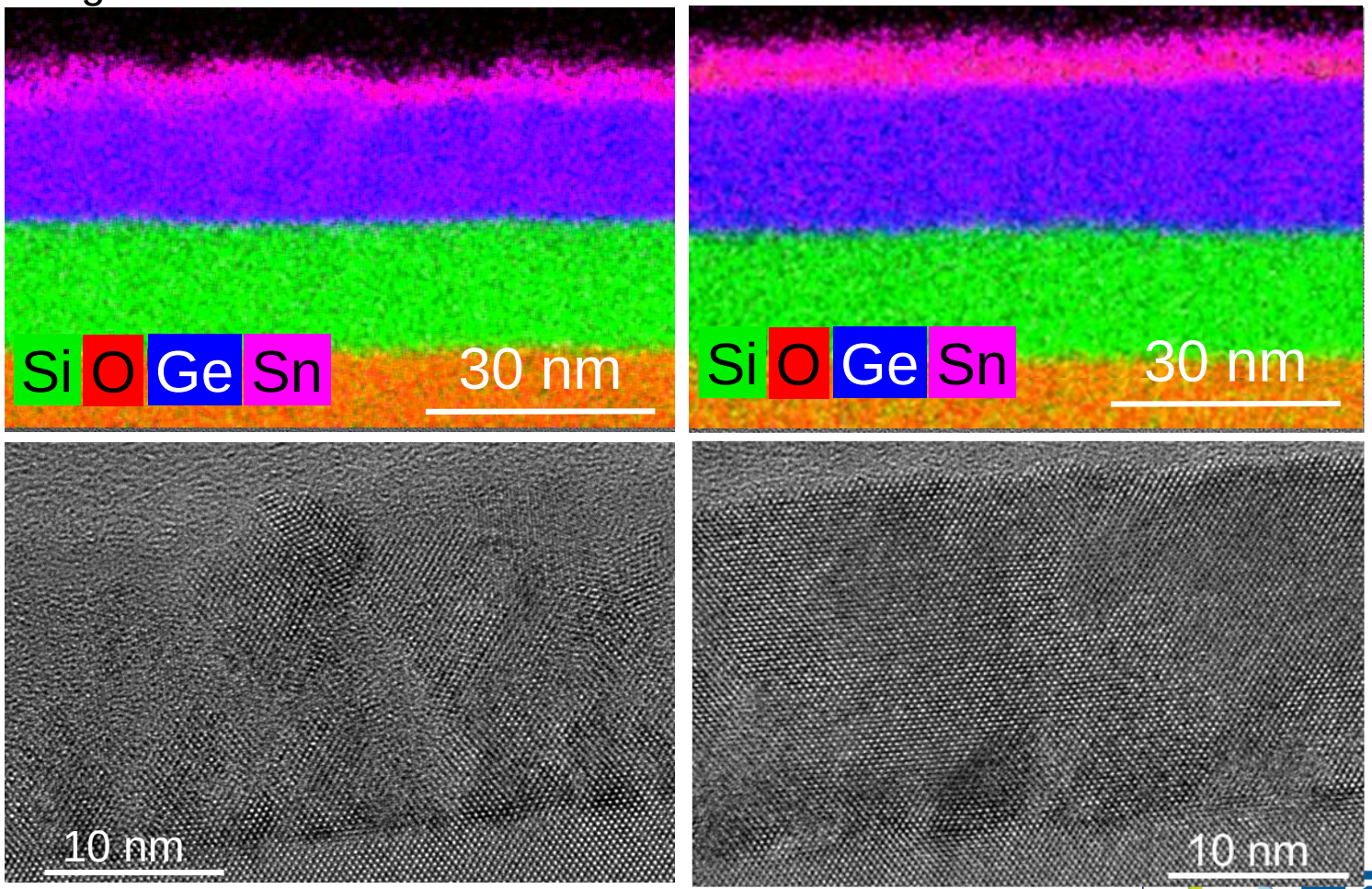
$Si_{1-x-y}Ge_ySn_x$ OI characterisation

Post growth PLA – TEM

$Ge_{1-x}Sn_xOI$

As grown

PLA 0.2 J cm^{-2}



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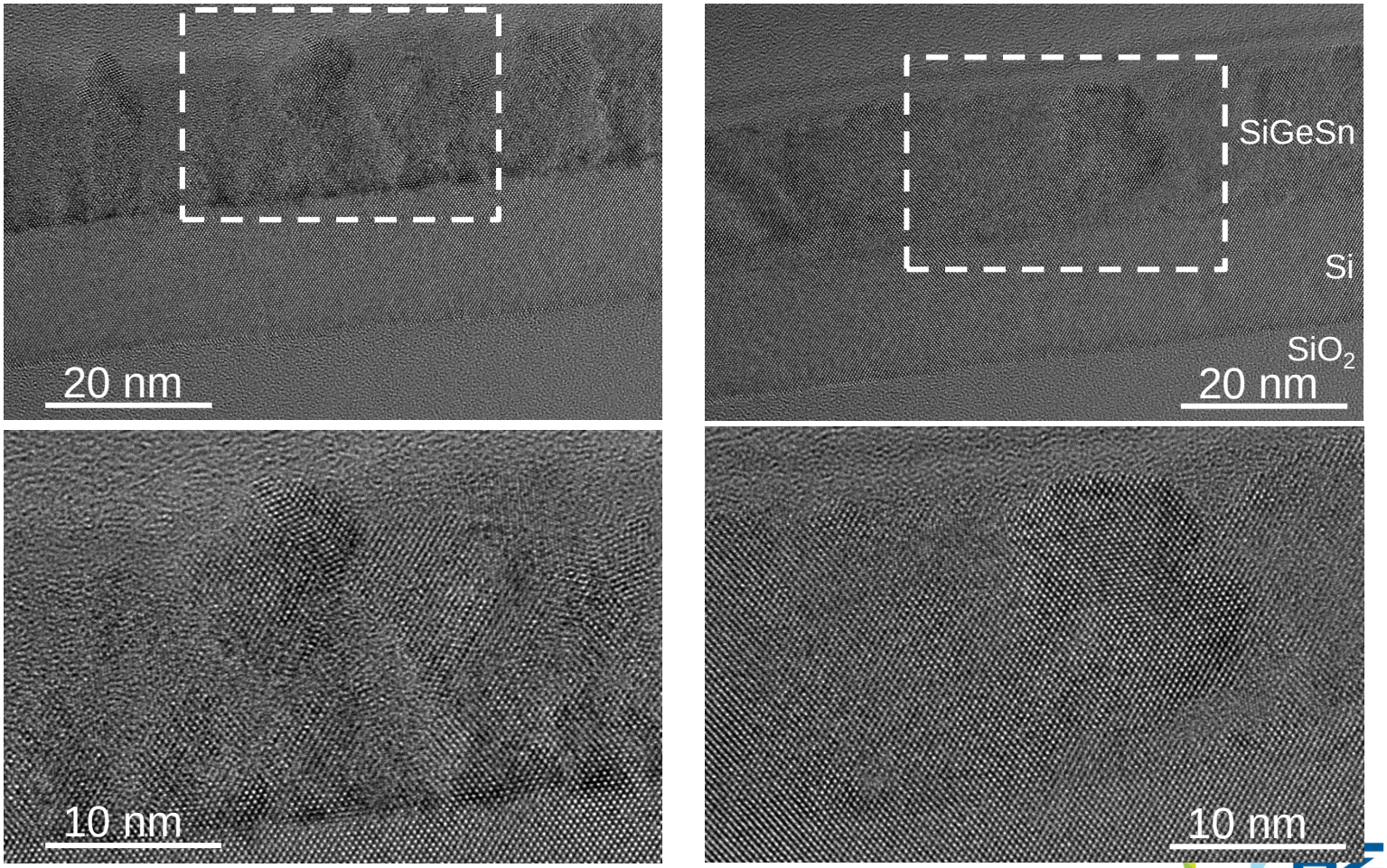
$Si_{1-x-y}Ge_ySn_x$ OI characterisation

Post growth PLA – TEM

$Si_{1-x-y}Ge_ySn_xOI$

As grown

PLA 0.25 J cm^{-2}



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$Si_{1-x-y}Ge_ySn_x$ OI characterisation

Post growth PLA – TEM

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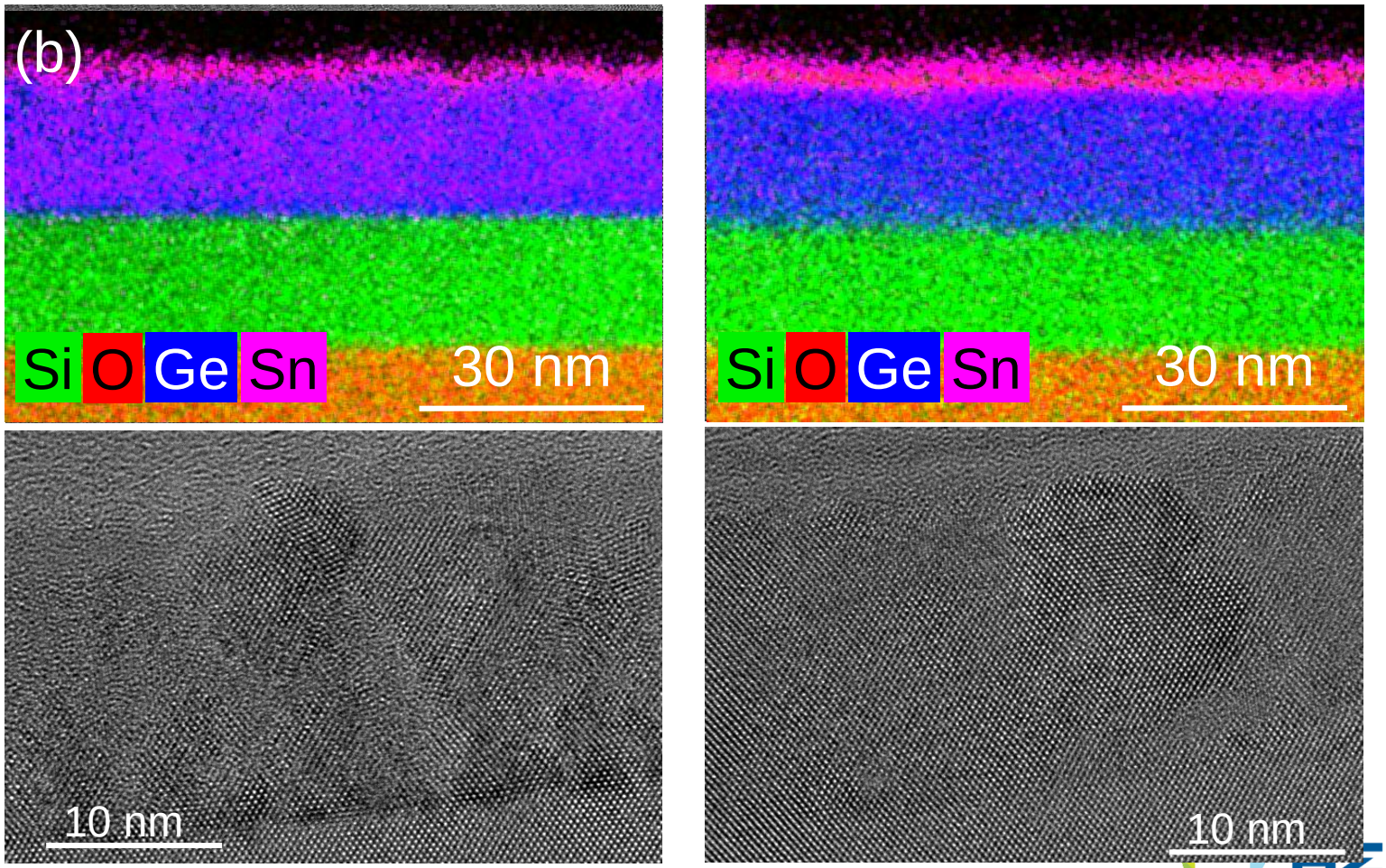
As grown

PLA 0.25 J cm^{-2}



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- Fabrication and characterisation of $Si_{1-x-y}Ge_ySn_x$ alloys -

Update

Transistor fabrication

- Material analysis $Si_{1-x-y}Ge_ySn_xOI$ -

- Device analysis -

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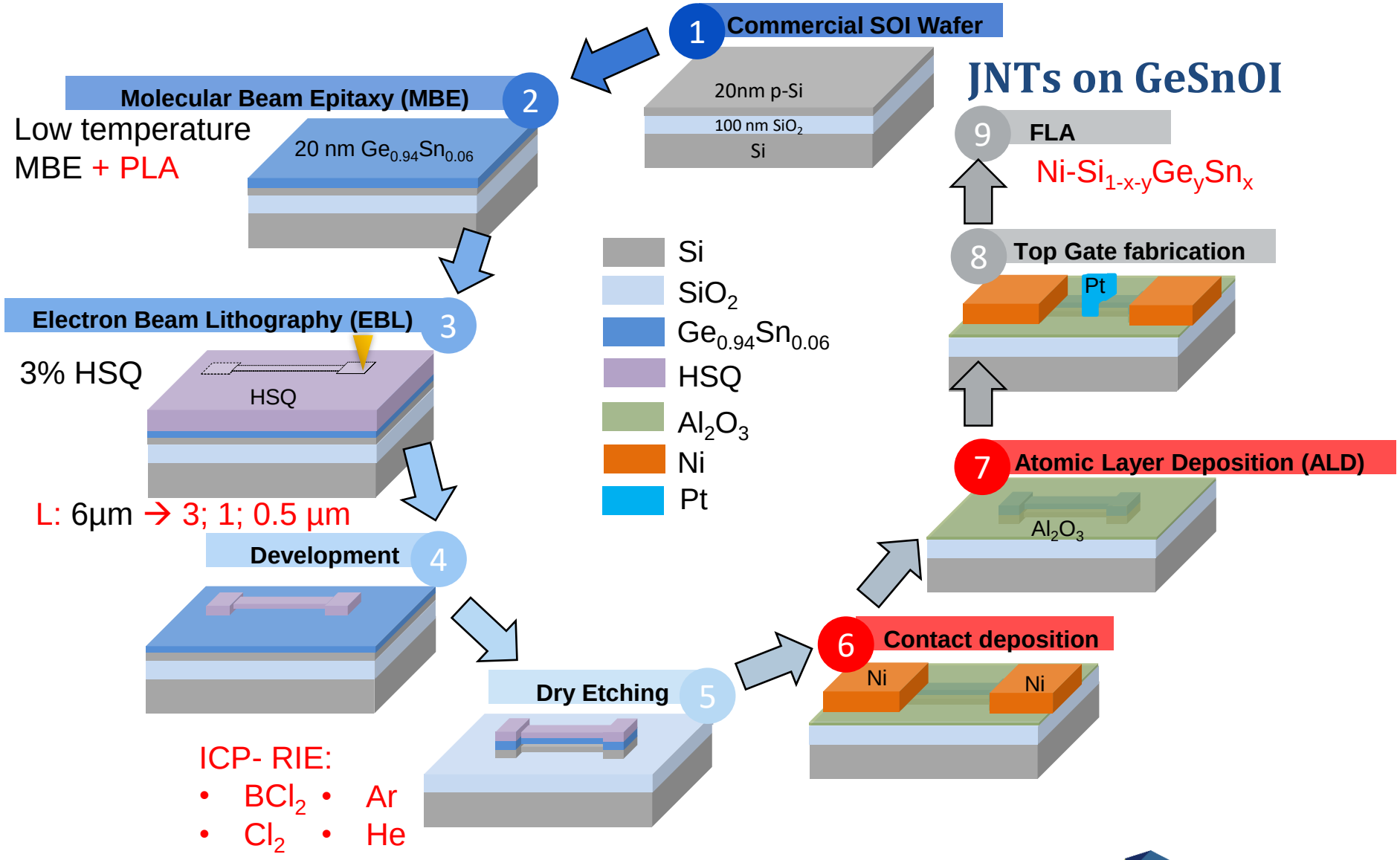
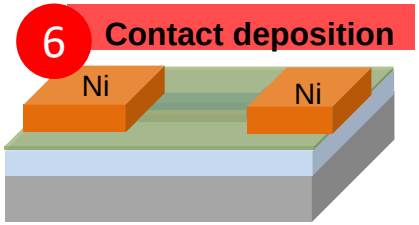
DRESDEN concept

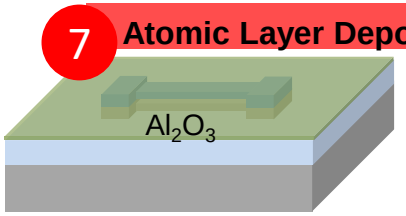
Transistor fabrication – general process flow



Transistor fabrication

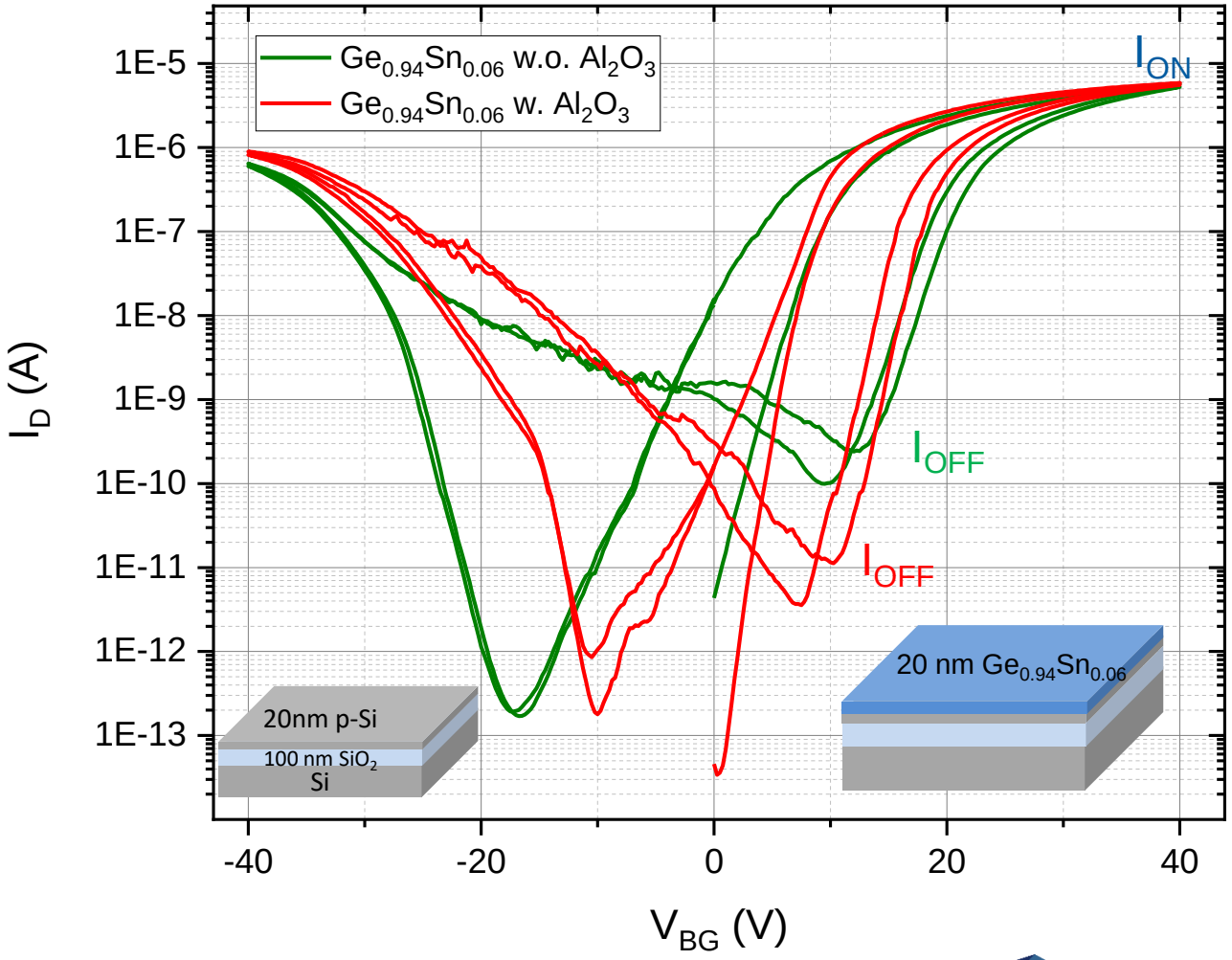
$Ge_{1-x}Sn_xOI$





- Double sweep
- I_{ON} = 6E-6 A
- I_{OFF} = 2E-10 A
- I_{OFF} = 1E-11 A

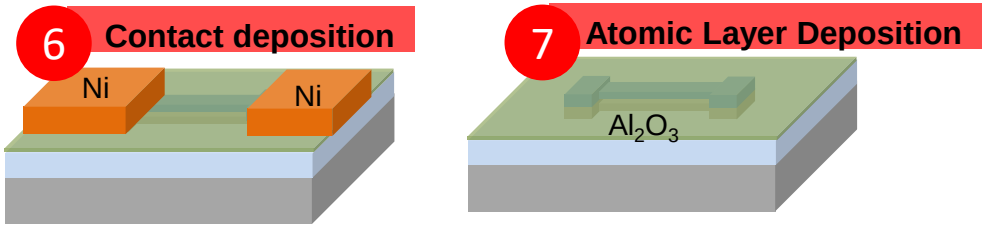
Influence Al_2O_3:
- Hysteresis ↓
- I_{on}/I_{OFF} 6E+5 ↑



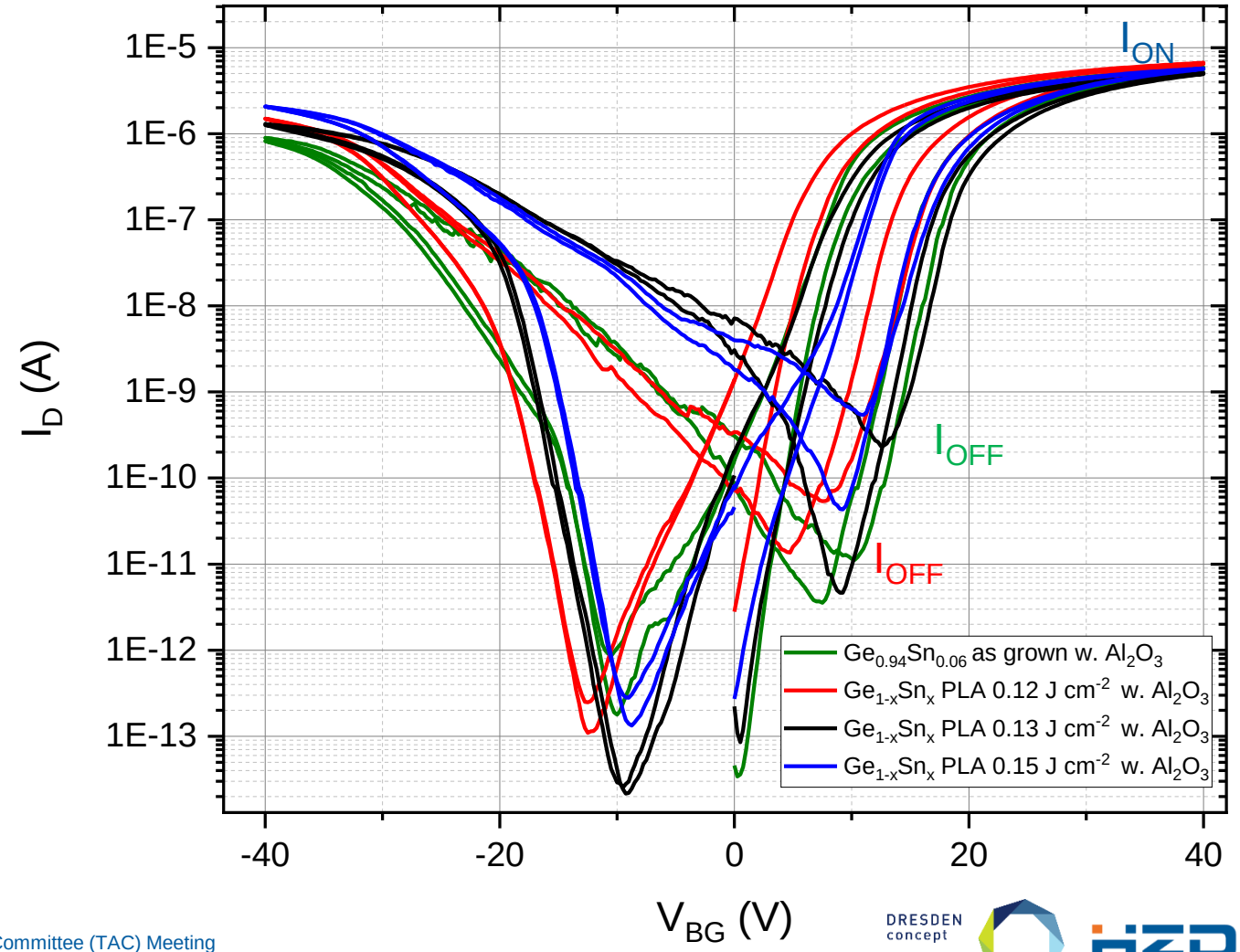
DRESDEN concept SCIENCE AND INNOVATION CAMPUS HZDR

Transistor fabrication

$Ge_{1-x}Sn_xOI$

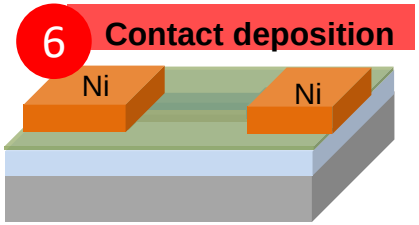


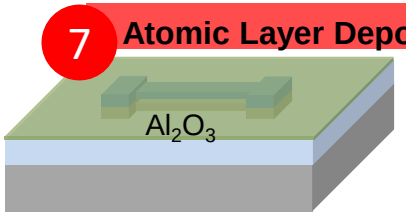
Influence PLA



Transistor fabrication

$Si_{1-x-y}Ge_ySn_xOI$



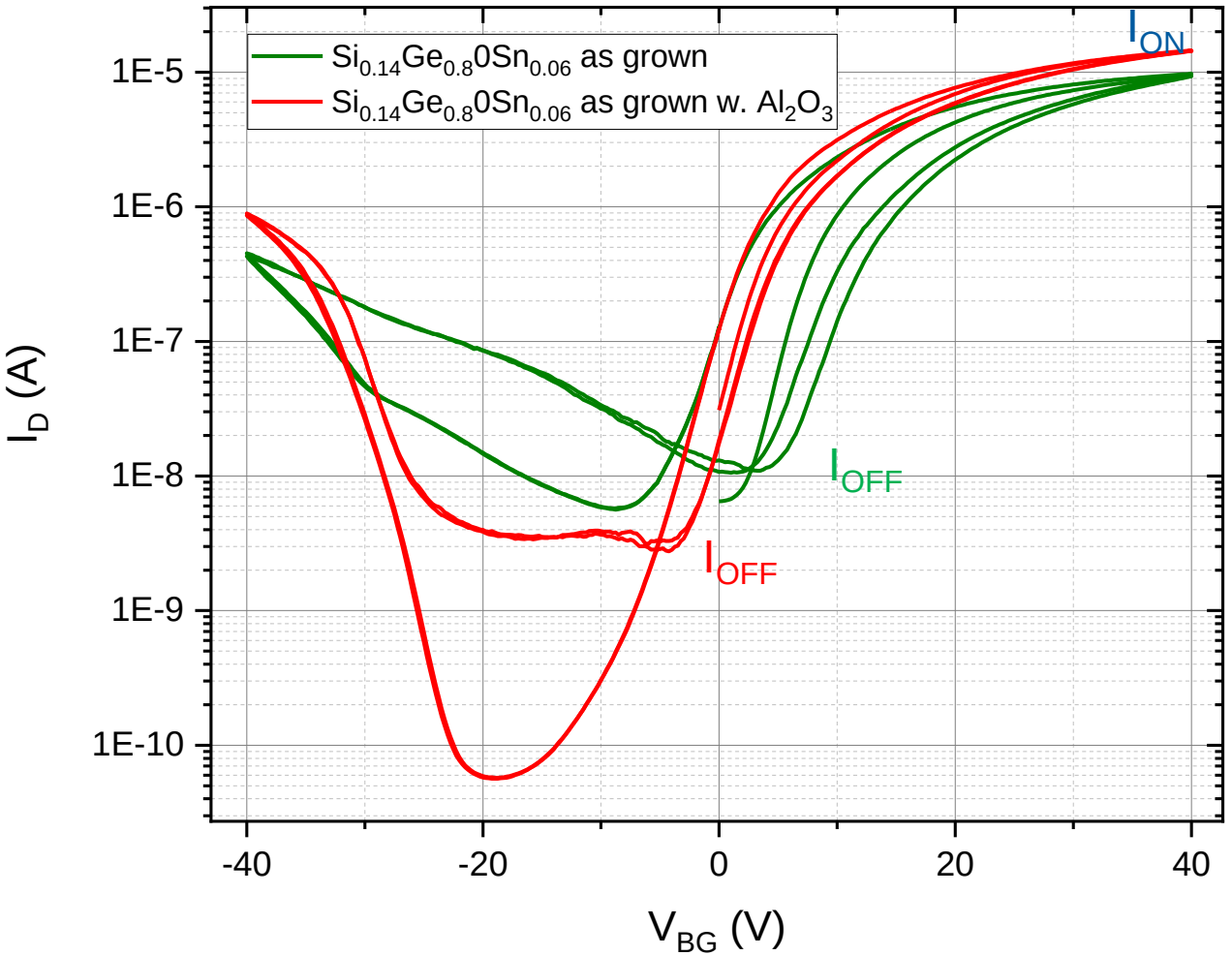


- Double sweep

- I_{ON} = 1E-5 A
- I_{OFF} = 1E-8 A

- I_{OFF} = 2E-9 A

Influence Al_2O_3:
- Left shift
- Hysteresis ↓
- I_{on}/I_{OFF} 5E+4



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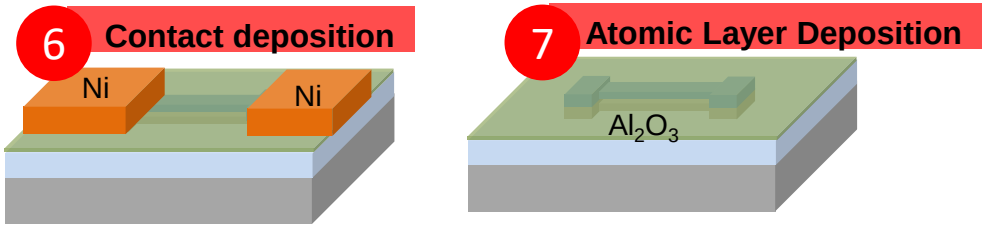
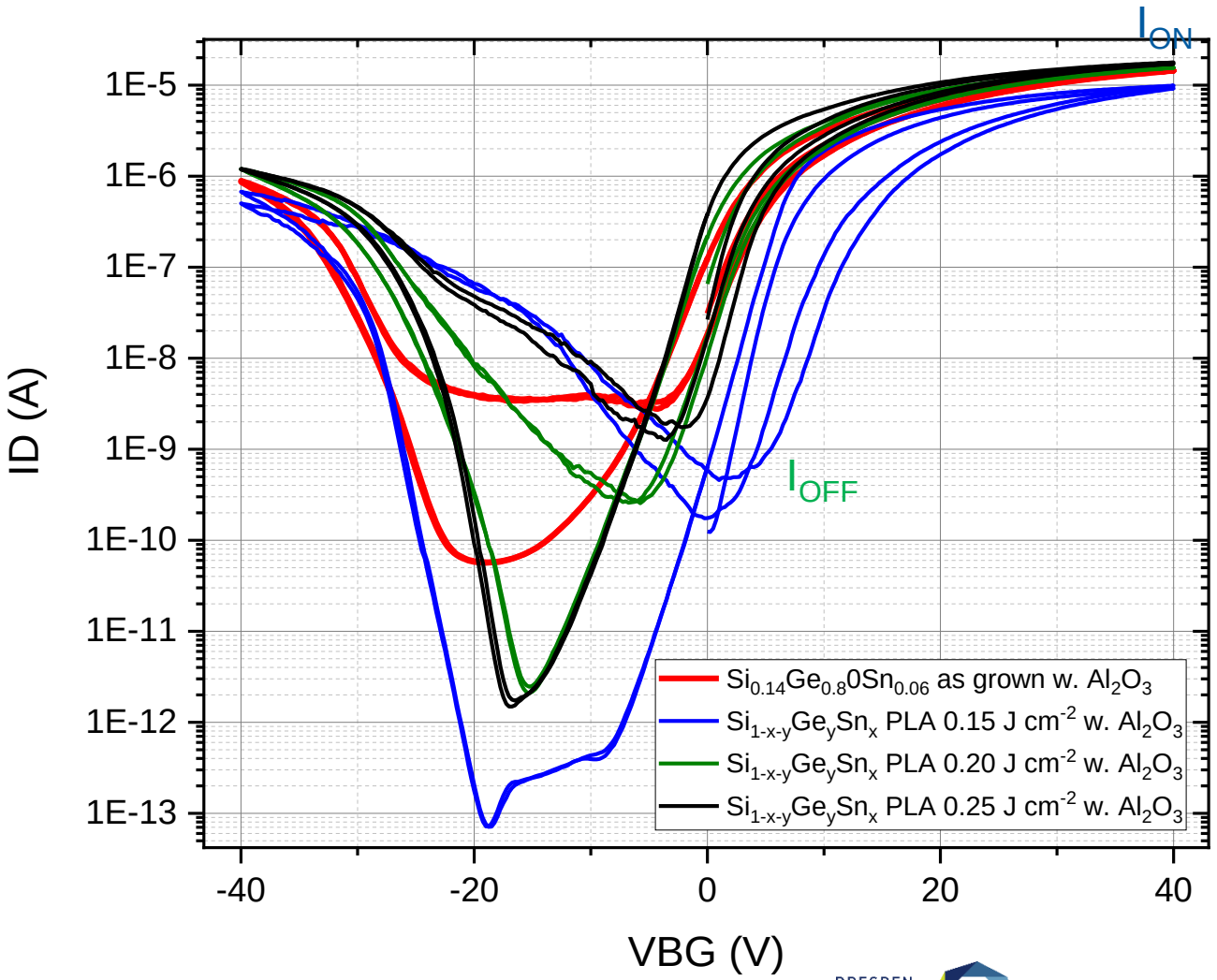
Transistor fabrication

$Si_{1-x-y}Ge_ySn_xOI$



Influence PLA



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DRESDEN concept

Summary $Si_{1-x-y}Ge_ySn_xOI$

- Device fabrication process adjusted based on previous results
- $Si_{1-x-y}Ge_ySn_x$ growth on Si caused defects in $Si_{1-x-y}Ge_ySn_x$ layer
- Post growth PLA performed
  - Amorphous inclusions can crystallize due to PLA
  - PLA can lead to Sn surface diffusion
- $Si_{1-x-y}Ge_ySn_xOI$ and $Ge_{1-x}Sn_x$ OI transistors fabricated
  - High I_{ON} could be achieved
  - Al_2O_3 increases the I_{ON}/I_{OFF} ratio, reduces hysteresis
  - Problems to turn the off transistor while using back gate
    - Control via top gate

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DRESDEN concept

10 theses about the theses

1. $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys are promising group IV semiconductor alloys of integrated circuits.
2. $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys can be fabricated by ion beam implantation and flash lamp annealing.
3. Millisecond Flash lamp annealing can be used for contact formation and recrystallization processes.
4. Nanosecond pulsed laser annealing with energy densities above the melting threshold leads to strain relaxation and elemental redistribution.
5. Nanosecond pulsed laser annealing can improve the quality of MBE grown $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys on silicon on insulator, but leads to redistribution of elements within the layer.
6. CMOS compatible fabrication of $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ x = 6 at.%, y = 80 at.% junction less transistors is feasible.
7. Junction less $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ x=6 at.%, y= 80 at.% transistors achieves a large on currents
8. Post growth thermal treatments can improve the device performance
9. Open for transistor topic
10. Open for transistor topic

Open topics

- Status talk
- 3rd reviwer
- Submission date