Cooperation between:
HZDR
and
Chair of material science and nanotechnology (TUD)

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DRESDEN concept

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Introduction

Group IV heterostructures for future nanoelectronic devices

- Fabrication and characterisation of $Si_{1-x-y}Ge_xSn_y$ alloys -

III Transistor characterisation

$Ge_{1-x}Sn_xOI$ JNT

II Process development

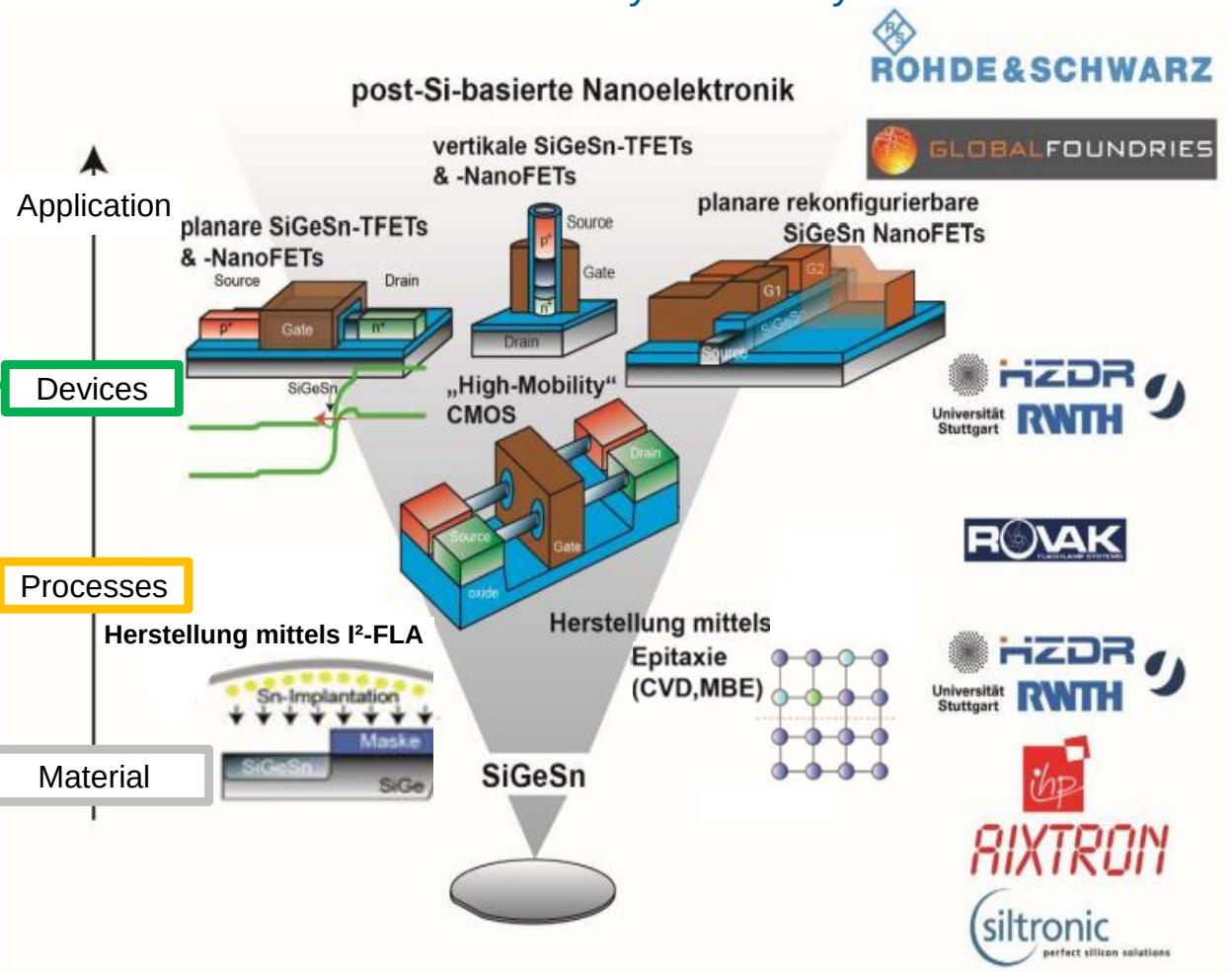
Contact formation

Etching

Lithography

I Material characterisation

GeSn and SiGeSn



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HELMHOLTZ ZENTRUM DRESDEN ROSSENDORF

Outline

- Fabrication and characterisation of $Si_{1-x-y}Ge_xSn_y$ alloys -

Motivation

Transistor fabrication

- Material analysis -

- Device analysis -

Summary

DRESDEN concept

Motivation

$Ge_{1-x}Sn_x$

$Si_{1-x-y}Ge_ySn_x$

Advantages:

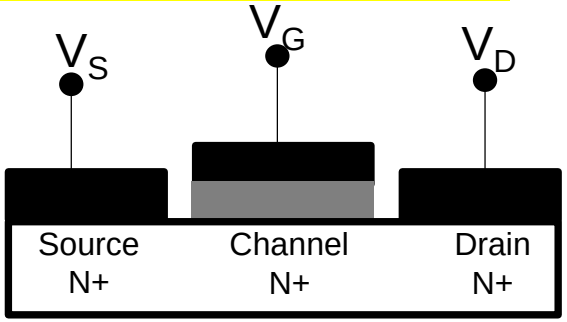
- effective band gap engineering
- high carrier mobilities
- integration in silicon based processes
- optoelectronics and nanoelectronics on same chip

same chip

optoelectronics

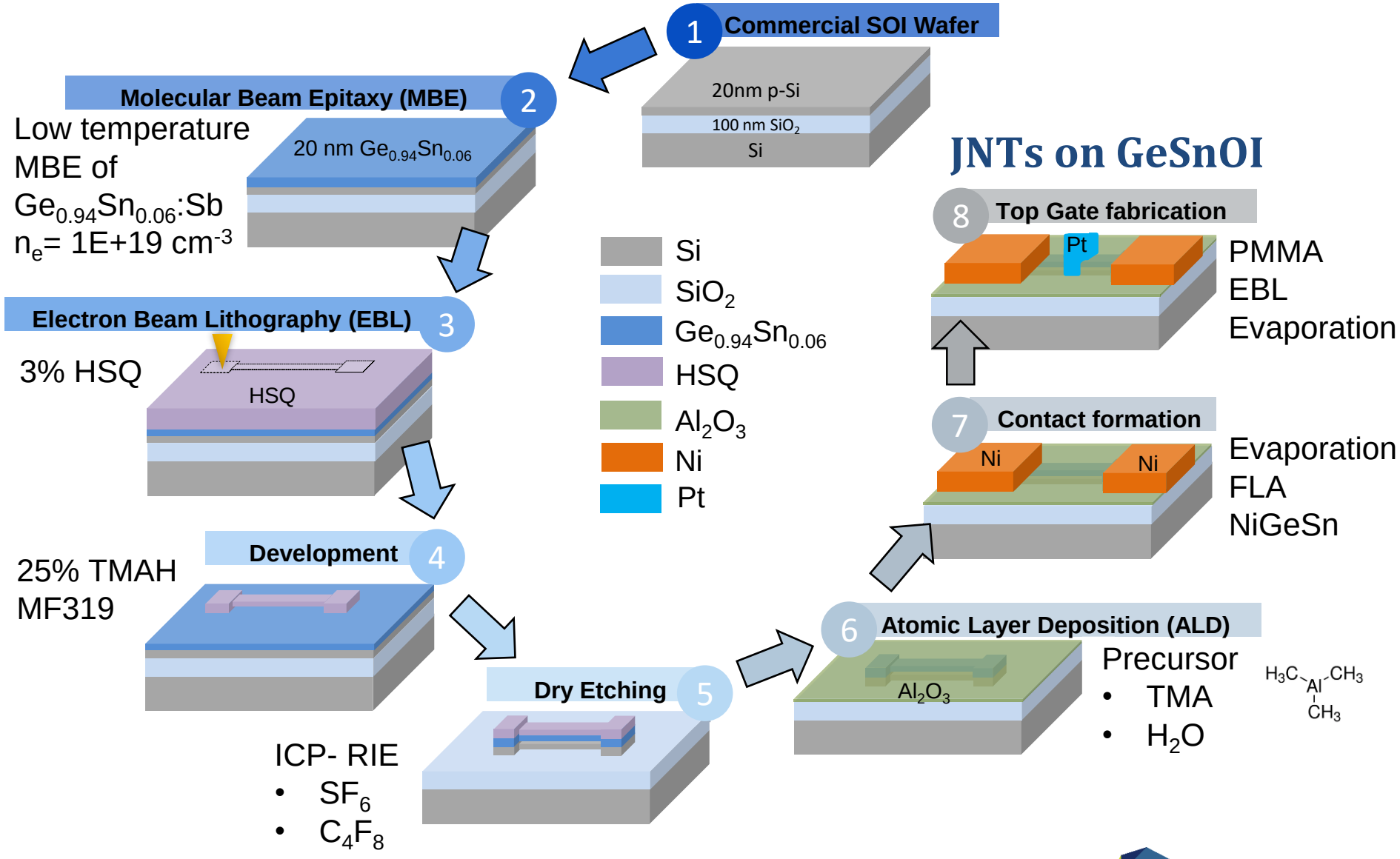
nanoelectronics

III	IV	V
B	C	N
Al	Si	P
Ga	Ge	As
In	Sn	Sb
Ti	Pb	Bi

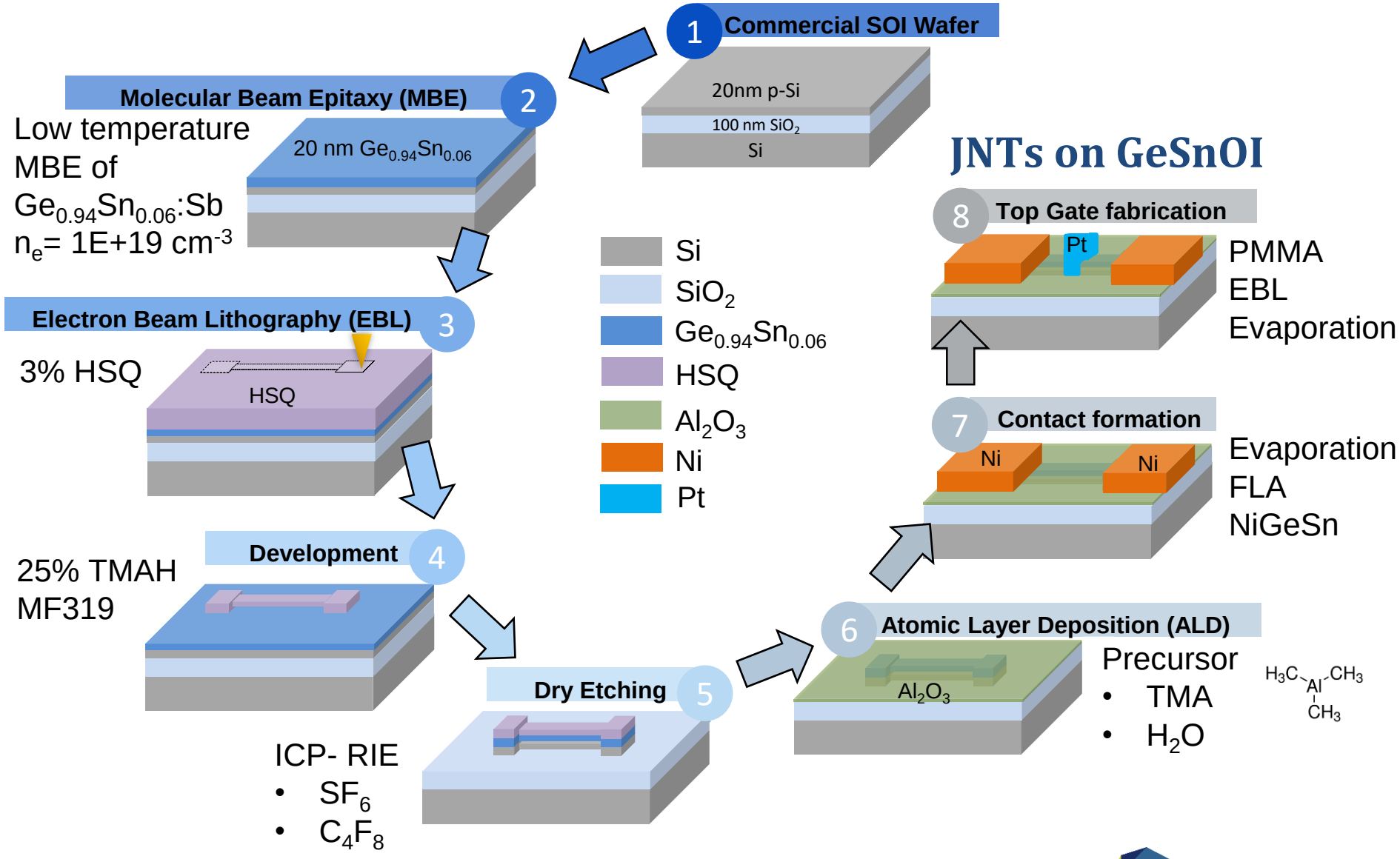


Junction-Less Transistor

Transistor fabrication – general process flow



Transistor fabrication – general process flow



Transistor fabrication

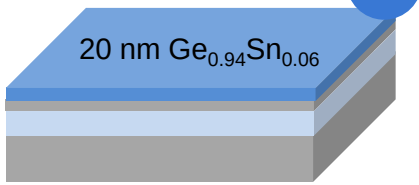
Material analysis

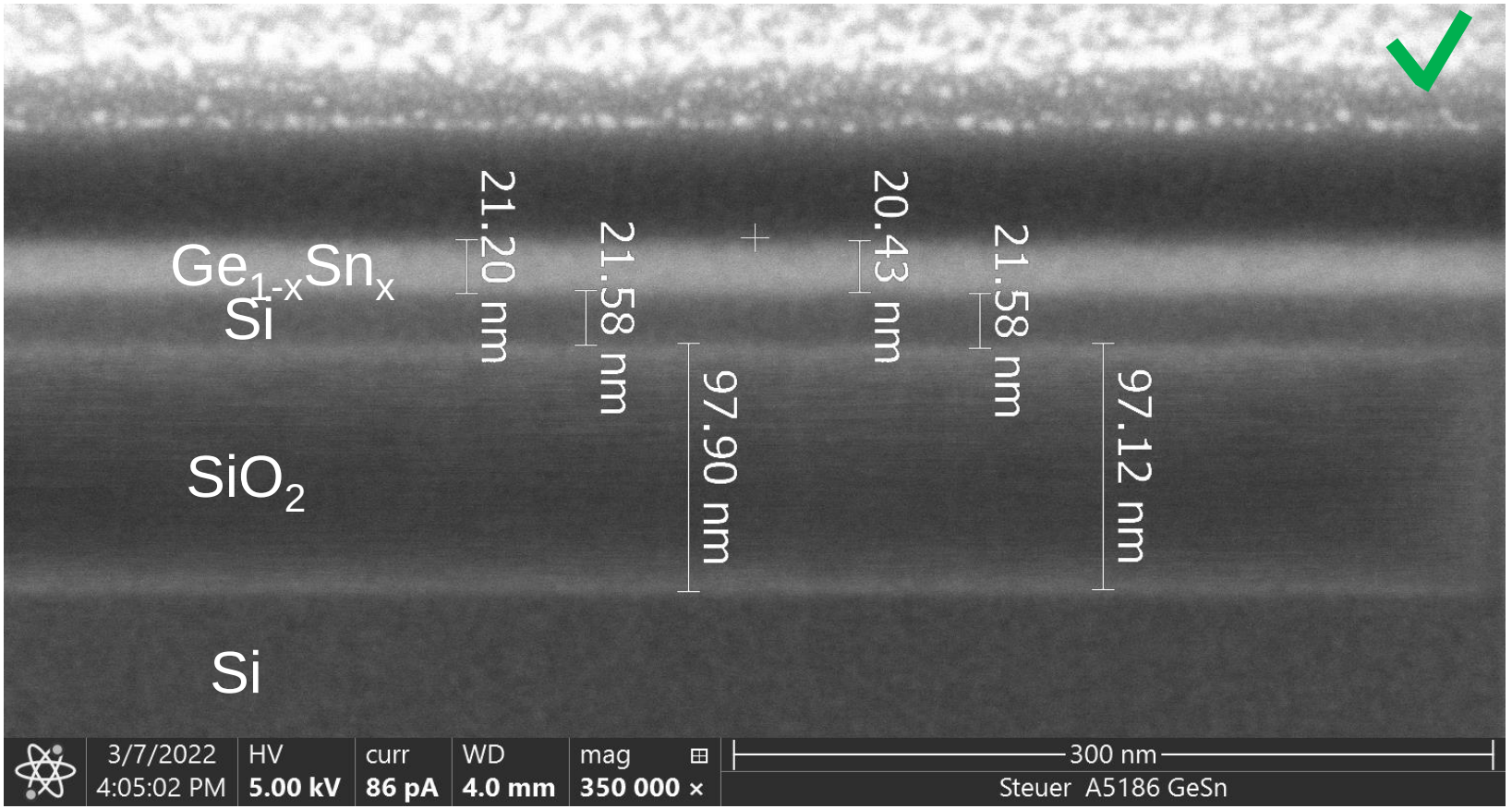
Molecular Beam Epitaxy (MBE) 2

Si

SiO_2

$Ge_{0.94}Sn_{0.06}$





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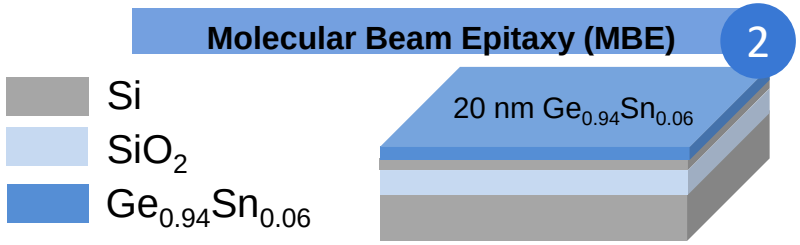
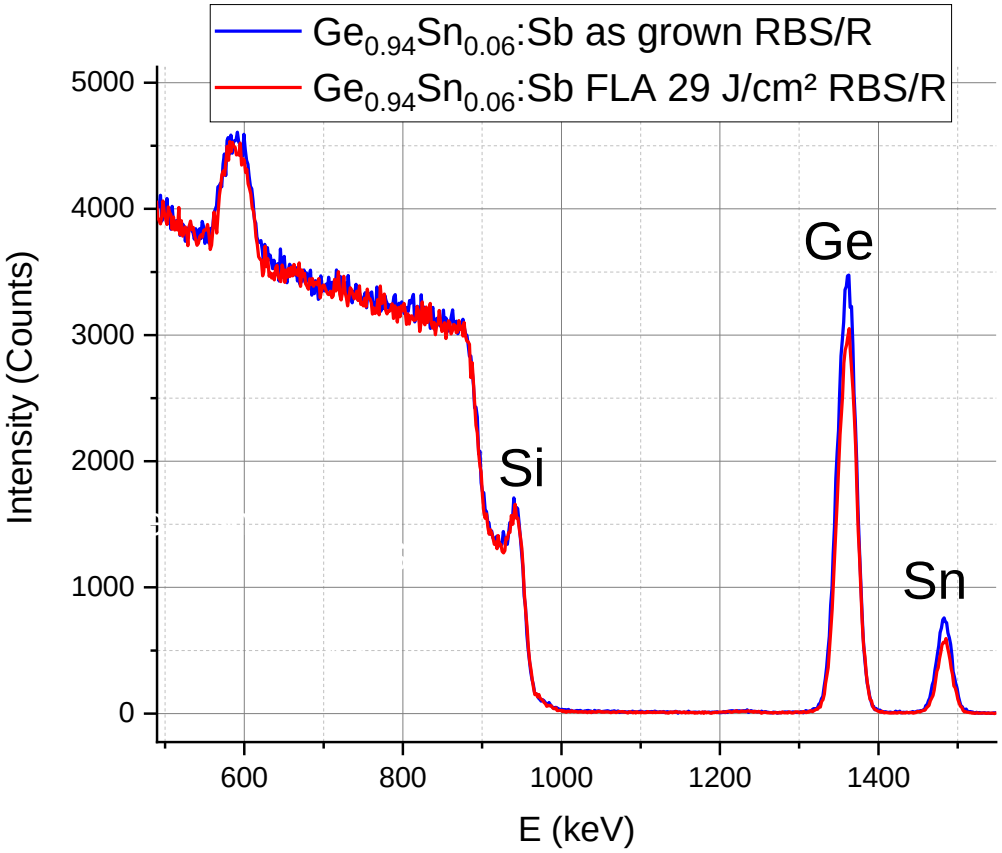
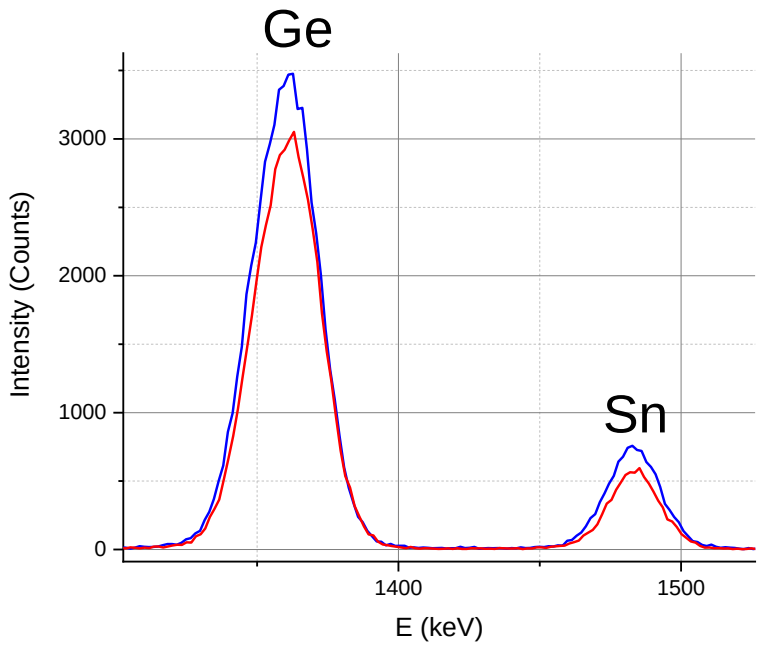
Transistor fabrication

Material analysis







SIMNRA simulation:

Material	Ge (at. %)	Sn (at. %)	Thickness (nm)
$Ge_{0.94}Sn_{0.06}$ as grown	94	6	20
$Ge_{0.94}Sn_{0.06}$ FLA	94	6	18

Transistor fabrication

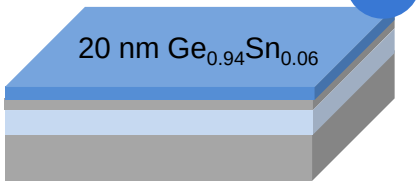
Material analysis

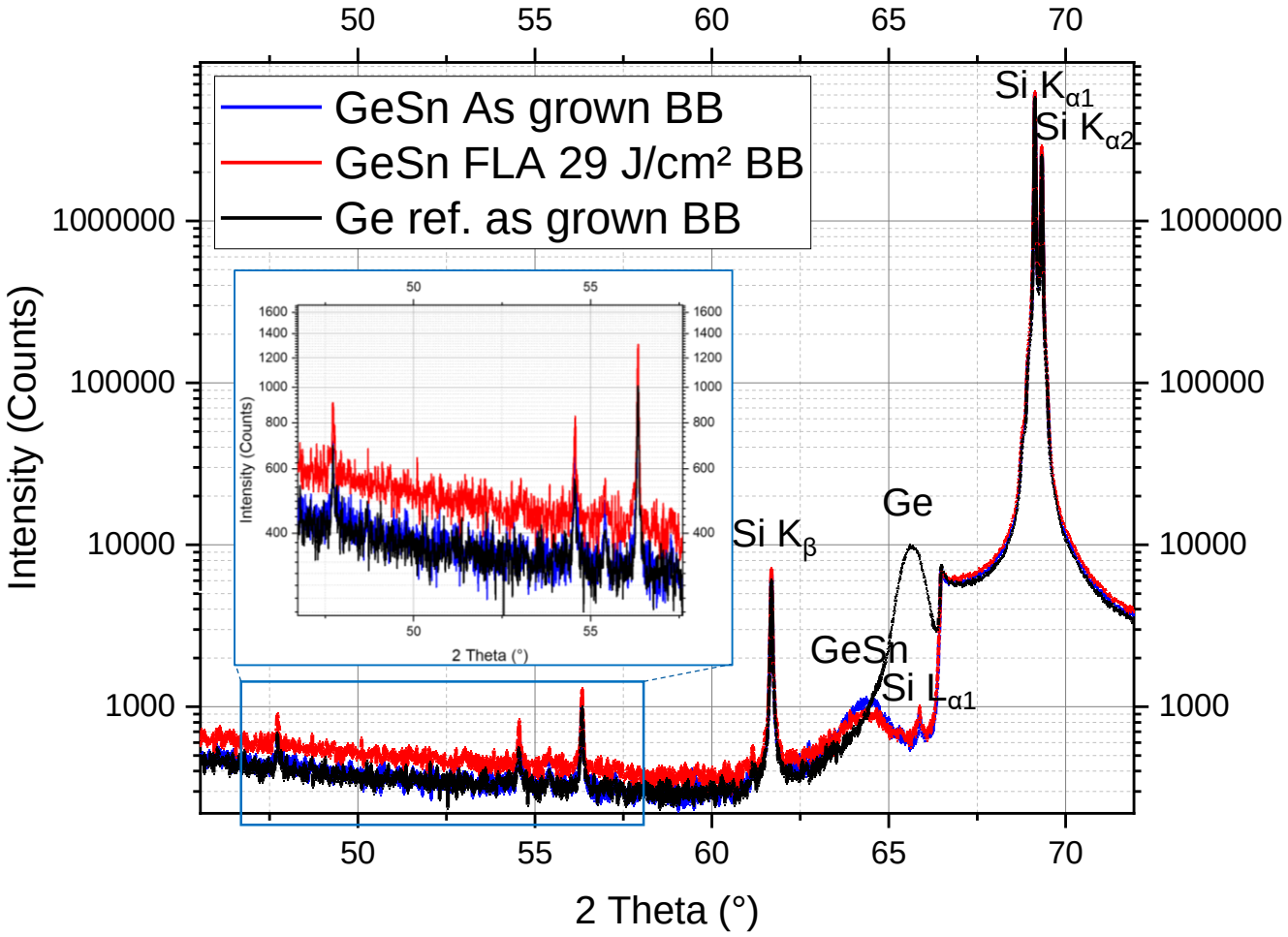
Molecular Beam Epitaxy (MBE) 2

Si

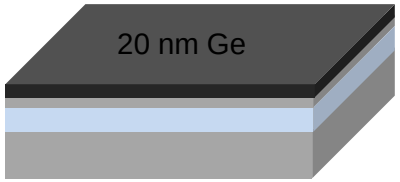
SiO_2

$Ge_{0.94}Sn_{0.06}$





Ge reference



No α-Sn or β-Sn segregations during MBE or due to FLA.

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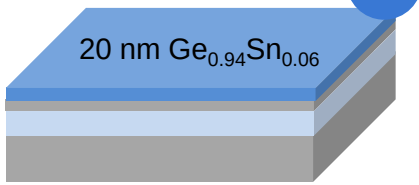
Transistor fabrication

Material analysis

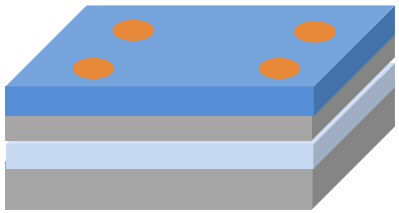
Molecular Beam Epitaxy (MBE) 2

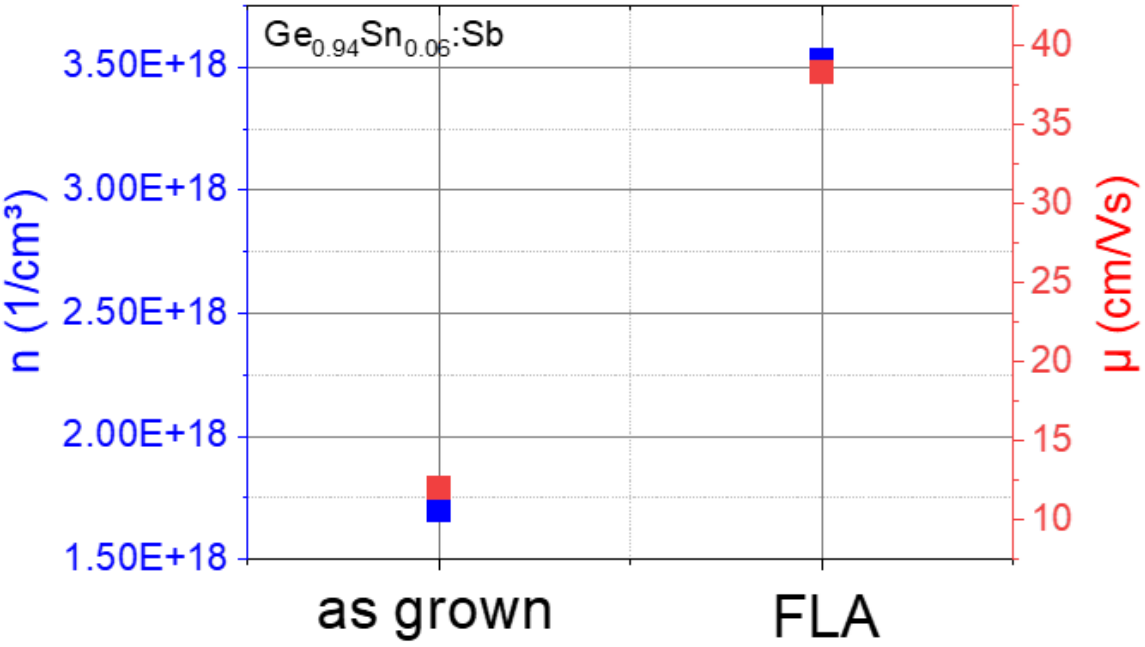
Si
SiO_2
$Ge_{0.94}Sn_{0.06}$



$Ge_{0.94}Sn_{0.06}$:Sb n_{Sb}= 1E+19 cm^{-3}

Hall effect measurements
in Van der Pauw configuration





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Outline

- Fabrication and characterisation of $Si_{1-x-y}Ge_xSn_y$ alloys -

Motivation

Transistor fabrication

- Material analysis -

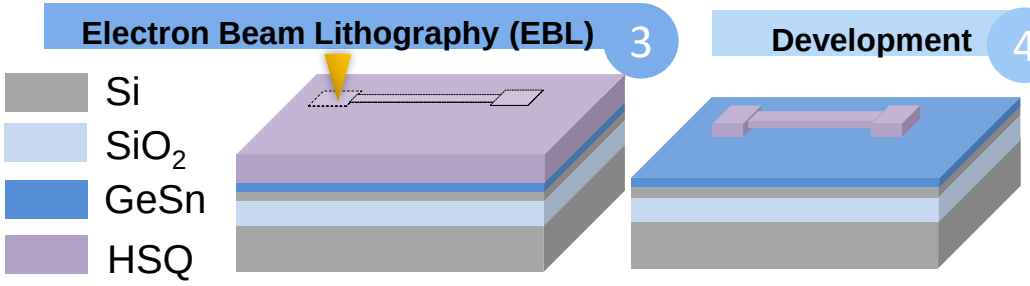
- Device analysis -

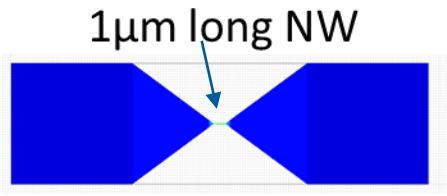
Summary

DRESDEN concept

Transistor fabrication

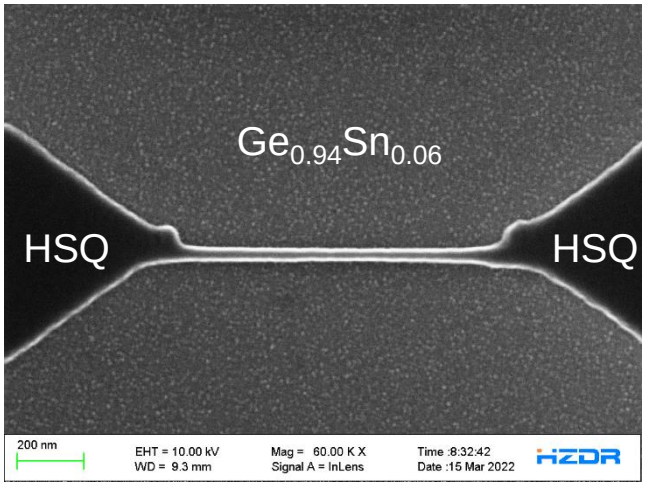
Patterning of NW

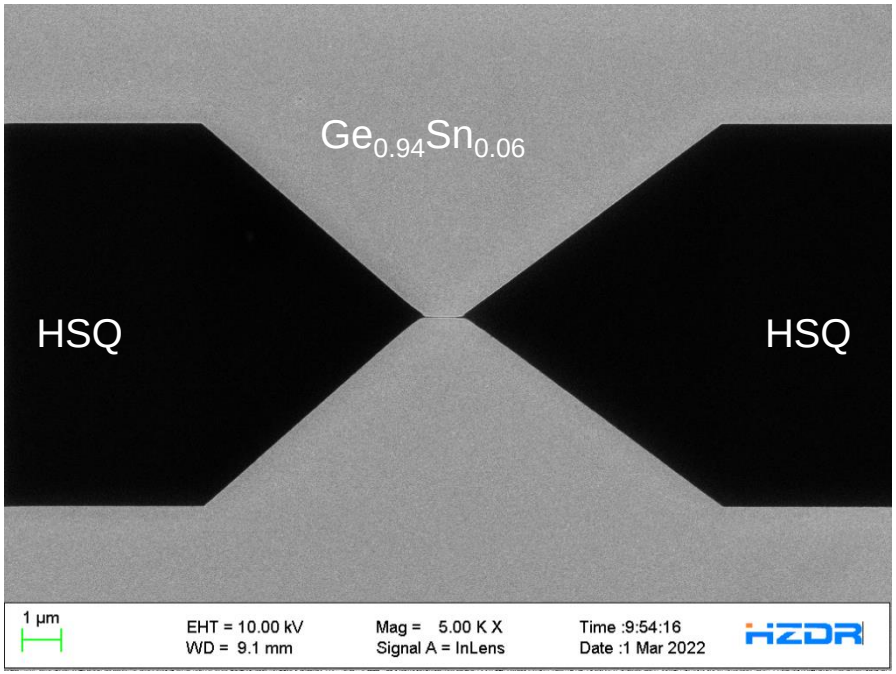


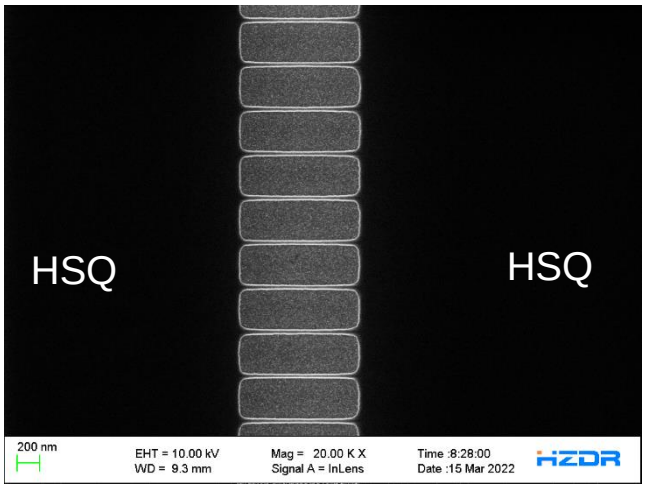


HSQ Nanowire (NW) width:

- 50 nm
- 30 nm
- 20 nm

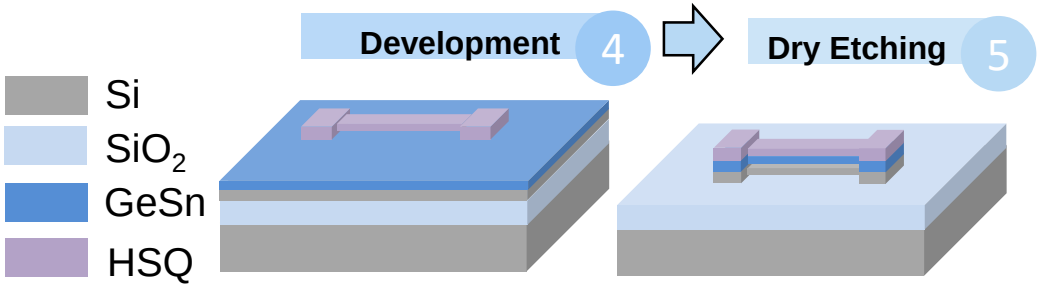


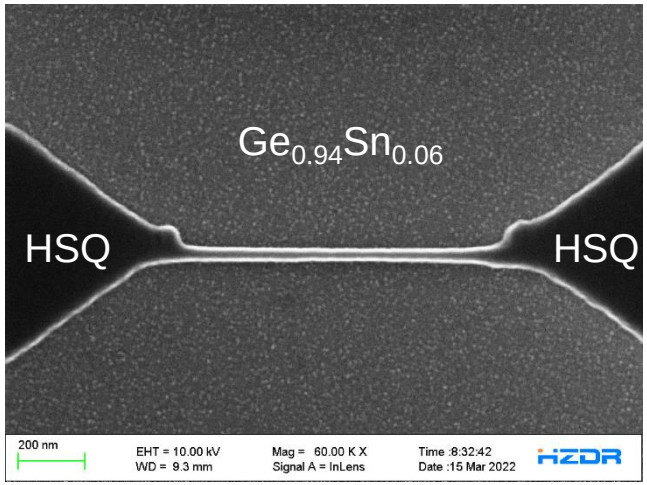




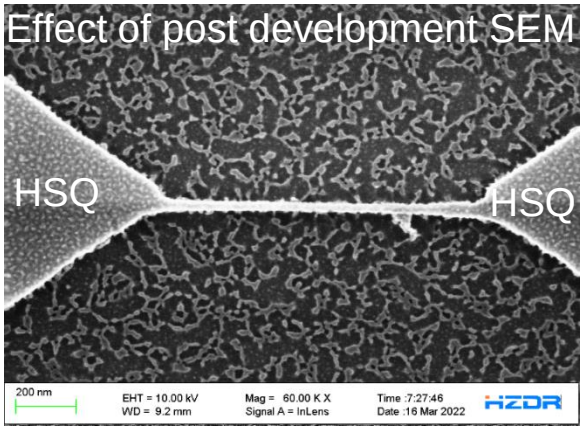
Transistor fabrication

Dry etching

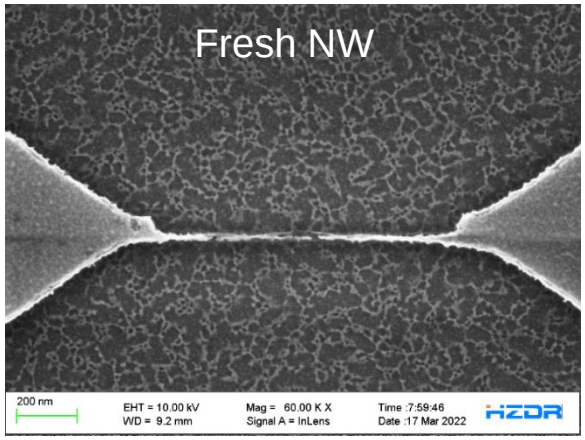




RIE



RIE + BHF



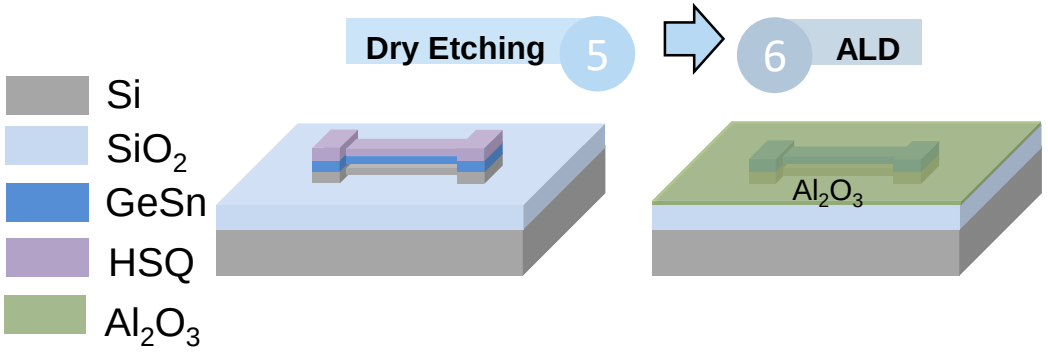
F-Based RIE:

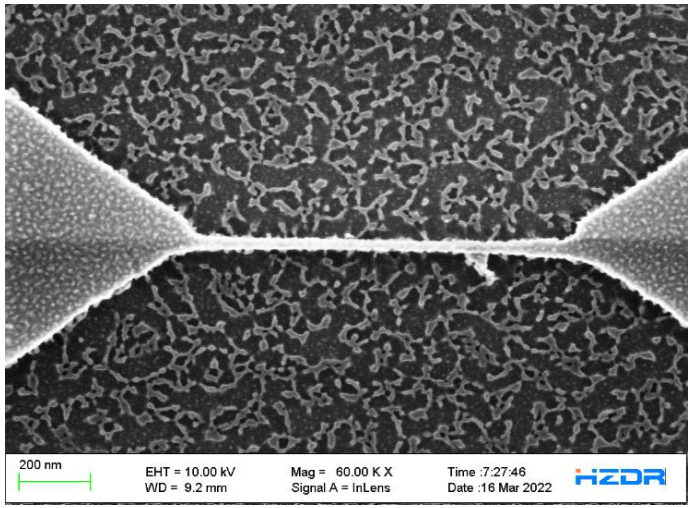
- High roughness
- Shrinking of NW

→ Process needs to be optimized

Transistor fabrication

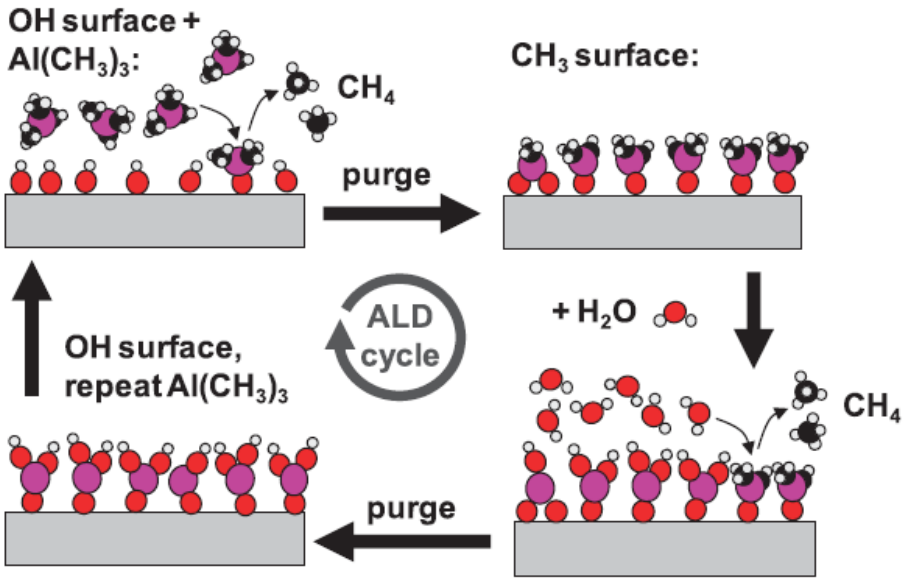
ALD





Thermal ALD at. 150 °C with TMA and H_2O

- 1% BHF
- 7 nm Al_2O_3



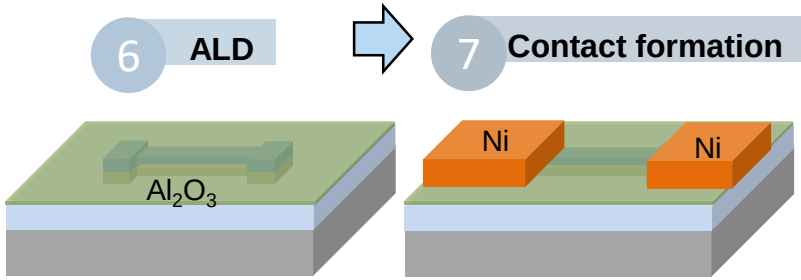
Gregory N. Parsons , Steven M. George , and Mato Knez , Guest Editors;
Progress and future directions for Atomic layer deposition and ALD-based chemistry. 2011
DOI: 10.1557/mrs.2011.238

Transistor fabrication

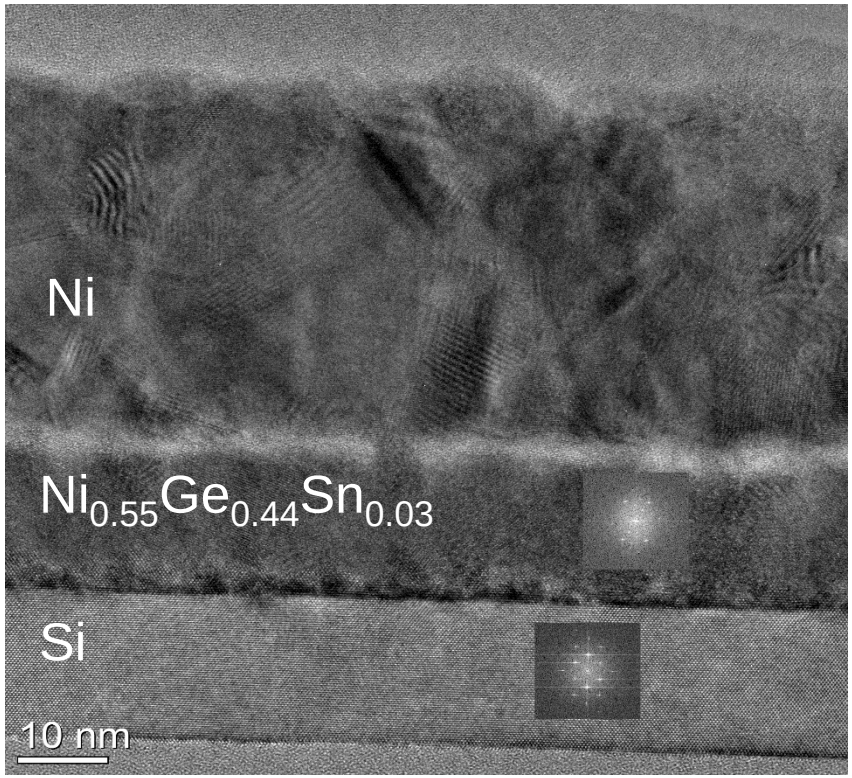
Contact formation

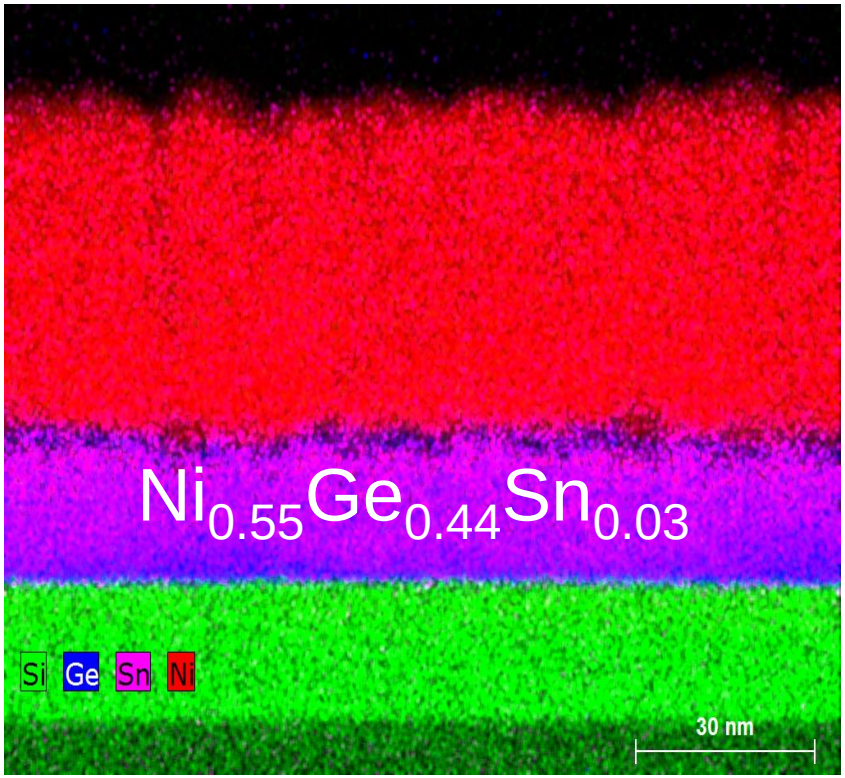
- UV Lithography of MAN1420
- HF dip
- Ni evaporation
- FLA 29 J/cm²

Si
SiO_2
GeSn
Al_2O_3
Ni



Successful formation of NiGeSn ✓



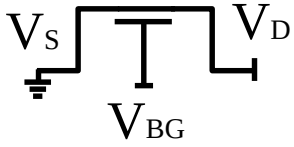


Transistor fabrication

Device analysis

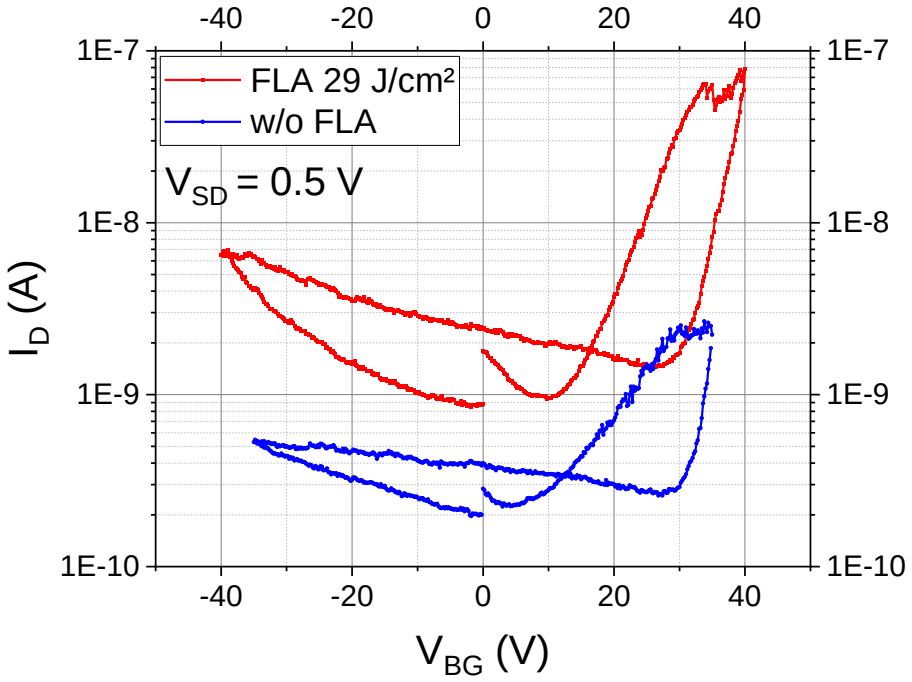
Si
SiO_2
GeSn
Al_2O_3
Ni

7 Contact formation

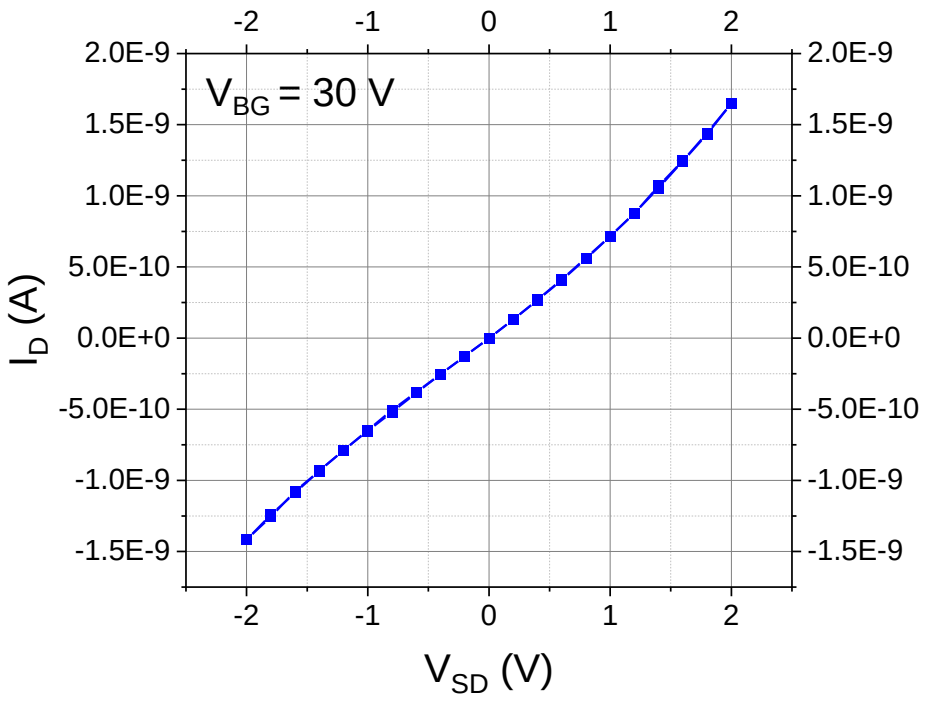


(-40 to +40) V

Transfer characteristic



Output characteristic



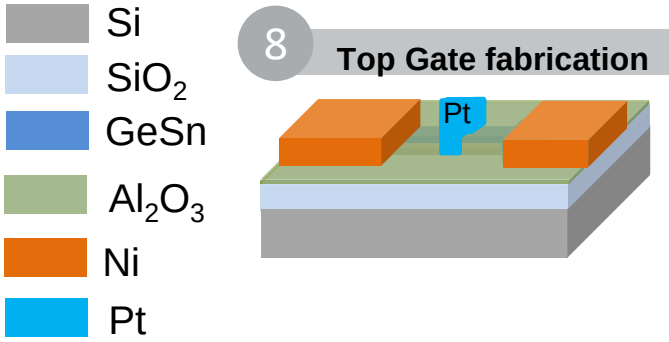
I_{ON}/I_{OFF}(FLA) ~ $3x10^1$

I_{ON}/I_{OFF} (w/o FLA) ~ $1x10^1$

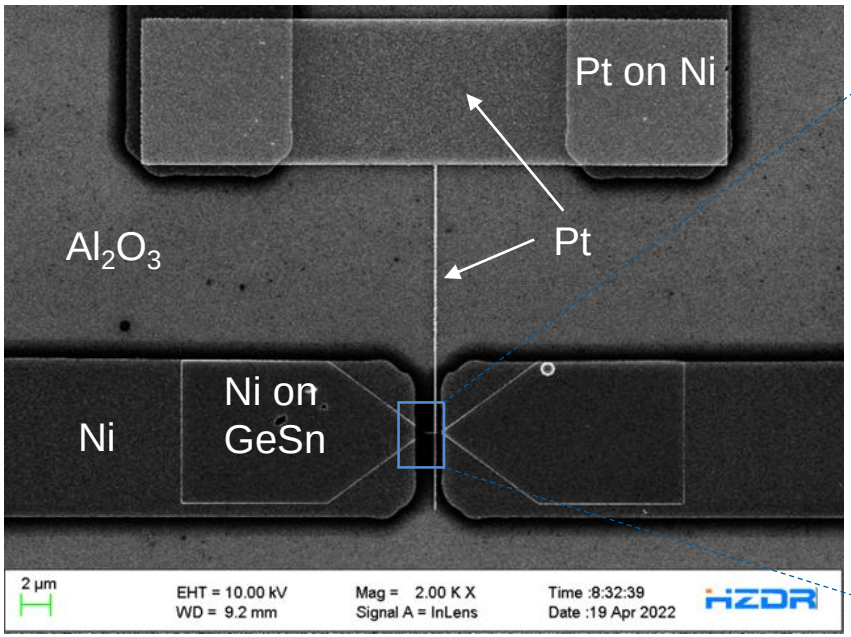
Transistor fabrication

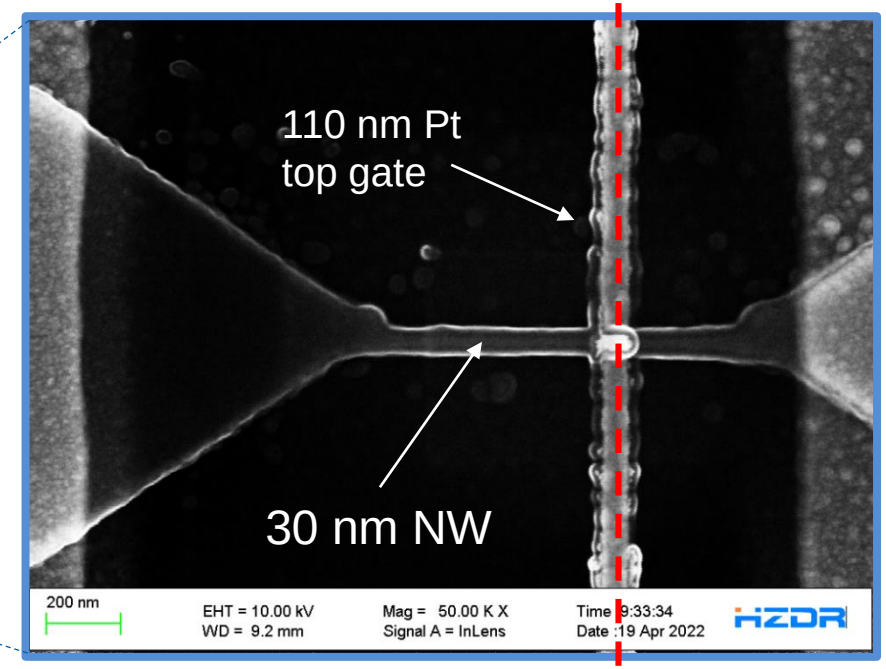
Top gate fabrication

- PMMA spin coating
- EBL
- Development
- Pt evaporation



Cross section TEM





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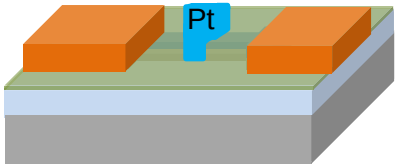
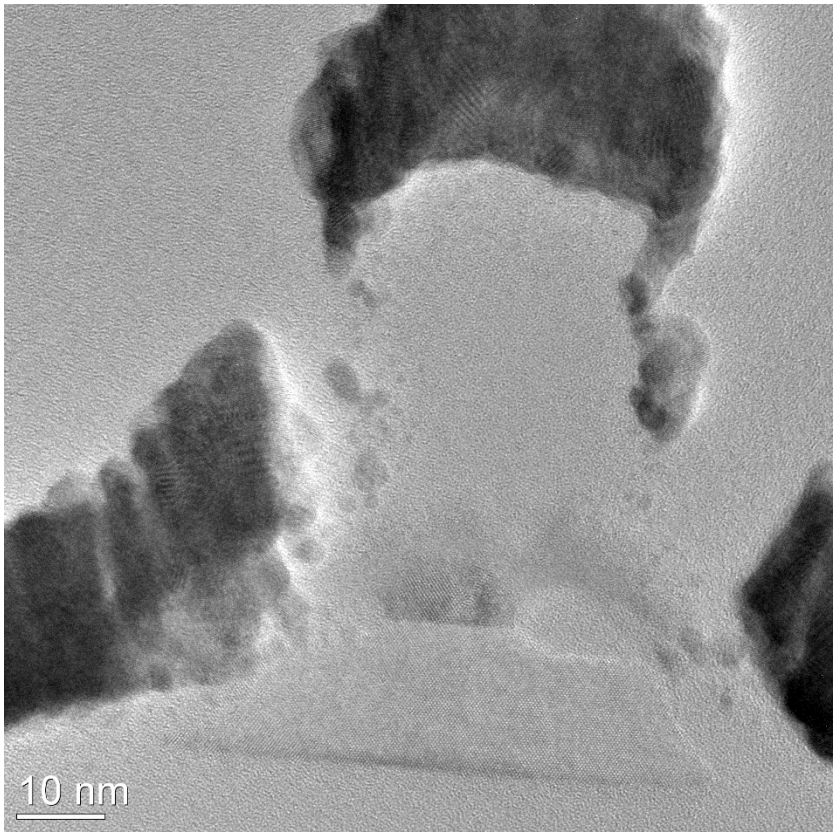
Transistor fabrication

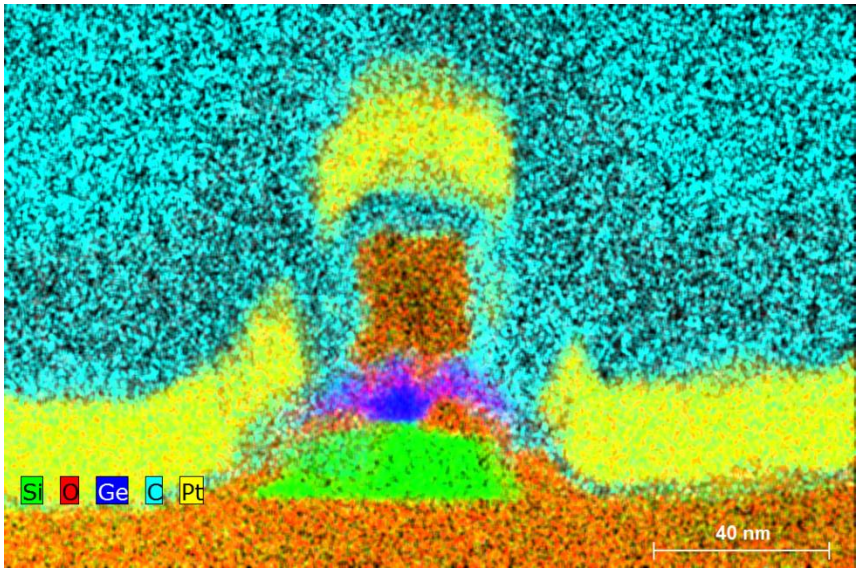
Device analysis

Si
SiO_2
GeSn
Al_2O_3
Ni
Pt

8 Top Gate fabrication







Observation:

- RIE needs to be optimized
  → Cl based RIE
- Al_2O_3 dielectric is not visible
- Pt top gate not continuous

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Outline

Group IV semiconductor alloys:
From material towards first Junction–Less Nanowire Transistors

Motivation

Challenges

Transistor fabrication

- Material analysis -

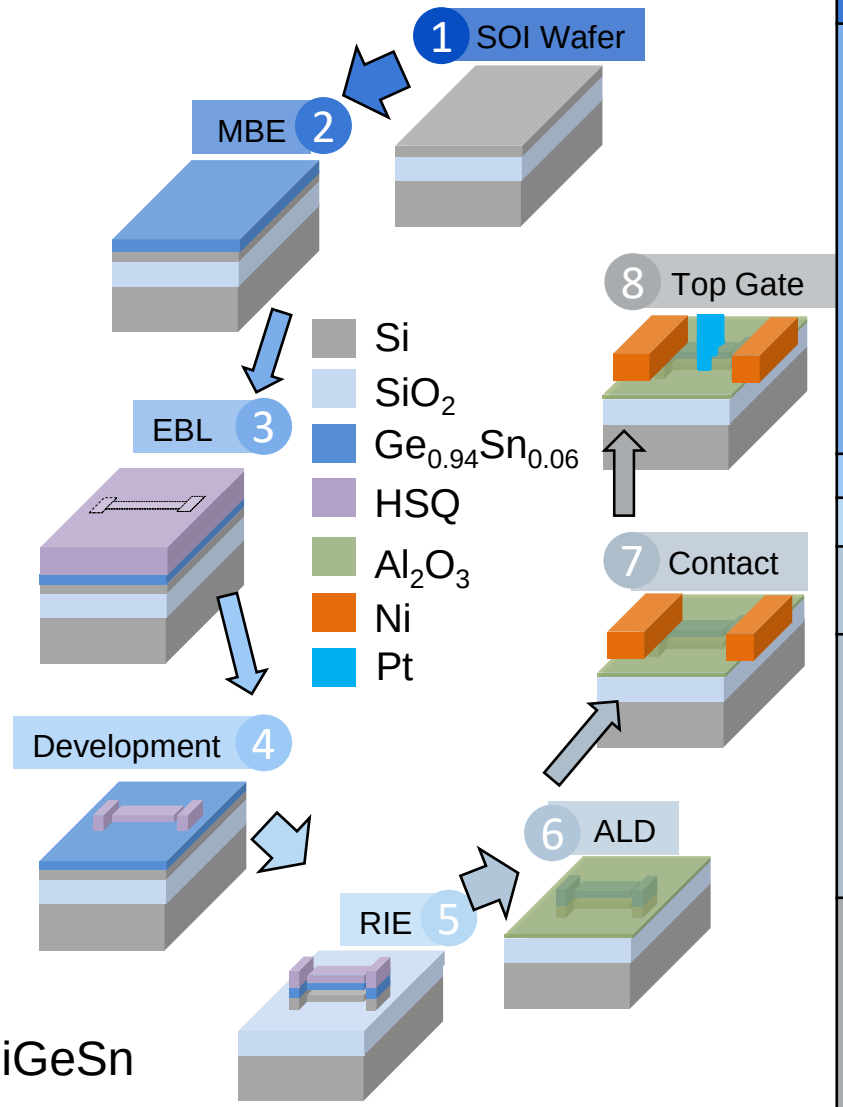
- Device analysis -

Summary

DRESDEN concept

Summary

- Material analysis:
  - GeSn layer by MBE
    - Layer stack
    - Chemical composition
  - Post growth FLA improves layer quality
- Device analysis:
  - Most process steps are usable
- Other Materials:
  - MBE: GeSn, SiGeSn
  - Ion implantation: Ge:Sn, SiGe:Sn



No		Step name	Status
2		MBE	✓
3 NW patterning	3-1	Spin coating MAN 1420	✓
	3-2	Post bake	✓
	3-3	Oxide etching	✓
	3-4	Si-SiO2 deposition Marker	✓
	3-5	Lift off	✓
	3-6	Oxide etching	✓
	3-7	HSQ spin coating	✓
	3-7	Post bake	✓
	3-8	EBL	✓
4		Development	✓
5		ICP RIE	X
6 ALD	6-1	Stripping HSQ	✓
	6-2	Al_2O_3 deposition	✓
7 Contact formation	7-1	Spin coating	✓
	7-2	Post bake	✓
	7-3	Oxide etching	✓
	7-4	Ni deposition	✓
	7-5	Lift off MAN 1420	✓
	7-6	FLA contact formation	✓
8 Top contact	7-1	Pre bake	✓
	7-2	Spin coating PMMA	✓
	7-3	Post bake	✓
	7-4	EBL	✓
	7-5	PMMA Development	✓
	7-6	Pt deposition	✓
	7-7	Lift off	✓

* Cleaning steps are not included

✓ Work well ✓ small optimization X large optimization