# Promotionsvorhaben

# Oliver Steuer

## - Thema und Projekt -
## - Aktueller Stand -
## - Ausblick -

**Oliver Steuer**

**06.05.2022**

**Institute of Ion Beam Physics and Materials Research**

**Helmholtz-Zentrum Dresden-Rossendorf**

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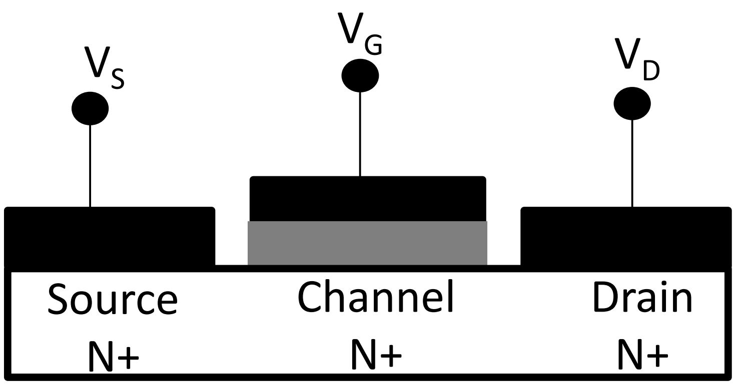
# Motivation

## Si

+ cheap
+ well understood
+ $SiO_2$
+ well developed technology
- carrier mobility




| Semiconductors | Group IV Si | Group IV Ge |
|---|---|---|
| Electron mobility ($cm^2/Vs$) | 1600 | 3900 |
| Hole mobility ($cm^2/Vs$) | 430 | 1900 |

| YEAR OF PRODUCTION | 2020 | 2022 | 2025 | 2028 | 2031 | 2034 |
|---|---|---|---|---|---|---|
| | G48M36 | G45M24 | G42M20 | G40M16 | G38M16T2 | G38M16T4 |
| Logic industry "Node Range" Labeling (nm) | "5" | "3" | "2.1" | "1.5" | "1.0 eq" | "0.7 eq" |
| IDM-Foundry node labeling | i7-f5 | i5-f3 | i3-f2.1 | i2.1-f1.5 | i1.5e-f1.0e | i1.0e-f0.7e |
| Logic device structure options | FinFET | finFET LGAA | LGAA | LGAA | LGAA-3D | LGAA-3D |
| Mainstream device for logic | finFET | finFET | LGAA | LGAA | LGAA-3D | LGAA-3D |
| LOGIC TECHNOLOGY ANCHORS | | | | | | |
| Patterning technology inflection for Mx interconnect | 193i, EUV DP | 193i, EUV DP | 193i, EUV DP | 193i, High-NA EUV | 193i, High-NA EUV | 193i, High-NA EUV |
| Beyond-CMOS as complimentary to mainstream CMOS | - | - | - | 2D Device, FeFET | 2D Device, FeFET | 2D Device, FeFET |
| Channel material technology inflection | SiGe25% | SiGe50% | SiGe50% | Ge, 2D Mat | Ge, 2D Mat | Ge, 2D Mat |
| Process technology inflection | Conformal Doping, Contact | Channel, RMG | Lateral /Atomic Etch | Non-Cu Mx | 3DVLSI | 3DVLSI |
| Stacking generation inflection | 2D | 3D-stacking: W2W, D2W Mem-on-Logic | 3D-stacking: W2W, D2W Mem-on-Logic | 3D-stacking, Fine-pitch stacking, P-over-N, Mem-on-Logic | 3D-stacking, 3DVLSI: Mem-on-Logic with Interconnect | 3D-stacking, 3DVLSI: Logic-on-Logic |

*Note: Information based on 2020 IRDS More Moore Table MM01

Source: International Roadmap for Devices and Systems (IRDS™) 2021 EditionIRDS™ 2021: Metrology

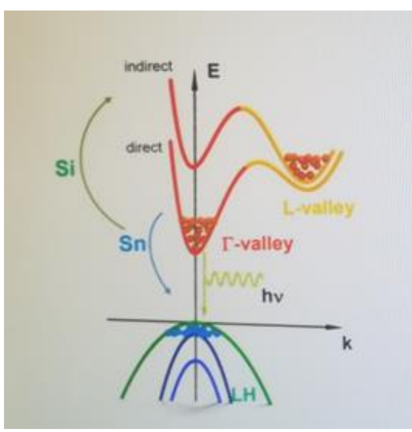
# Motivation

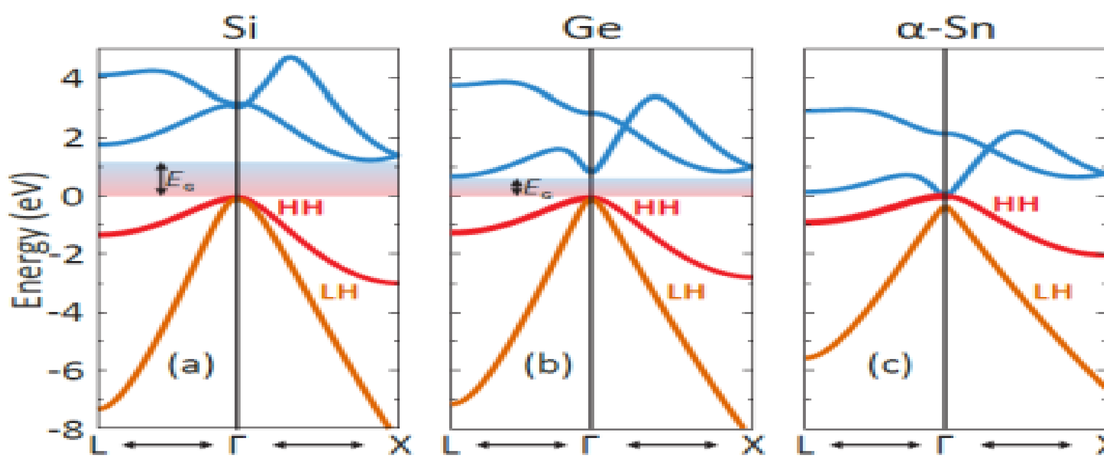
**$Ge_{1-x}Sn_x$**

**$Si_{1-x-y}Ge_ySn_x$**

## Advantages:

• effective band gap engineering •
• high carrier mobilities •
• integration in silicon based processes •
• optoelectronics and nanoelectronics on same chip •




P.Moontragoon, Z. Ikonić, and P. Harrison; Band structure calculations of Si–Ge–Sn alloys: achieving direct band gap materials. Semiconductor science and technology, 2007.



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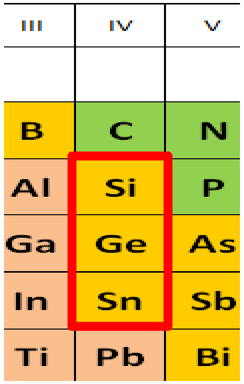
# Motivation

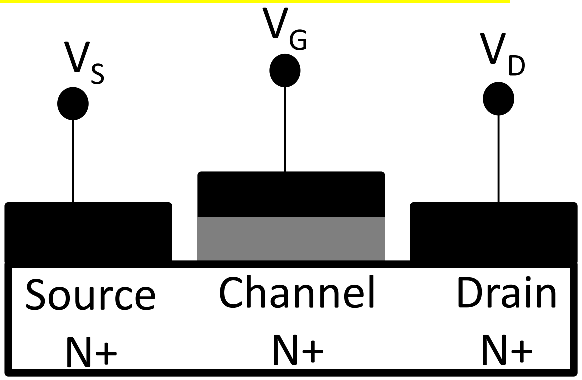
**$Ge_{1-x}Sn_x$** | **$Si_{1-x-y}Ge_ySn_x$**

## Advantages:

- effective band gap engineering
- high carrier mobilities
- integration in silicon based processes
- optoelectronics and nanoelectronics on same chip

**optoelectronics** ⟵ **same chip** ⟶ **nanoelectronics**



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# BMBF-Project

Dr. Slawomir Prucnal   Dr. Yordan Georgiev   Moazzam Khan   Oliver Steuer

## Group IV heterostructures for future nanoelectronic devices

III Transistor fabrication & characterisation

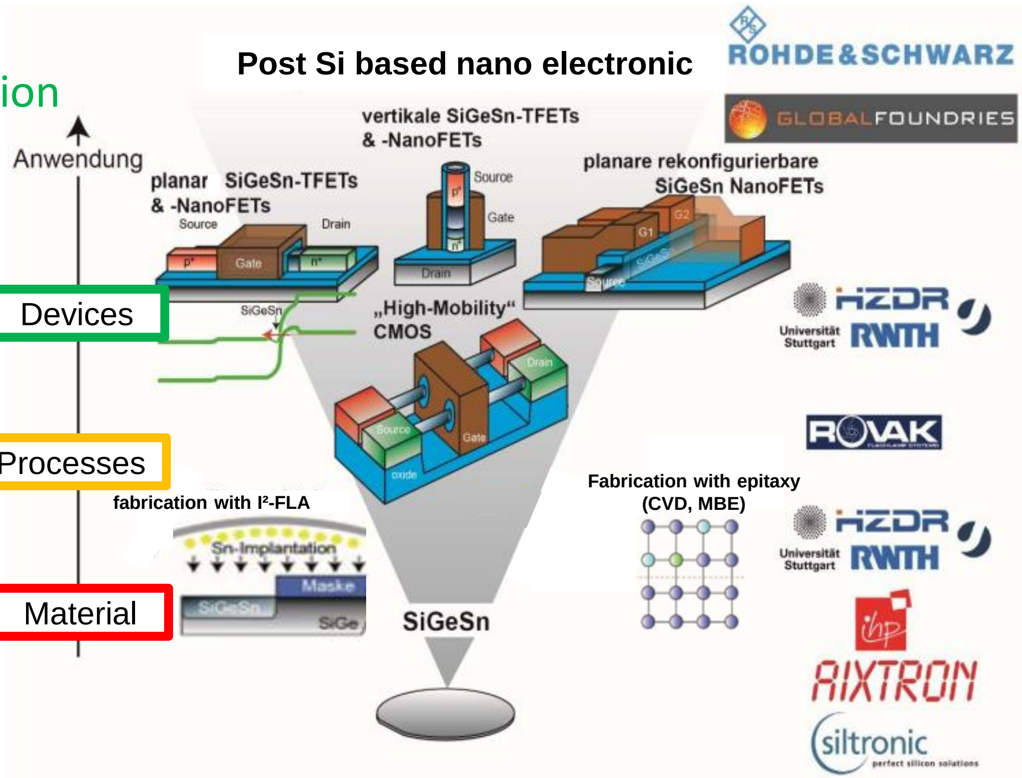
- $Si_{1-x-y}Ge_xSn_yOI$ JNT

II Process development

- Contact formation
- Annealing
- Ion implantation

I Material characterisation

- GeSn and SiGeSn



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# Challenges

## $Si_{1-x-y}Ge_ySn_x$

- Solubility of Sn < 1%

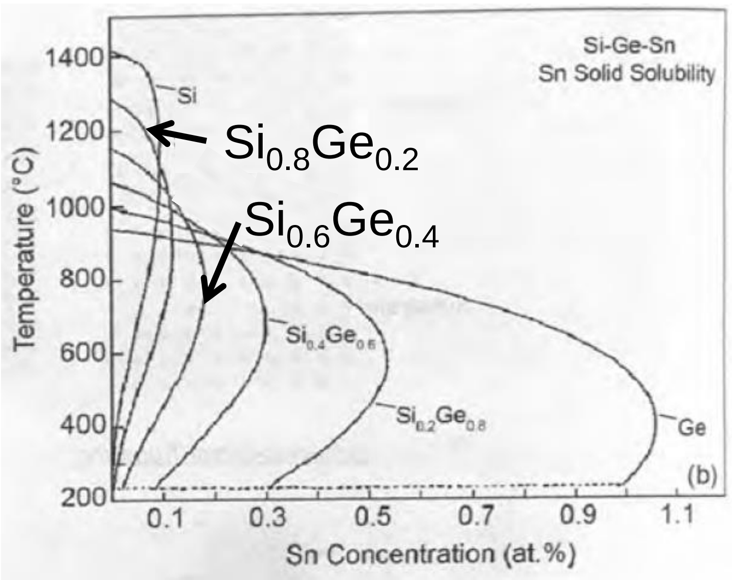



Fig. Calculated Sn solid solubility curves as a function of temperature for various Si-Ge solid compositions. The dashed line correspond to the ternary eutectic points.

J.P. Fleurial, A. Borshchevsky, SiGe-Metal ternary phase diagram calculations, J. Electrochem. Sci. 137 (1990) 2928, DOI:10.1149/1.2087101

## $Ge_{1-x}Sn_x$

- solubility limit < 1%

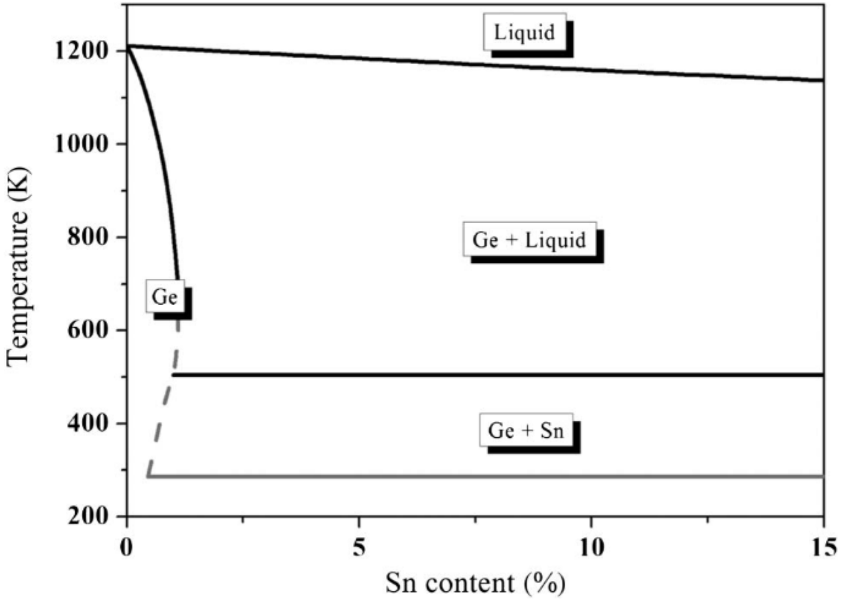


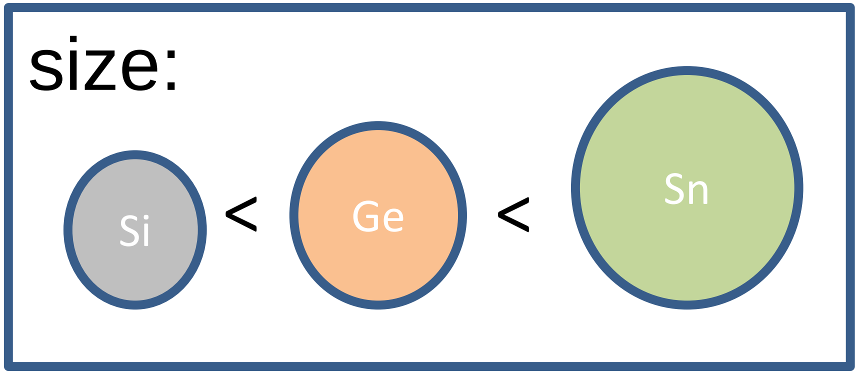

Fig. Equilibrium phase diagram of Ge-Sn. Shown is the Ge rich side up to 15%Sn.

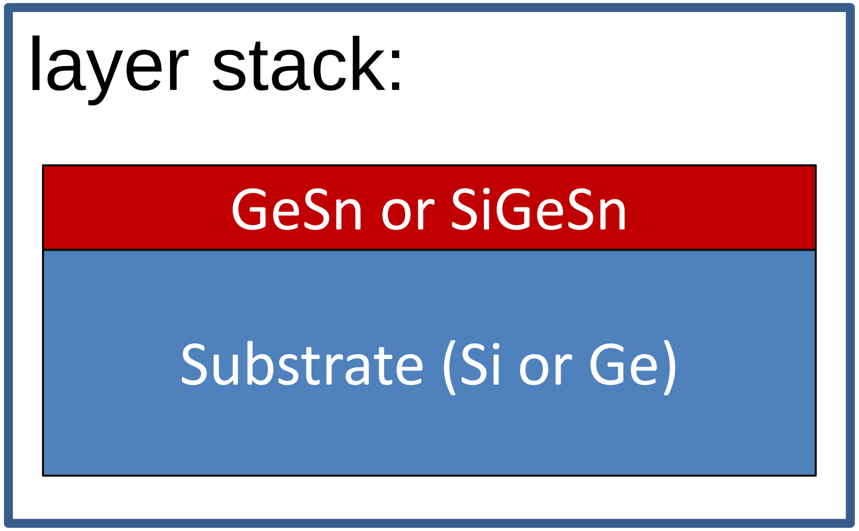
E. Kasper, M. Kittler, M. Oehme, and T. Arguirov: Germanium tin: silicon photonicstoward the mid-infrared; 2013

# Challenges

## GeSn

- compressive strain



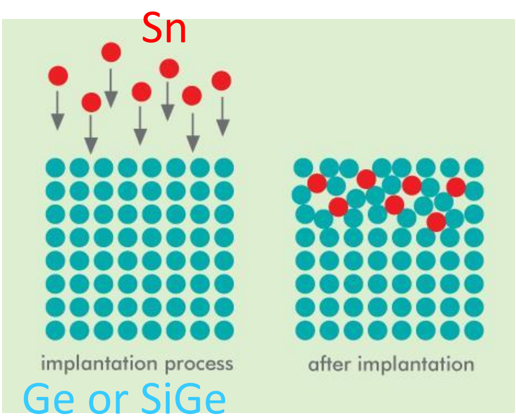



# Material fabrication SiGeSn

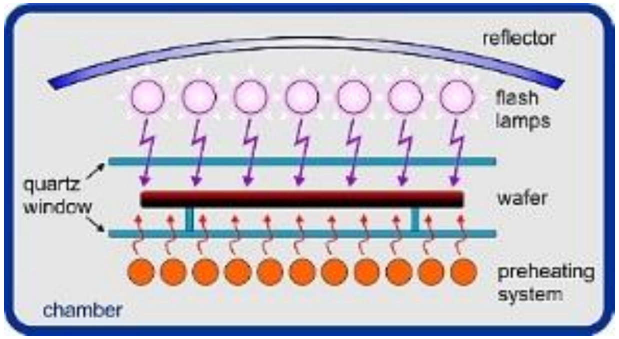
## Ion implantation and FLA - process

Ion implantation

FLA: Recrystallization

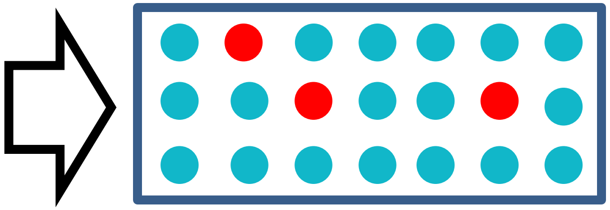



+




https://www.hzdr.de/db/Pic?pOid=56057

$Si_{1-x-y}Ge_xSn_y$





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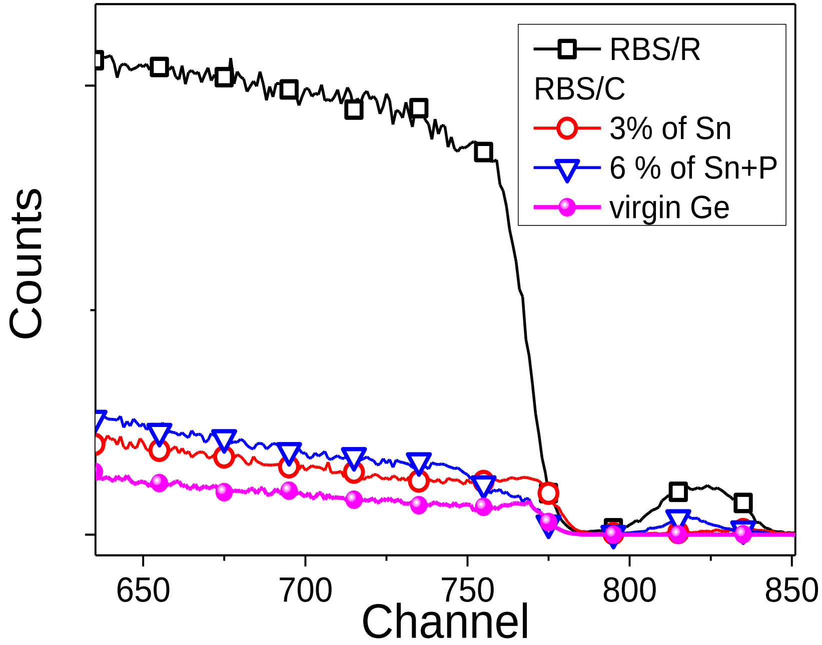
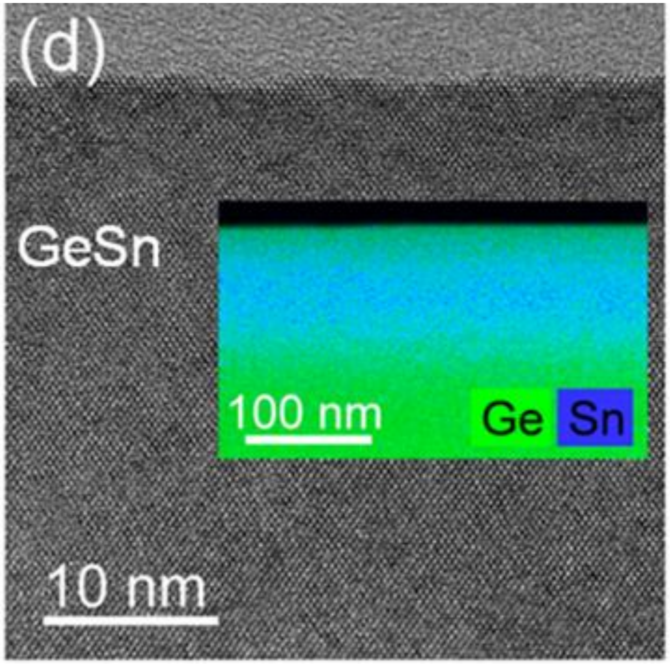
# Material fabrication GeSn

## Ion implantation and FLA

- up to 6% Sn for GeSn on Si



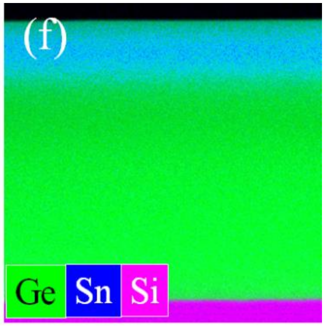



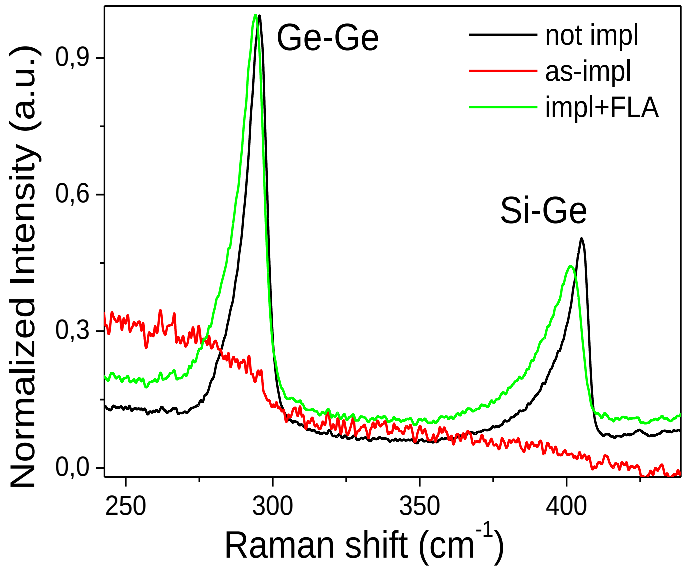

S. Prucnal, Y. Berencén, M. Wang1, L. Rebohle, R. Kudrawiec, M. Polak, V. Zviagin, R. Schmidt-Grund, M. Grundmann, J. Grenzer, M. Turek, A. Drożdziel, K. Pyszniak, J. Zuk, M. Helm, W. Skorupa, and S. Zhou
Band gap renormalization in n-type GeSn alloys made by ion implantation and flash lamp annealing, Journal of Applied Physics, 125 (2019).

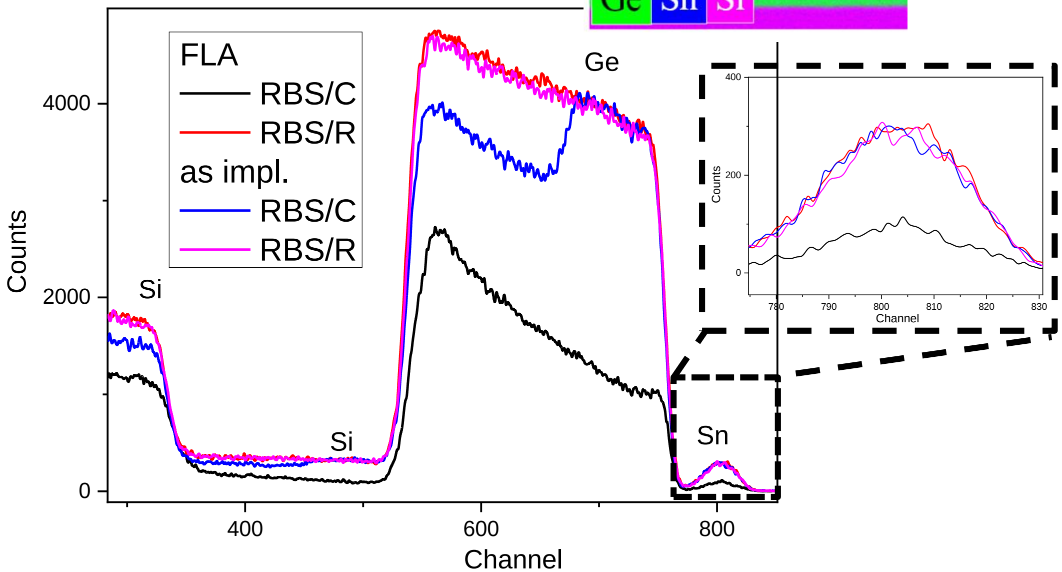
# Material fabrication SiGeSn

## Ion implantation and FLA

- up to 4.5% Sn for SiGeSn on Si



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# Promotionsvorhaben

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- Thema und Projekt -

- Aktueller Stand -

- Material characterisation -

- Ausblick -

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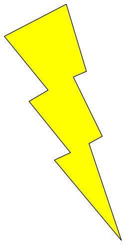
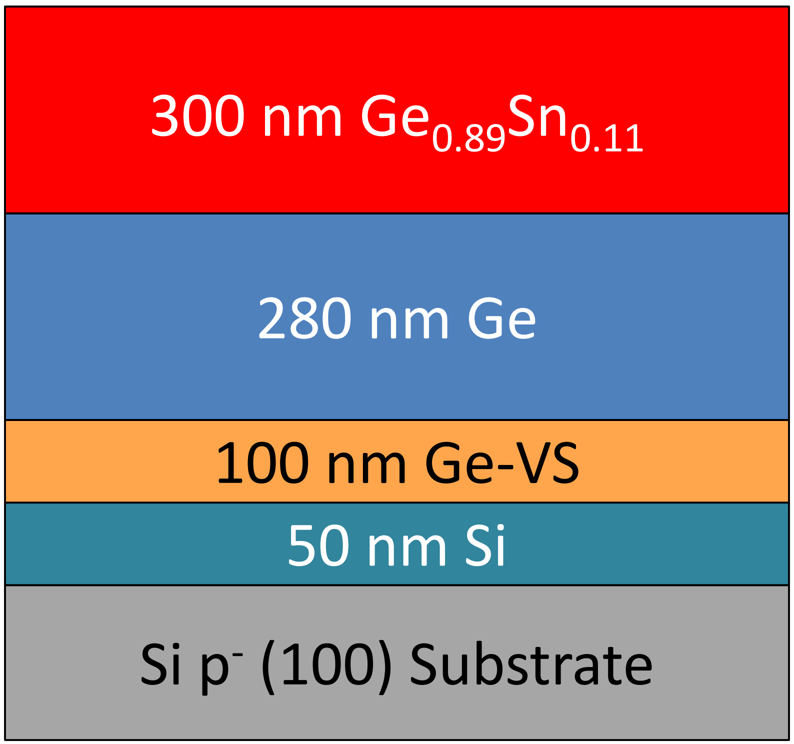
# Band-gap and strain engineering in GeSn alloys using post-growth pulsed laser melting



laser wavelength: 308 nm
annealing time: 28 ns
annealed area: 5x5 mm²




| samples | energy density [J/cm²] |
|---|---|
| a) | 0.20 |
| b) | 0.25 |
| c) | 0.30 |
| g) | 0.35 |
| e) | 0.40 |
| f) | 0.50 |
| g) | 0.60 |

Measurements:
µRaman, HRXRD, TEM, PR
Hall effect,
Positron annihilation spectroscopy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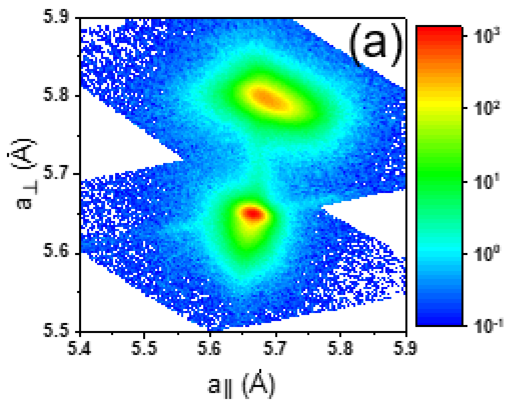
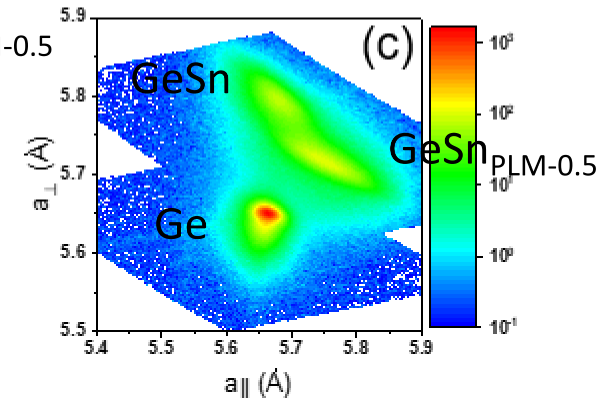
## HRXRD – RSM:

$GeSn_{as\text{-}grown}$




$GeSn_{PLM\text{-}0.5}$




| | Sn (at.%) | $a_\parallel$ (Å) | $a_\perp$ (Å) | $a_0$ (Å) | $\varepsilon_{\parallel\ XRD}$ |
|---|---|---|---|---|---|
| $Ge_{as\text{-}grown}$ | - | 5.6647 | 5.6503 | 5.6575 | 0.0009 |
| $GeSn_{as\text{-}grown}$ | 11.1 | 5.6928 | 5.7944 | 5.7502 | -0.0100 |
| GeSn | 10.2 | 5.6811 | 5.7907 | 5.7430 | -0.0108 |
| $GeSn_{PLM\text{-}0.4}$ | 9.6 | 5.7361 | 5.7394 | 5.7380 | -0.0003 |
| $GeSn_{PLM\text{-}0.5}$ | 8.9 | 5.7478 | 5.7190 | 5.7316 | 0.0028 |
| $GeSn_{PLM\text{-}0.6}$ | 8.9 | 5.7536 | 5.7149 | 5.7318 | 0.0038 |

Compressive strain

Tensile strain



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# Band-gap and strain engineering in GeSn alloys using post-growth pulsed laser melting

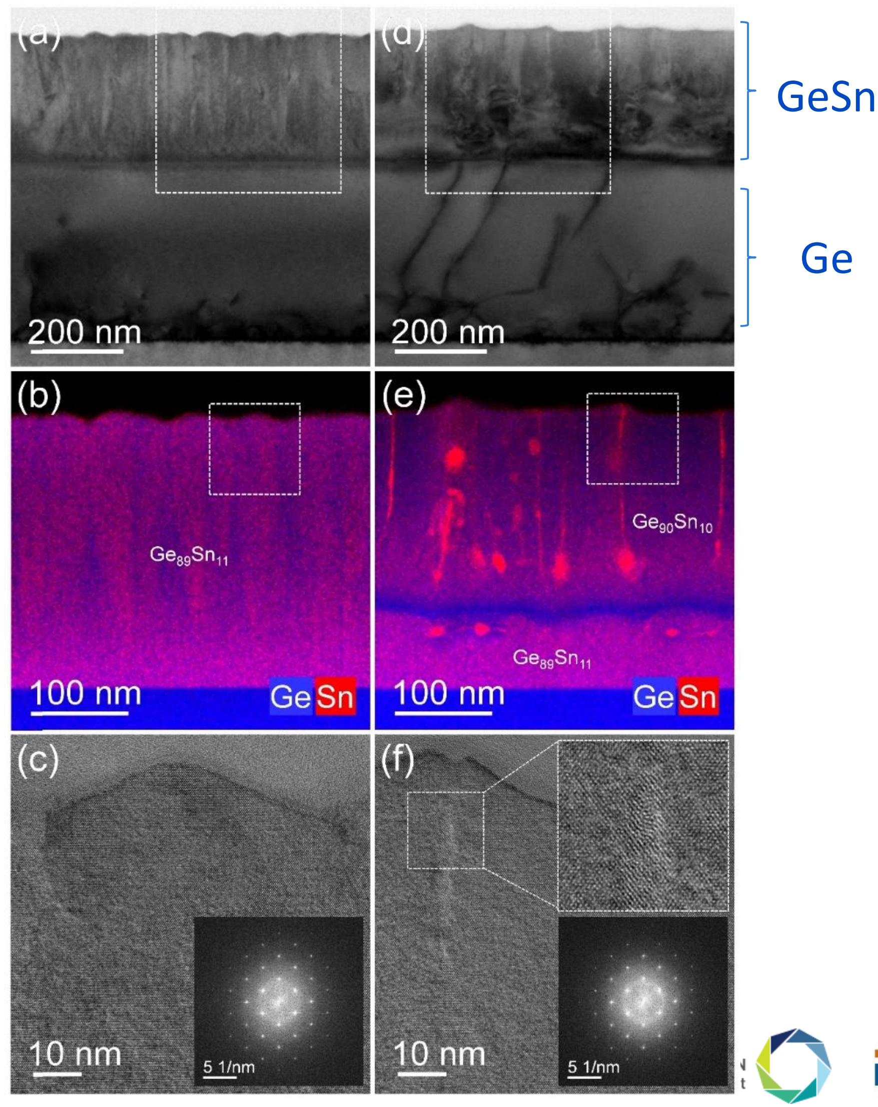
## TEM:

As grown | PLM 0.5 J/cm²

bright-field TEM

EDX

HRTEM



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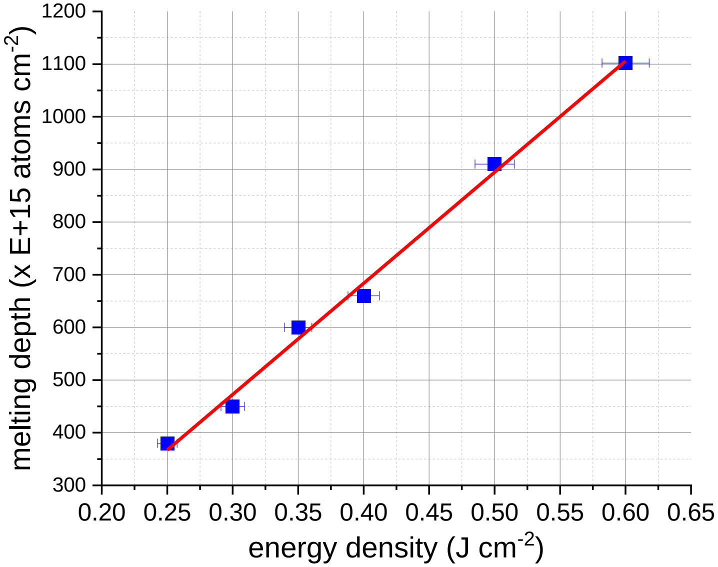
# Band-gap and strain engineering in GeSn alloys using post-growth pulsed laser melting

## Summary:

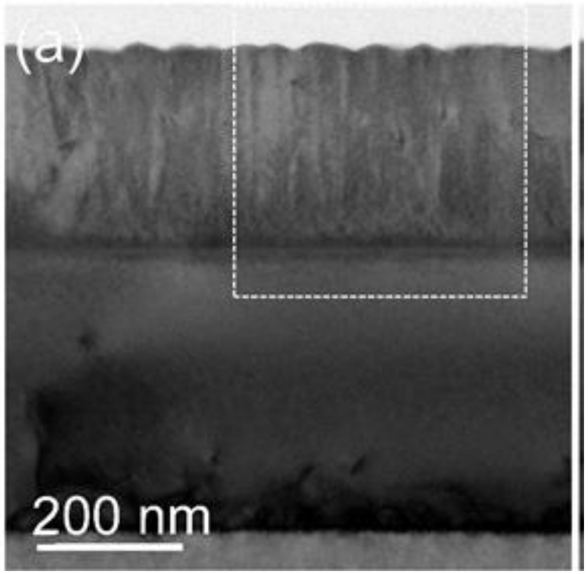
- control of the molten layer thickness
- afterwards still single crystalline samples
- small redistribution of Sn
- direct band gap is about 0.5 eV
- **able to release in plain strain**

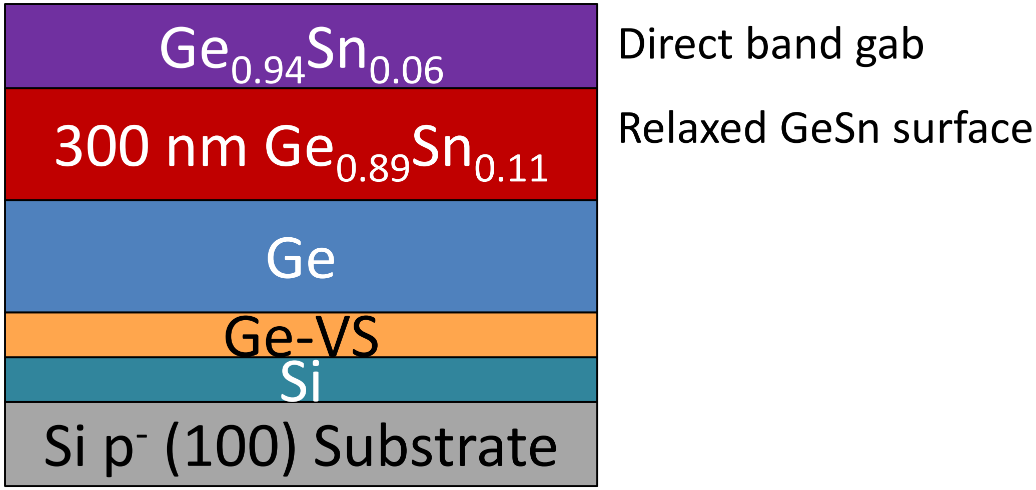


# Band-gap and strain engineering in GeSn alloys using post-growth pulsed laser melting

## Outlook:

- Defect evolution in GeSn
- Relaxed GeSn as virtual substrate for $GeSn_{0,06}$



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# Promotionsvorhaben

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- Thema und Projekt -

- Aktueller Stand -

- Transistor fabrication -

- Ausblick -

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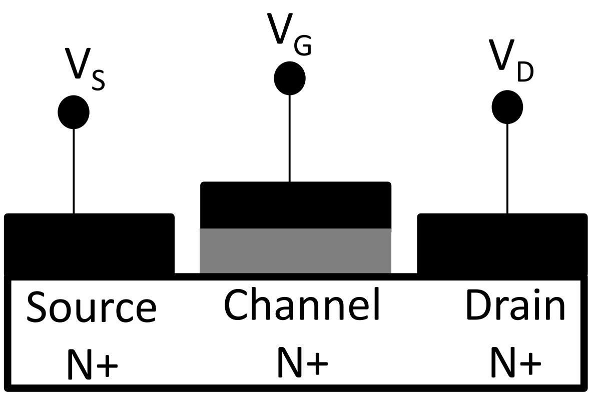
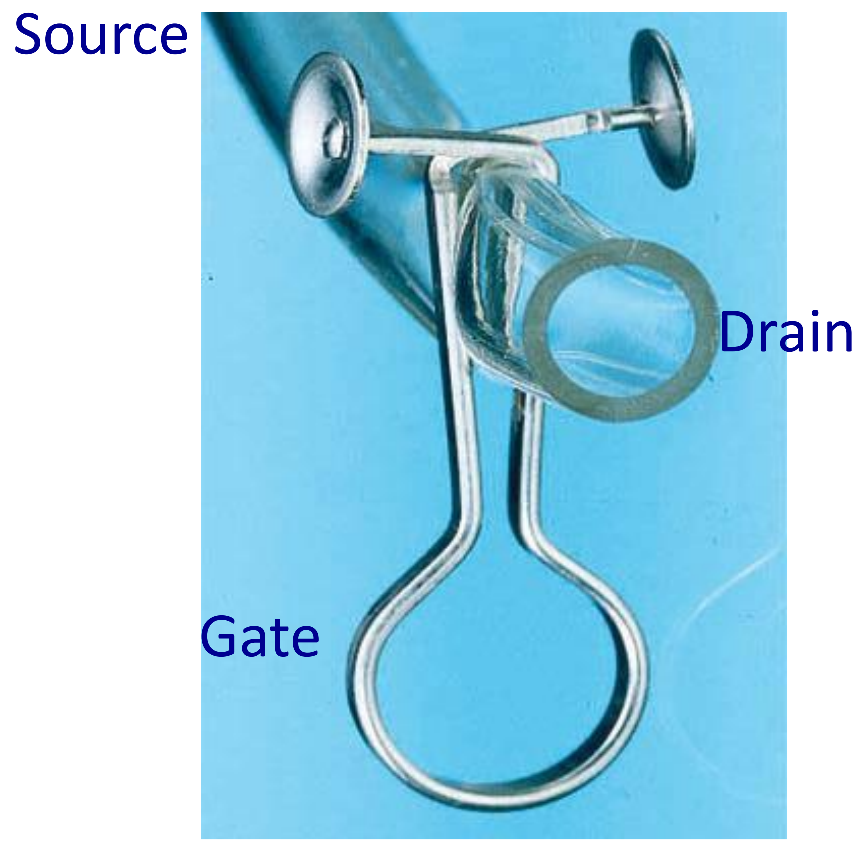
# JL-FET principles

Utilizes a semiconductor film with a gate to control its resistance and hence, the current flowing through it.



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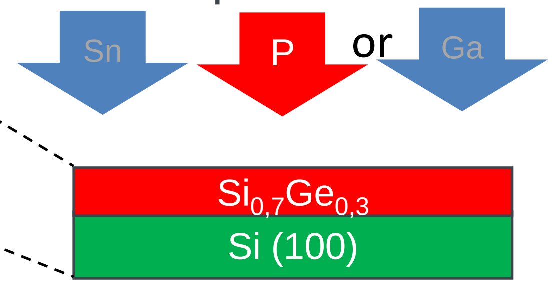
# Fabrication of n-type SiGe-JNT

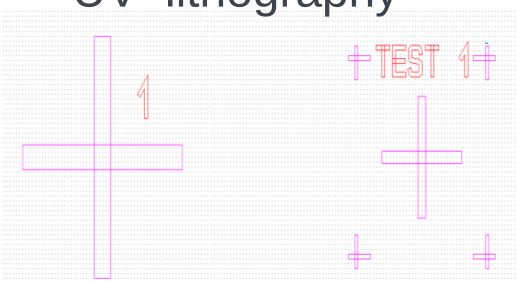
0. initial state


1. Implantation P

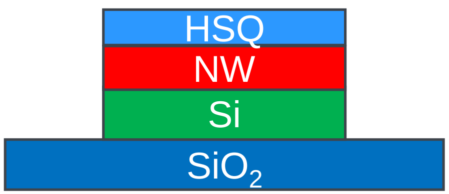



2. FLA


3. Markers
- UV lithography -

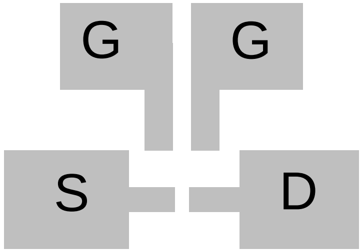



4. Patterning of nanowires (NW)
- E-beam lithography -

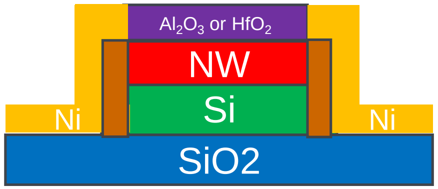



5. Dielectric

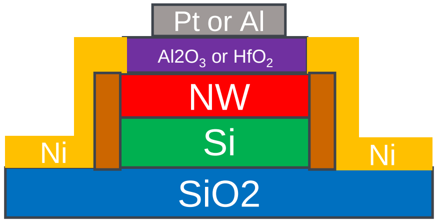

6. S/D/G contact pads
- UV lithography -




7. FLA




8. Gate metal





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# Materials for fabrication

## Ion implantation and FLA

15 nm $Si_{0,7}Ge_{0,3}$
12 nm Si (100)
21 nm $SiO_2$
750 µm Si bulk

P doped SiGe
Ga doped SiGe

15 nm $Si_{0,7}Ge_{0,3}Sn_x$
12 nm Si (100)
21 nm $SiO_2$
750 µm Si bulk

P doped SiGeSn
Ga doped SiGeSn

## Molecular beam epitaxy

20 nm $Si_{1-x-y}Ge_xSn_y$ — MBE
20 nm p-Si (100)
100nm $SiO_2$
Si $p^-$ (100) Substrat

(20 nm p-Si (100), 100nm $SiO_2$, Si $p^-$ (100) Substrat: SOI wafer)

20 nm Ge:Sb

**20 nm $Ge_{0.94}Sn_{0.06}$:Sb**

20 nm $Si_{0.15}Ge_{0.85}$:Sb

20 nm $Si_{0.14}Ge_{0.8}Sn_{0.06}$:Sb


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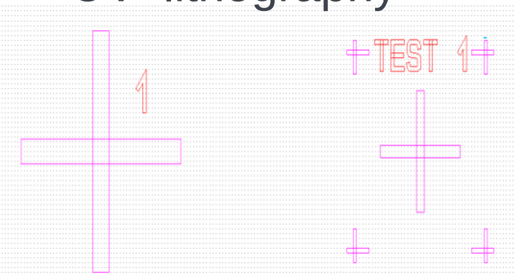
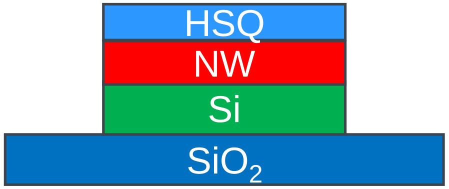
# Fabrication of n-type GeSn-JNT

1. Markers
- UV lithography -

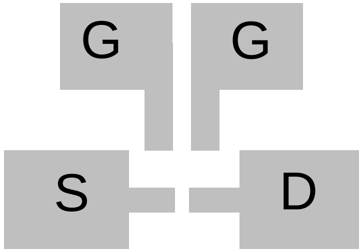



2. Patterning of nanowires (NW)
- E-beam lithography -



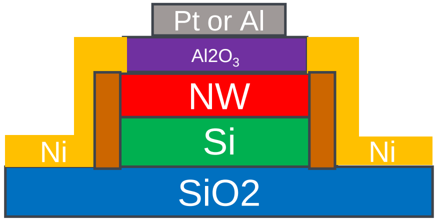

3. Dielectric


4. S/D/G contact pads
- UV lithography -

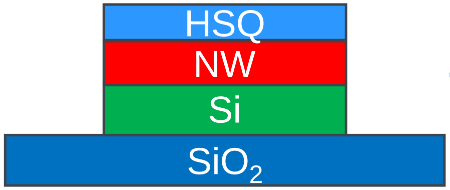



5. FLA


6. Gate metal

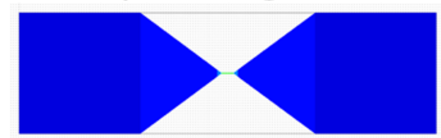


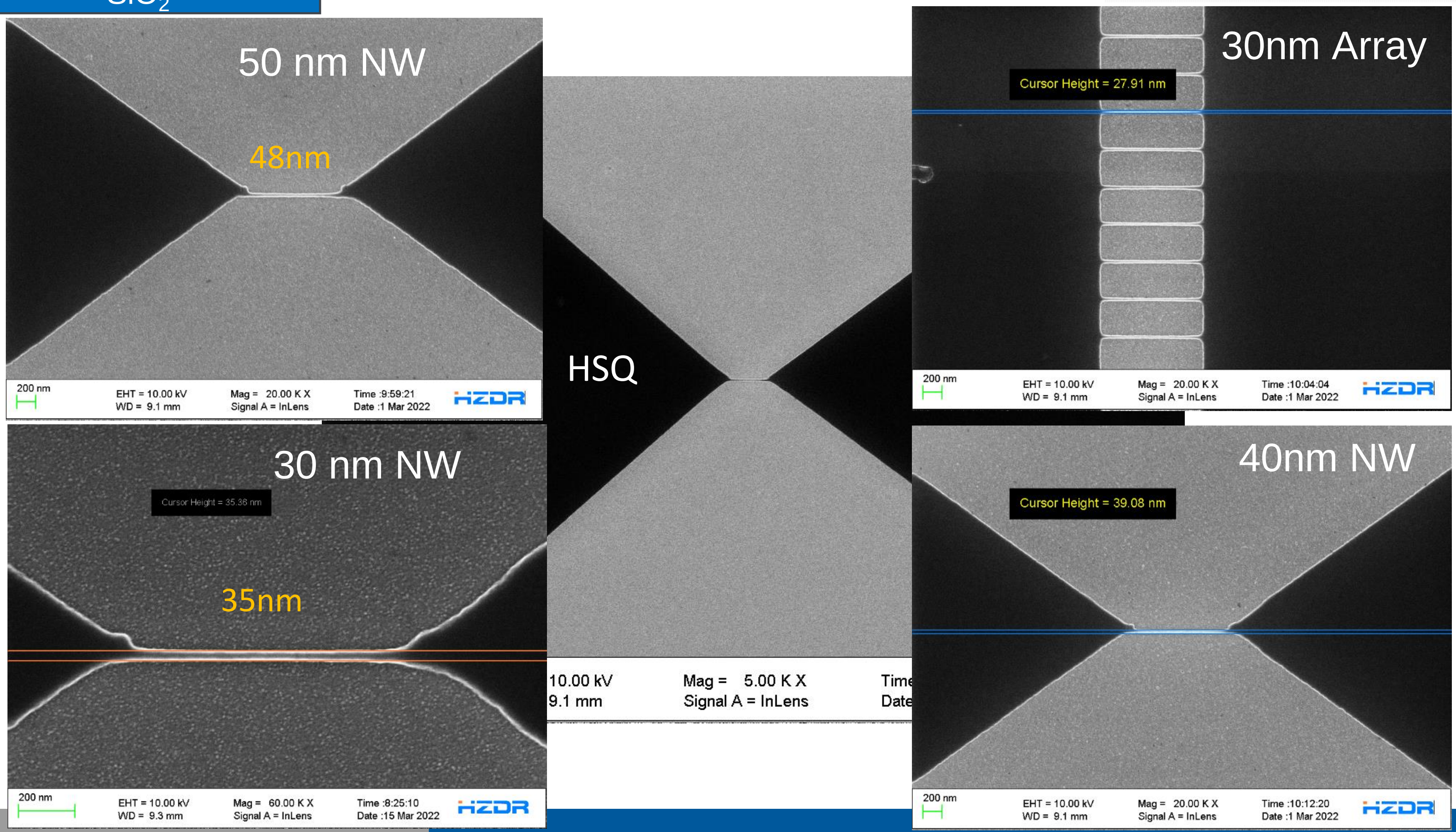
# Fabrication of n-type GeSn-JNT




## 2. Patterning of nanowires (NW)
## - E-beam lithography -

1µm long NW





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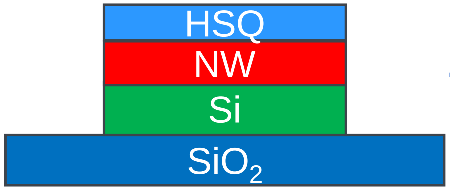
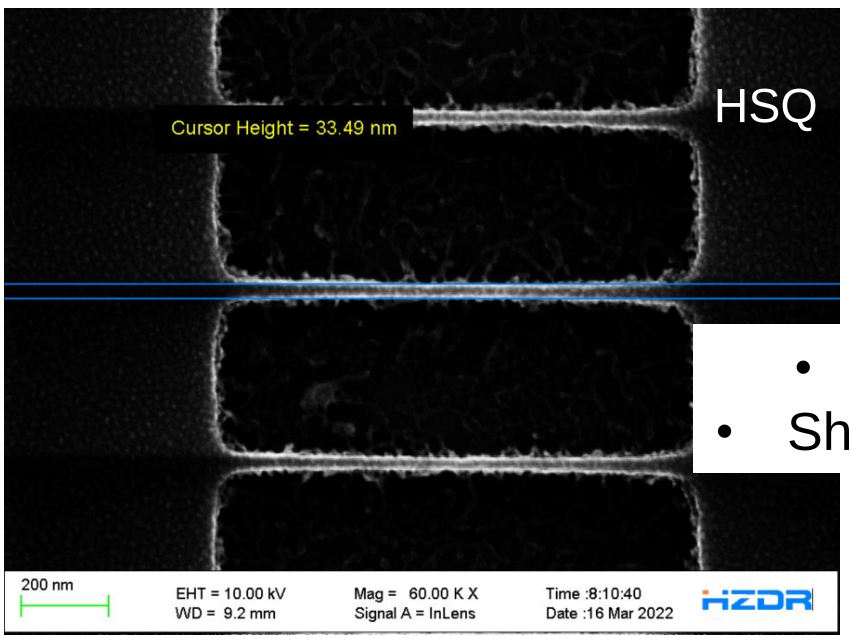
# Fabrication of n-type GeSn-JNT




## 2. Patterning of nanowires (NW)
## - RIE -

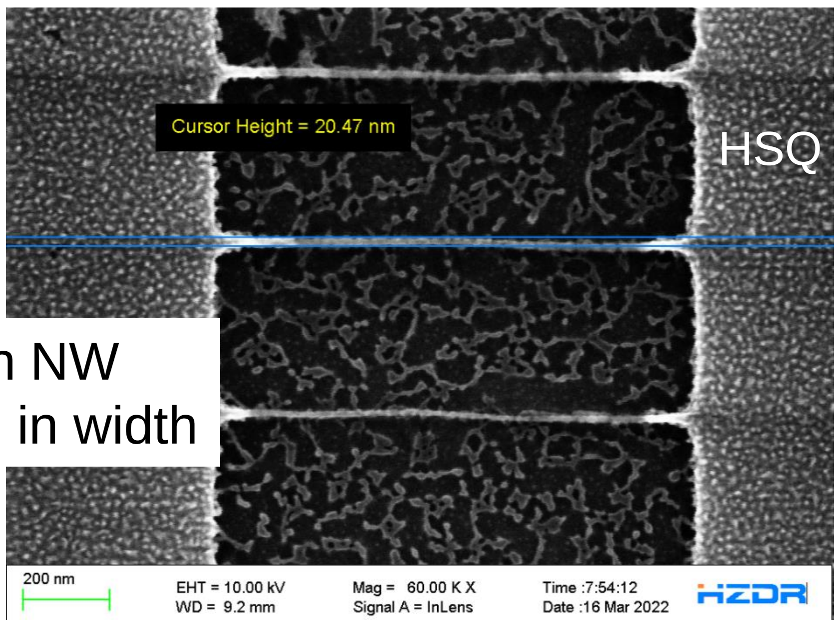
### A) F-Based RIE

C4F8 = 22 sccm; SF6 = 10sccm; O2 = 5 sccm
Pressure = 0.9 Pa ICP power = 400 W
**RF power = 12 W Etch time = 28 s**




### B) F-Based RIE

C4F8 = 22 sccm; SF6 = 10sccm; O2 = 5 sccm
Pressure = 0.9 Pa ICP power = 400 W
**RF power = 14 W Etch time = 30 s**




- Rough NW
- Shrinking in width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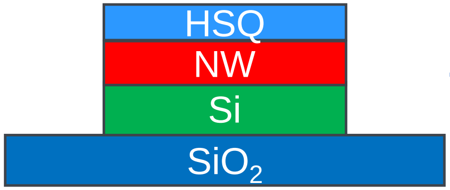
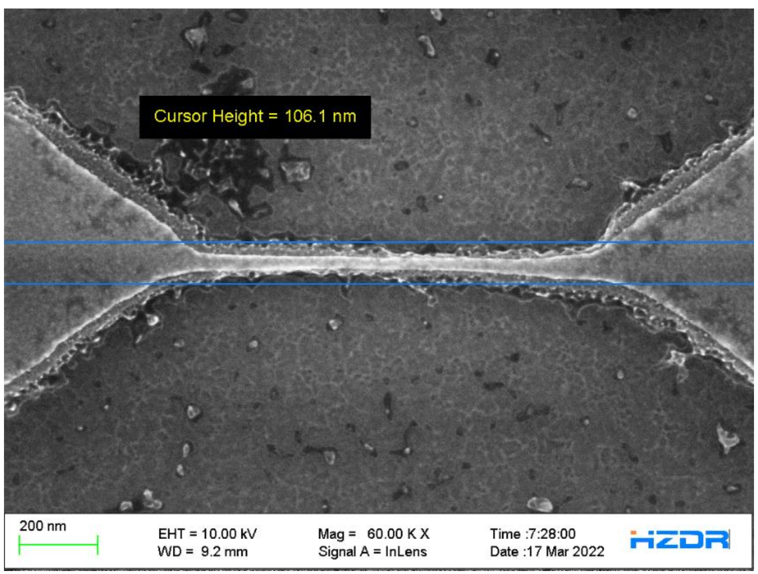
# Fabrication of n-type GeSn-JNT




## 2. Patterning of nanowires (NW)
## - HSQ removal -

### A) F-Based RIE

C4F8 = 22 sccm; SF6 = 10sccm; O2 = 5 sccm
Pressure = 0.9 Pa ICP power = 400 W
**RF power = 12 W Etch time = 28 s**

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C4F8 = 22 sccm; SF6 = 10sccm; O2 = 5 sccm
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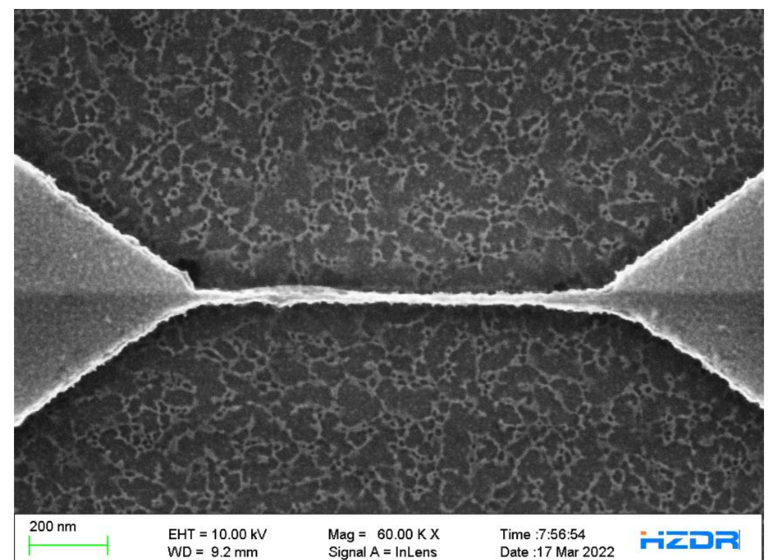


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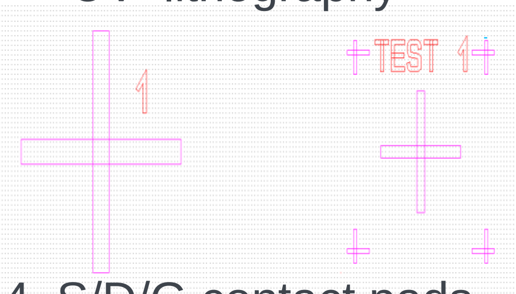
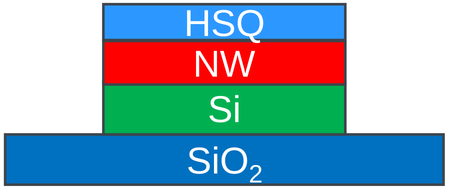
# Fabrication of n-type GeSn-JNT

1. Markers
- UV lithography -

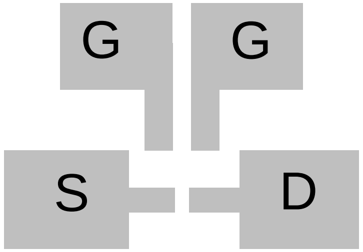



2. Patterning of nanowires (NW)
- E-beam lithography -



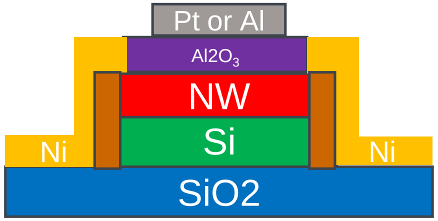

3. Dielectric


4. S/D/G contact pads
- UV lithography -




5. FLA


6. Gate metal



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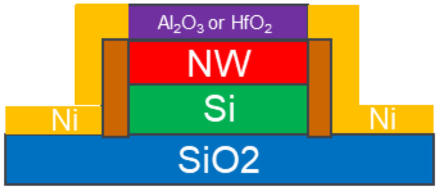
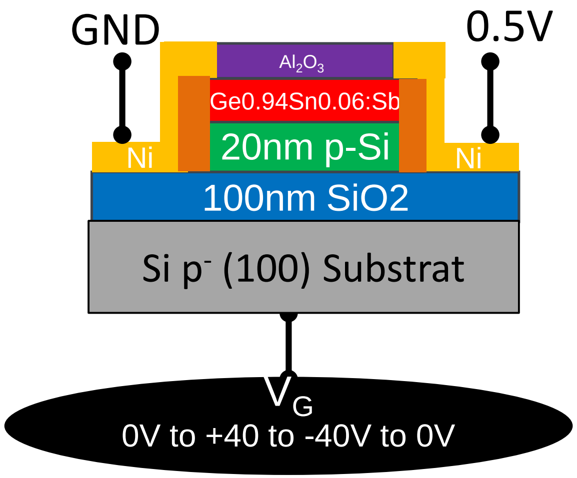
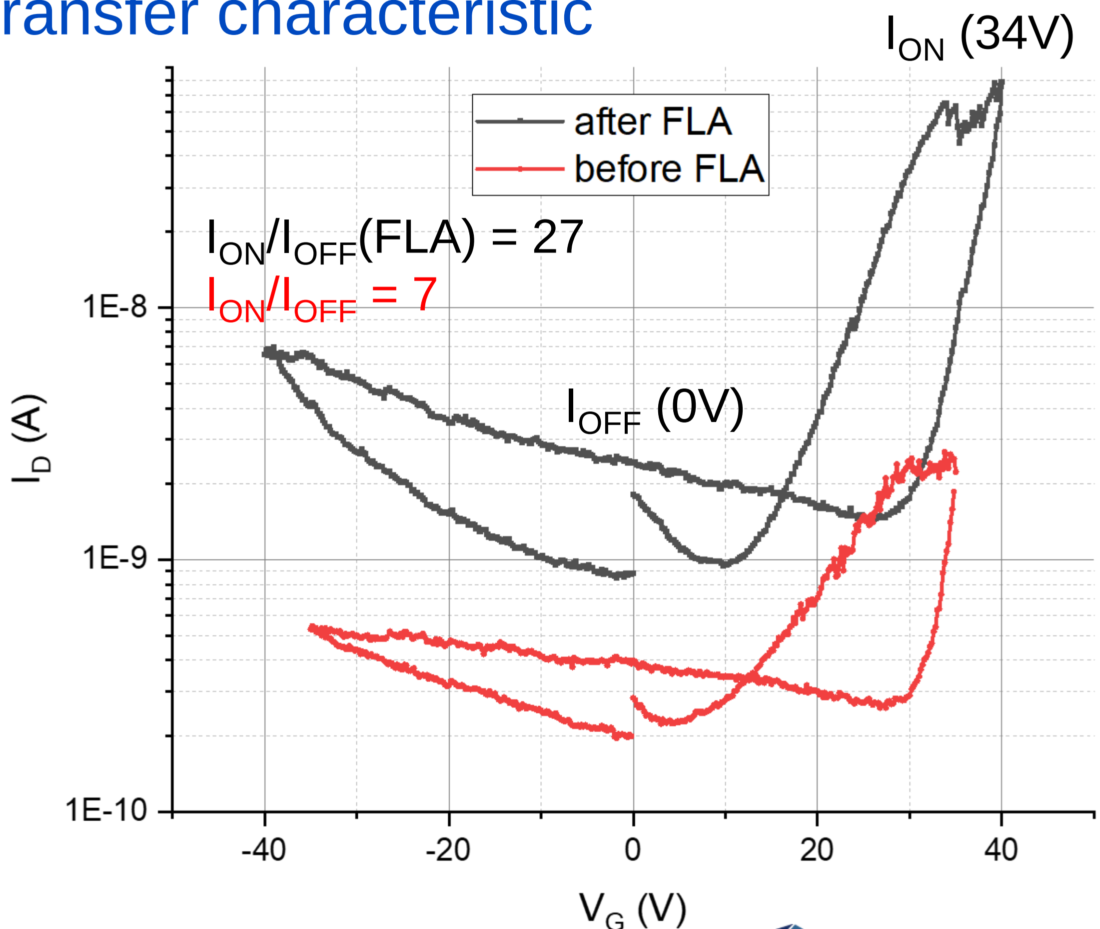
# Fabrication of n-type GeSn-JNT

5. FLA




## 5. Electrical characterisation
## BG-transfer characteristic



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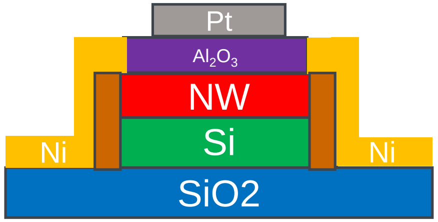
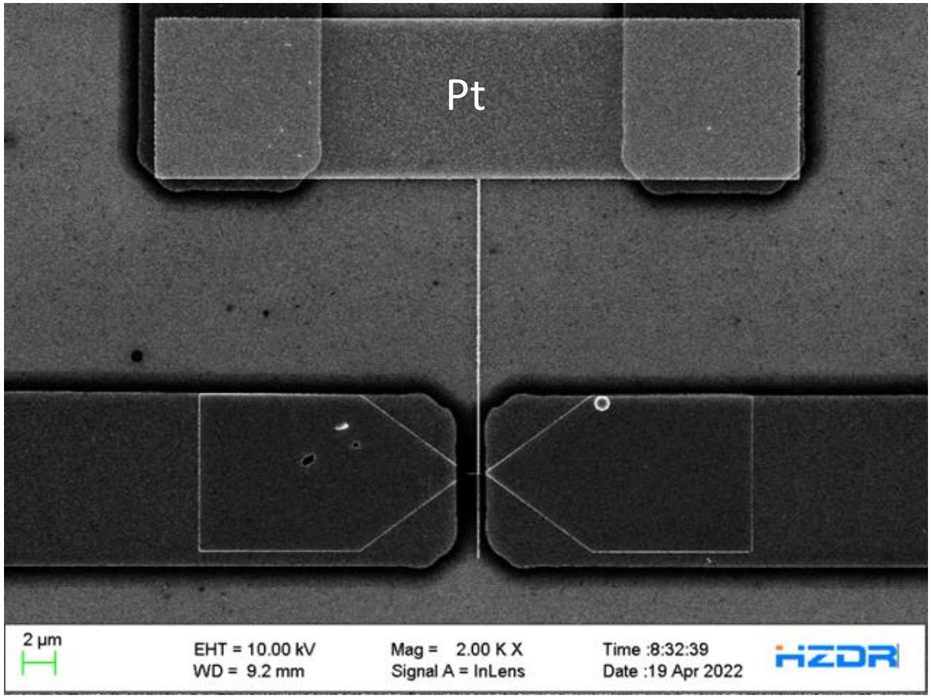
# Fabrication of n-type GeSn-JNT

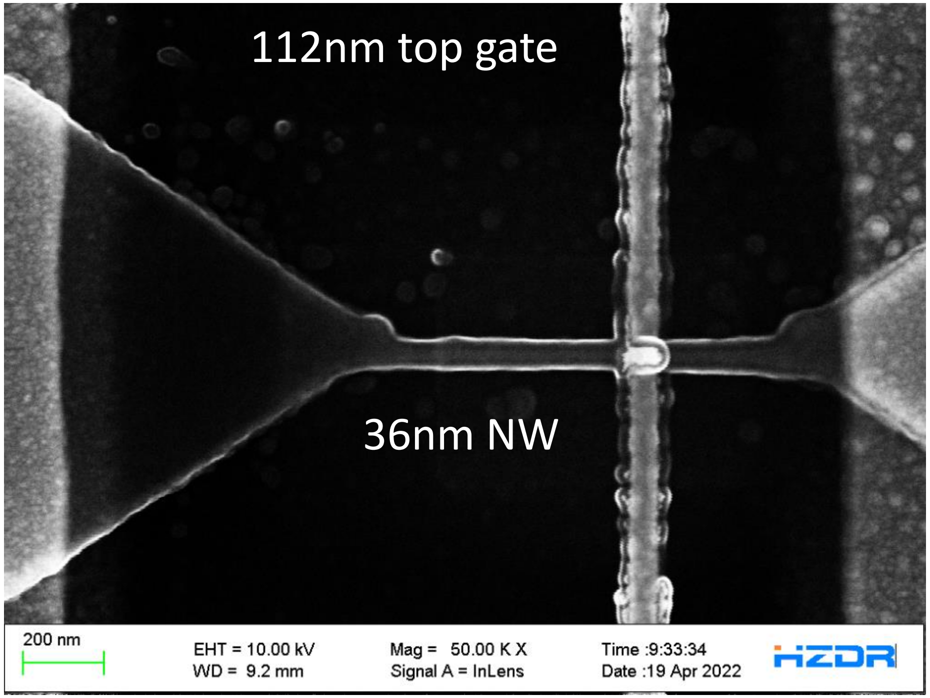
6. Gate metal




## 6. Top gate

- Electrical characterisation
- TEM

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# Promotionsvorhaben

# Oliver Steuer

- Thema und Projekt -

- Aktueller Stand -

- Ausblick -

**Oliver Steuer**

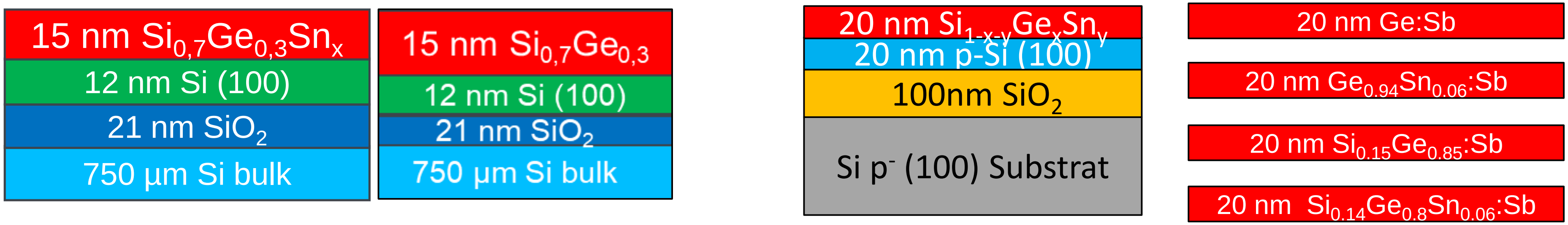
**06.05.2022**

**Institute of Ion Beam Physics and Materials Research**

**Helmholtz-Zentrum Dresden-Rossendorf**

# Outlook and PhD topic

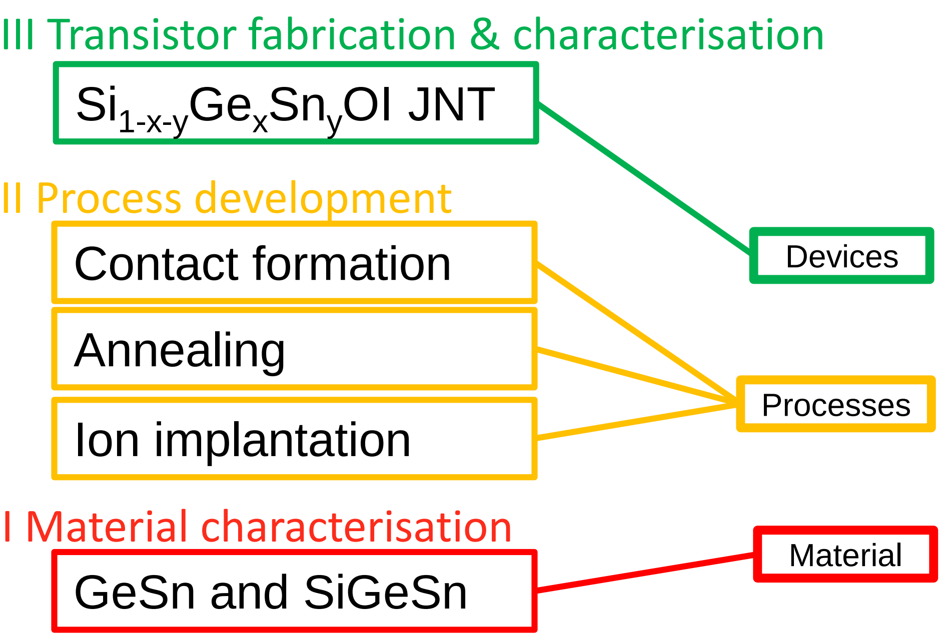
## Group IV heterostructures for future nanoelectronic devices




- Electrical charakertsation
  - 4 types of Sn implanation
  - 6 transistors MBE

- Influence of FLA of $Al_2O_3$ on Ge and Si
- Ion implantationen P, Ga and Sn
- Contact formation (CTLM)

- Band gab and strain engineering
- Defect investegation in GeSn and SiGeSn
- Virtual Substrate for GeSn and SiGeSn
- Material for transistors




Topic?: Fabrication and characterisation of $Si_{1-x-y}Ge_xSn_y$ alloys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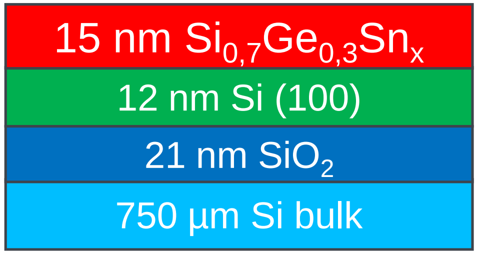
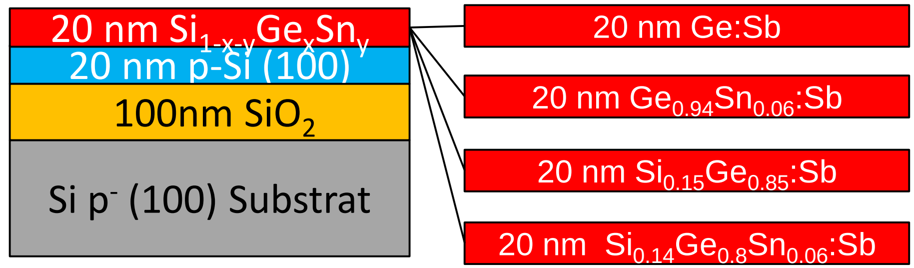
# Pitfalls




- Thin films difficult for material characterisation
- Si below main layer
- Cleanroom HZDR not always open (Corona + construction site April- September)
- RIE in partner institute
- Sn segregation during processes possible
- Delays in processes due to broken tools



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