TECHNISCHE UNIVERSITÄT DRESDEN

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Faculty of Mechanical Engineering Institute of Materials Science, chair „materials science and nanotechnology“

# Silicon-Nanowire Field Effect Transistors as Bio-Sensors

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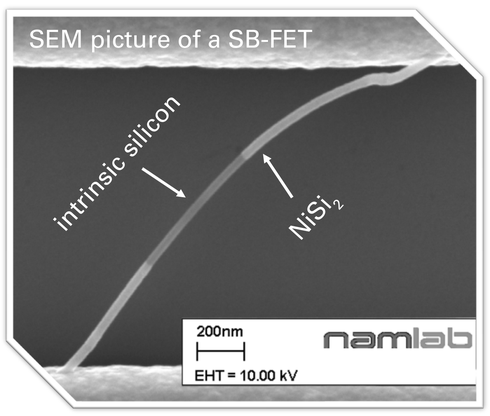
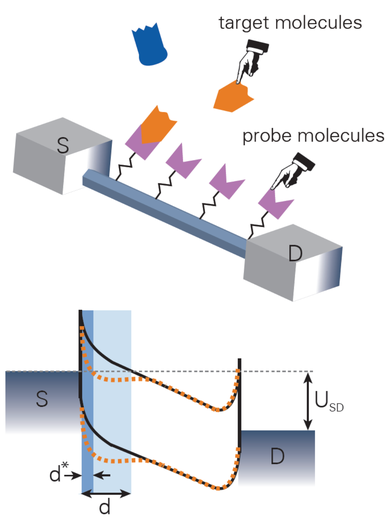
## Thesis: sensing with modulation of Schottky barriers?

**Single nanowire FET with intruded Ni contacts**

- annealing leads to axial diffusion of Ni into the nanowire
- metallic $NiSi_2$ is formed with a atomic sharp interface to the intrinsic silicon of the wire

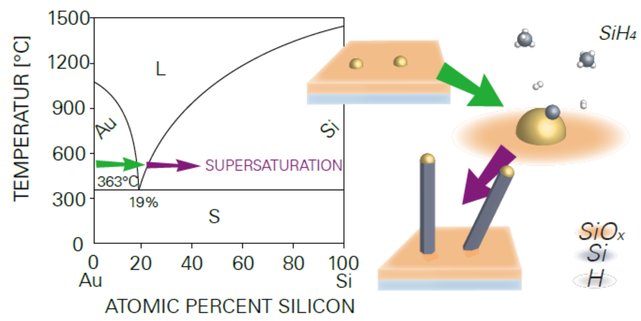


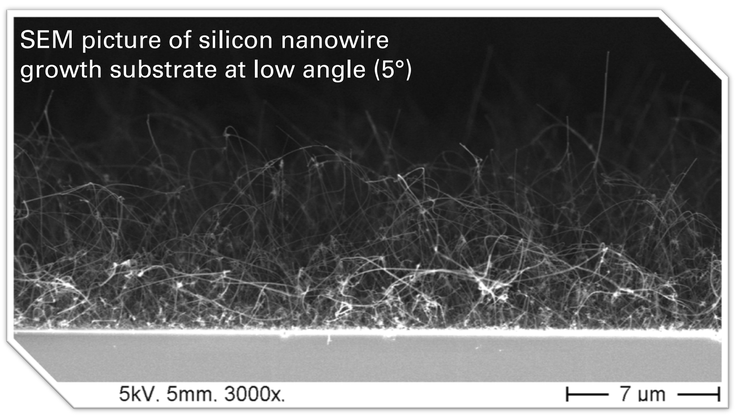



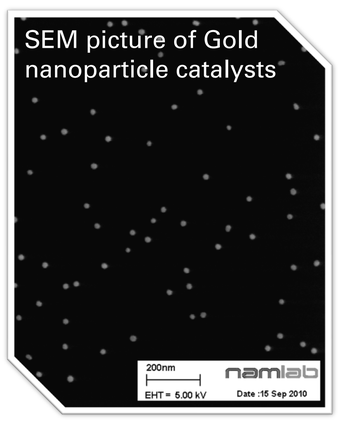

- atomic sharp metal-semiconductor interface poses defined Schottky barriers (SB-FET)
- effective manipulation of barrier height with applied electric fields (gate voltage) is possible
- binding events of target and probe molecules near Schottky barriers lokally bend bands and lower energy barriers for electrons or holes

## Nanowire growth via VLS (vapor liquid solid)

- bottom up synthesis of silicon nanowires in CVD furnace via VLS method with silane as precursor
- Gold particles with a diameter of 20nm made by Turkevich method serve as catalyst
- growth time of 10min at 450°C with a diluted silane gas ($SiH_4/H_2$ = 1/10) flow of 200sccm (60Torr) leads to 7-10µm long monocrystalline silicon nanowires



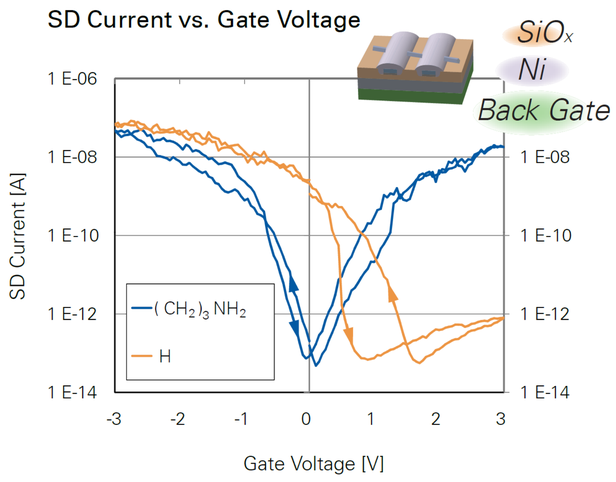



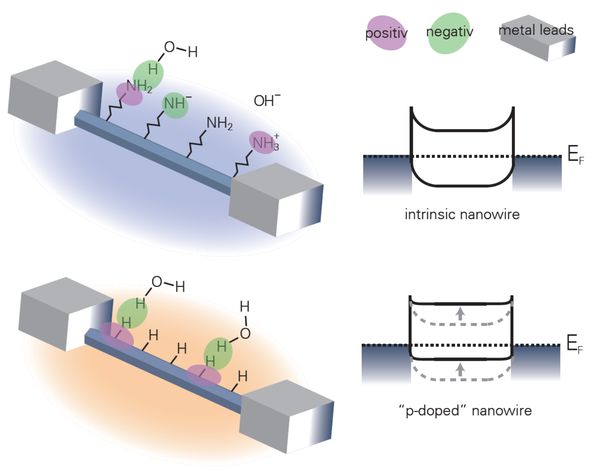




## Electrical characteristics of single nanowire FETs

**Back gated single nanowire FET**

- 20nm thermal silicon oxide gate dielectric, source-drain (SD) voltage 0.5V
- $(CH_2)_3NH_2$ (alkane chain) terminated wires show ambipolar behaviour
- untreated wires behave like p-doped wires (unipolar behaviour)
- totally different IV characteristics, not just a simple shift like it is expected for a change in surface charge



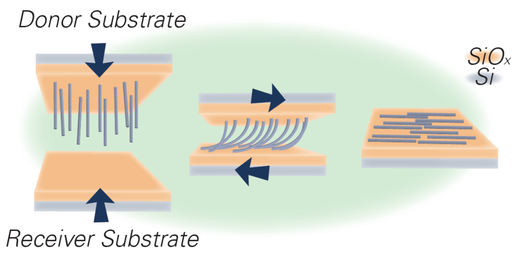




**Suggested mechansim**

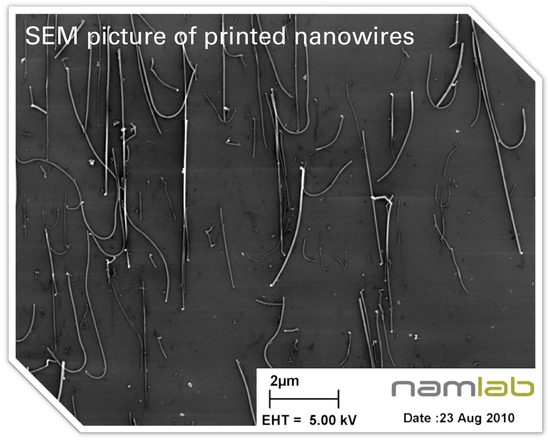
- surface Fermi level pinning or „doping“(charge transfer) due to polar molecules like $H_20$
- „p-doped“ nanowires: lower barrier for holes, higher barrier for electrons lead to rectified charge transport
- alkane chains shield from polar molecules and possible charge transfer

## Creation of parallel arrays of nanowire FETs

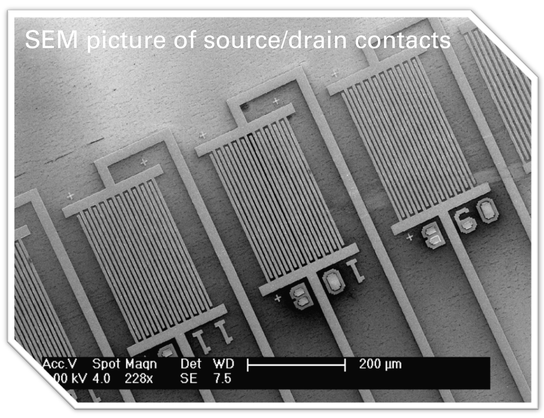
**Increase of sensitive area and signal amplitude compared to single nanowire FETs**

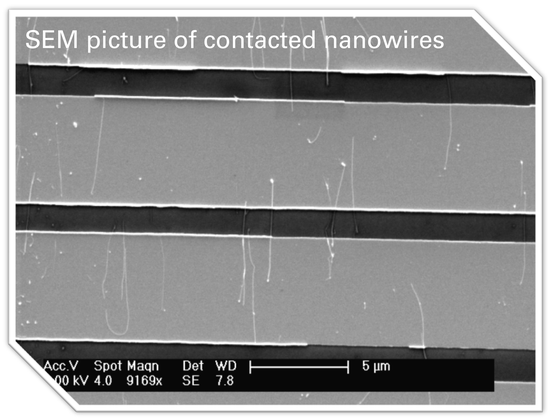



- alignment of nanowires with contact printing technique to obtain ordered arrays horizontally on silicon oxide




- top-down lithographical methods for defining Ni contacts on nanowire arrays
- interdigitated fingers design for source/drain contacts

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